SIMULATION OF SHORT CHANNEL VERTICAL MOSFET STRUCTURES

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LIST OF SYMBOLS

ϕ_S	Surface potential
ϕ_F	Fermi potential
$\overline{\mu}_n$	Surface electron mobility
μ	Electron mobility
C_D	depletion MOS capacitance
C_i	Insulator capacitance
C_{it}	Interface-state MOS capacitance,
d_{max}	Channel depletion width
I_D	Drain current
I_{off}	Off-state leakage current
J_D	Drain current density in two dimension
J_{off}	Off-state leakage current density in two dimension
k	Boltzmann's constant
L	Gate/channel length
N_a	Concentration of acceptors
N_C	Channel doping concentration,
n_i	Intrinsic concentration of electrons
q	Magnitude electron charge
Q_d	Charge in the depletion region at strong inversion
Q_i	Effective MOS interface charge
r_j	Diffused junction depth
T	Temperature in unit Kelvin
t_{ox}	Gate oxide thickness
V_{DS}	Drain voltage
V_{GS}	Gate voltage
V_{th}	Threshold voltage
W_B	Width of the body region between the two channels
W_C	Spacing between the pocket and the gate oxide
W_D	Drain depletion width
W_S	Source depletion width
Z	Width of the channel
Φ_{ms}	Metal-semiconductor work function potential difference

LIST OF ABBREVIATIONS

2-D	Two dimension
BTBT	Band-to-band tunneling
DC	Direct current
DIBL	Drain induced barrier lowering
DP	Dielectric pocket
DP-VMOST	Vertical MOSFET incorporating a dielectric pocket
FD- SOI	Fully depleted silicon on insulator
FILOX	Fillet local oxidation
FinFET	Fin field effect transistor
GIDL	Gate induced drain leakage
ICs	Integrated circuits
ITRS	International technology roadmap for semiconductor
MOS	Metal oxide semiconductor
MOSFET	Metal oxide semiconductor field effect transistor
S	Subthreshold slope
SCEs	Short-channel effects
SDE	Source drain extension
SOI	Silicon on insulator
SSD	Solid source diffusion
TCAD	Technology computer-aided design
VMOST	Vertical MOSFET
VMOST-EL	VMOST growth with epitaxial layers
VRG	Vertical replacement gate
VWF	Virtual Wafer Fabrication

SIMULASI STRUKTUR SALURAN PENDEK MOSFET MENEGAK

ABSTRAK

Baru-baru ini, penghujung bagi pelengkap semikonduktor logam oksida (CMOS) mendatar sudah semakin nyata. Transistor kesan medan semikonduktor oksida logam (MOSFET) menegak (VMOST) adalah salah satu struktur yang menjanjikan untuk masa depan teknologi CMOS. Masih banyak kajian perlu dilakukan pada struktur VMOST agar akan mantap seperti teknologi CMOS mendatar. Telah diketahui bahawa ada banyak parameter perlu mempertimbangkan dalam rekabentuk sebuah MOSFET. Dengan bantuan rekabentuk teknologi komputer tambahan (TCAD), parameter-parameter bagi MOSFET boleh diubahsuai dengan cepat dan jimat kos. Projek ini berdasarkan kepada dua dimensi (2D) simulasi kerja. Simulator yang digunakan adalah ATHENA, DEVEDIT dan ATLAS keluaran SILVACO International masing-masing bagi struktur peranti dan ciri-ciri elektrik dari peranti parameter struktur dengan yang dicadangkan dengan mekanisme fizikal dalaman berkaitan dengan operasi peranti. Tujuan projek ini adalah untuk mempelajari struktur NVMOST seperti VMOST dengan pertumbuhan lapisan epitaxial (VMOST-EL), MOSFET menegak menggabungkan saku dielektrik (DP-VMOST) dan get penggantian menegak (VRG) MOSFET. Untuk VMOST-EL, kesan daripada pelbagai pengedopan saluran kepekatan, N_C, pada 80 dan 50 nm panjang saluran yang dibincangkan. VMOST-EL dengan 50 nm bagi L dan 2 x 10^{18} cm^{-3} bagi N_C, V_{th}, J_D dan J_{off} masing-masing ialah 0.22 V, 1227 µA/µm and 2.8 x 10^{-7} A/µm. Keputusan kajian menunjukkan bahawa N_C banyak mempengaruhi ciri-ciri elektrik. Selain itu, kesan dari jarak antara saku dielectrik dan get oksida, W_C, pada pelbagai N_C diperiksa pada DP-VMOST. DP-VMOST dengan W_C = 10 nm dan N_C =

2 x 10^{18} cm^{-3} mempunyai 1024 μA/μm bagi J_D, 2.2 x 10^{-8} A/μm bagi J_{off} dan 0.32 V bagi V_{th}. DP banyak mengurangkan susutan dari salir ke saluran serta persimpangan pn yang menyumbang terhadap prestasi saluran pendek sub-100 nmVMOST lebih baik. Tambahan pula, ada kemungkinan untuk mengawal ciri elektrik peranti dengan hanya mengubah W_C berbanding mengendalikan kepekatan pengedopan saluran atau ketebalan get oksida. Perbandingan dengan kerja Donaghy et al. (2004), trend yang beza bagi J_{off}, apabila pengedopan saluran kepekatan 3 x 10^{18} cm^{-3}, nilai yang diperoleh adalah lebih rendah daripada J_{off} bagi N_C = 4 x 10^{18} cm^{-3}. Fenomena ini kemungkinan disebabkan of model yang diguna untuk pencirian. Akhirnya, untuk VRG-MOSFET, kesan dari lebar bagi kawasan jasad antara dua saluran, W_B, dengan pelbagai N_C juga dikaji. Ia menunjukkan bahawa jasad keupayaan yang akan menyebabkan kawasan jasad menjadi separa atau sepenuhnya tersusut banyak dipengaruhi apabila W_B dan N_C rendah. Bagi VRG MOSFET dengan L = 50 nm, N_C = 3.5 x 10^{18} cm^{-3} dan W_B = 200 nm, ia menunjukan 0.53 V bagi V_{th}, 482.6 μA/μm bagi J_D dan 3.31 x 10^{-13} A/μm bagi J_{off}. Sebaliknya, hasil Hergenrother et al. (1999) dengan 50 nm bagi L and 3.5 x 10^{18} cm^{-3} bagi N_C, ia menunjukan 0.73 V bagi V_{th}, 5 x 10^{-10} A/μm bagi J_{off} dan 68 μA/μm bagi I_D. Perbezaan ini disebabkan simulasi ini hanya dalam 2-D struktur MOSFET VRG. Manakala, struktur yang diperkenalkan oleh Hergenrother et al. (1999) ialah “persegi panjang” mengelilingi struktur dengan 16.4 μm bagi lebar.

SIMULATION OF SHORT CHANNEL VERTICAL MOSFET STRUCTURES

ABSTRACT

Recently, the end of the planar bulk complementary metal oxide semiconductor (CMOS) had become visible. Vertical metal oxide semiconductor field effect transistor (VMOST) structures are one of the promising structures for future CMOS technologies. There are still a lot of research needs to be done on the VMOST structures to mature as that of planar CMOS technologies. It is well known that there are many parameters needed to be considered in designing MOSFET. With the aid of computer-aided design, we can optimize the MOSFET parameters faster and with lower cost. This project is based on two-dimension (2D) simulation works. Simulators used are ATHENA, DEVEDIT and ATLAS from SILVACO International. ATENA and DEVEDIT are used to simulate the device structures. Meanwhile, ATLAS is used to predict the electrical outputs of the proposed parameters device structures with insight into the internal physical mechanisms associated with device operation. The aim of this project is to study NVMOST structures, which are VMOST growth with epitaxial layers (VMOST-EL), vertical MOSFET incorporating dielectric pocket (DP) (DP-VMOST) and vertical replacement gate (VRG) MOSFET. For VMOST-EL, the effects of various channel doping concentration, N_C, on 80 and 50 nm channel length are discussed. VMOST-EL with L of 50 nm and N_C of 2 x 10^{18} cm^{-3}, has the V_{th}, J_D and J_{off} of 0.22 V, 1227 µA/µm and 2.8 x 10^{-7} A/µm, respectively. The results revealed that N_C have significant influence on electrical behaviours. Besides, for DP-VMOST structures, the effects of spacing between the pocket and the gate oxide, W_C, on various N_C are examined. DP-VMOST with W_C = 10 nm and N_C = 2 x 10^{18} cm^{-3} has J_D of 1024

μA/μm, J_{off} of 2.2 x 10^{-8} A/μm and V_{th} of 0.32 V. The DP strongly decreases the depletion from drain to the channel as well as the p-n junction area which contribute to better short channel performance sub-100 nm VMOST. Additionally, there is a possibility to control the device output by only vary the W_C rather than controlling the doping concentration or gate oxide thickness. As we compared to Donaghy et al. (2004) work, the trends are different for J_{off}, at a channel doping concentration of 3 x 10^{18} cm^{-3}, the value of J_{off} obtained is lower than N_C of 4 x 10^{18} cm^{-3}. This phenomenon may due to the models used for characterization. Finally, for VRG-MOSFET, the effects of the width of the body region between the two channels, W_B, with various N_C are also investigated. It showed that body potential is strongly affected by the low W_B and $N_{C,}$ which will cause the body region to become partial depleted or fully depleted. For VRG MOSFET with L = 50 nm, N_C = 3.5 x 10^{18} cm^{-3} and W_B = 200 nm, it shows V_{th} of 0.53 V, J_D of 482.6 μA/μm and J_{off} of 3.31 x 10^{-13} A/μm. In contrast, work by Hergenrother et al. (1999) with L of 50 nm and N_C of 3.5 x 10^{18} cm^{-3} showed V_{th} of 0.73 V, J_{off} of 5 x 10^{-10} A/μm and J_D of 68 μA/μm. The disagreements exist because the simulation in this work is only available in 2-D VRG MOSFET structures. However, the structure introduced by Hergenrother et al. (1999) is “rectangular” surround structure with the width of 16.4 μm.

CHAPTER 1

INTRODUCTION

1.1 Introduction

In the early 1930s, Lilienfeild (1930) was the first, and followed by Heil (1935) to propose the principle of the surface field effect transistor. Then, Shockley and Pearson (1948) studied the modulation of conductance of thin films of semiconductors by surface charges. After that, Kahng and Attala (1960) reported the first demonstration of a silicon-silicon dioxide metal oxide semiconductor (MOS) transistor. Since that, MOS transistors started to be an important device in electronic industry. At that moment, the basic device characteristics have been subsequently explored by Ihantola and Moll (1964), Sah (1964), and Heiman and Hofstein (1963). Until now, the study of the MOSFET is still going on (Tewksbury, 1981; Shin et al., 1992; Wang et al., 2008; Flachowsky et al., 2008 and Griffoni et al. 2010).

MOSFET had been successfully undergone scaling to improve performance and followed the Moore's Law (Moore, 1965) as the number of components on a single piece of silicon had doubled every year over the last few decades. The main reason of this phenomenon is due to the fact it could be scaled to smaller dimensions which improved the integrated circuit performance such as speed, packing density and power consumption. Table 1.1 shows the comparison of the critical parameters

which are the gate dielectric thickness, the channel length and junction depth of MOSFET between year 1970 and 2008. It shows that MOSFET had gone through tremendous scaling.

Table 1.1: Comparison of the critical parameters of MOSFET between year 1970 and 2008. (Adapted from Osburn and Huff, 2002 and ITRS, 2007a).

Parameters	**1970**	**2008**
gate dielectric thickness, t_{ox}	50-100 nm	1.1-1.6 nm
channel length, L	7.5 μm	0.045 μm
junction depth	~1 μm	0.025 μm

Recently, non-classical CMOS structures had been introduced and proposed in the ITRS (2007a) as the current CMOS structure near the limit of scaling. Those are fully depleted SOI (FD-SOI) (Ohtou et al., 2007), FINFET (Vega and Liu, 2009), tri-gate (Irisawa et al., 2009) and vertical transistors. Among those new structures, VMOST structure is one of the promising devices to be the future CMOS.

1.2 Research background

The fundamental differences between lateral and vertical MOS transistor are shown in Fig.1.1. Fig. 1.1(a) is a silicon wafer. Fig. 1.1(b) shows the planar MOS transistor where both the current carrying plane and the current flows are parallel to the wafer surface. For VMOST, both the current carrying plane and the current flow

are perpendicular to the wafer surface as shown in Fig 1.1(c). From these points, it can be easily recognized either a MOS transistor is a planar or vertical MOSFET.

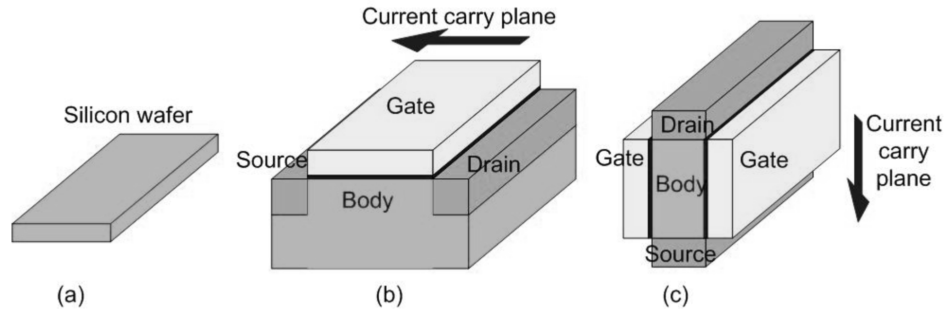


Fig. 1.1: Schematic view of planar and vertical MOSFET. (a) Silicon wafer. (b) Planar MOSFET. (c) Vertical MOSFET.

As the dimension of MOSFET becomes smaller and smaller, problems such as short-channel effects (SCEs), drain induced barrier lowering (DIBL) and hot electron effects starts to appear (Chen et al., 2002; Thompson et al., 1998 and Troutman, 1979). Fundamental scaling limits and main issue causing failure for conventional MOS devices are shown in Table 1.2.

Table 1.2: Fundamental scaling limits for conventional MOS devices and reasons. (Adapted from Thompson et al., 1998).

Feature	**Limit**	**Reason**
Oxide thickness	2.3 nm	Leakage (I_{GATE})
Junction depth	30 nm	Resistance (R_{SDE})
Channel doping	V_{th} = 0.25 V	Leakage (I_{OFF})
Souce/drain extension under diffusion	15 nm	Resistance (R_{INV})
Channel length	0.06 µm	Leakage (I_{OFF})
Gate length	0.10 µm	Leakage (I_{OFF})

Up to now, these limitations had been overcome with the introduction of source drain extension (SDE) (Wakabayashi et al., 2002), low-K dielectrics (Kikkawa, T., 2000), silicided contacts (Lee and Li, 2006) and silicon on insulator (SOI) structure (Cristoloveanu, S., 1997). Besides these, another critical step in fabrication process is lithography. In order to achieve sub-100nm, advanced lithography technology is needed to get a fine and consistent pattern.

With reference to ITRS (2007a), the channel length will be around 10 nm by the year 2020 and there are still many challenges and red brick wall needed to breakthrough. Thus, further scaling will require the introduction of new technologies which are new materials (Liu et al., 2001; Selvakumar and Hecht, 1991; Tezuka et al., 2007) and new transistor structures (Ohtou et al., 2007; Vega and Liu, 2009 and Irisawa et al., 2009) to overcome the challenges.

New transistor structures especially VMOST structures had gone through intensive research works. It is due to the three main advantages as described by Gili et al. (2003). Firstly, the channel length is defined by non-lithographic methods. Secondly, surround or double gate structures allow more channel width per unit area, which thus increase the drive current per unit area. Thirdly, the gate length is decoupled from packing density. Therefore, the layout requires less space than planar MOS transistors in some applications especially device that need long channel transistors. This was shown by Risch et al. (1996) and Risch et al. (1997) where the planar layout channel width is 8F and the area size is reduced more than a factor of

two for vertical layout. Note that F is the smaller dimension used in MOSFET layout design rules.

Up to date, VMOST structure is still new and limited in production lines compare to the mature planar MOSFET technologies. Still, a lot of research is needed to be done in order to replace planar MOSFET in future. Most of the reported works of VMOST in literature only fabricated one set parameters of the structures. With simulation, it consumes lesser time and cost to optimized the device parameters. For VMOST structures, there are still a lot of parameters that remains unclear and need to be optimized. Therefore, simulation is the best solutions to study the effects of those parameters.

1.3 The importance of TCAD modelling

Technology computer-aided design (TCAD) plays an important role in the development and optimization of technologies, devices and integrated circuits (ICs). According to Giles (2004), the complexity of a modern technology could not be successfully completed without extensive use of modelling tools in almost every aspect of its development. Furthermore, TCAD can also be used as an education tools (Parent and Del Rio-Parent, 2007).

The main reasons is that TCAD is one of the few enabling methodologies that can reduce development cycle times and costs (ITRS, 2007b). As we all know, to test varied new parameters of a device can be very costly and time consuming. In

addition, numerical simulation of semiconductor device fabrication and operation is important to the design and manufacture because it offers the feasibility to give insight into the relationships between processing choices and nanoscale devices that can not be obtained from physical metrology tools alone. Besides, TCAD is important for the step of the optimisation of devices or ICs. There are many parameters that can influence the performance of devices or ICs. Therefore, with the assists of TCAD, it could be optimized easily without repeating the fabrication for testing. Even though sometime the parameters proposed in TCAD do not function in real devices but the failure is low.

1.4 Research Objectives

The aims of this research are to simulate three types of NVMOST in 2-D structures:

1. Single gate VMOST growth with epitaxial layers (VMOST-EL) structures
2. Single channel length vertical MOSFET incorporating a dielectric pocket (DP) (DP-VMOST) structures
3. Double gates vertical replacement gate (VRG) MOSFET.

The short channel effects with various channel doping concentration, N_C, on those structures are discussed. Besides, spacing between the pocket and the gate oxide,

W_C, for DP-VMOST and the effects of the width of the body region between the two channels, W_B, for VRG MOSFET on various N_C are examined, respectively.

1.5 Originality of the research works

The originality of this research work lays in the study of few parameters for the three types of VMOST structures with 2-D simulator. For DP-MOSFET structure, it shows that as we varied the W_C, the outputs will also be altered. Therefore, it is possible to be used to vary the device outputs. Moreover, with different mobility models, it shows different trends of the off-state leakage current at channel doping concentration of 4 x 10^{18} cm^{-3}. For VRG-MOSFET structure, as the W_B decreases, the body region would become partially or fully depleted, which is in analogy with the thin double gate VMOST. From the results, it shows the possibility of tailoring the device outputs by varying the W_B.

1.6 Organization of dissertation

This dissertation is organized as follows:

In Chapter 2, selected vertical MOS transistors (VMOSTs) structures in literature are reviewed.

In Chapter 3, the theory of the MOSFET will be described. Moreover, the short channel effects (SCEs) of MOSFET will also be explained.

Chapter 4 is devoted to the explanation of simulation tools. The simulation programs are ATHENA, ATLAS and DEVEDIT from Silvaco International. Each of the programs will be illustrated.

In Chapter 5, the results and discussion of the three simulated VMOST structures, namely, VMOST-EL, VMOST incorporating dielectric pocket (DP) and VRG MOSFET, are discussed.

Finally, in Chapter 6, conclusion of this dissertation and recommendations for future research are given.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

In this chapter, present and selected VMOST structures will be reviewed. The VMOST structures are VMOST fabricated with ion implantation, VMOST growth with expitaxial layers (VMOST-EL), VMOST with fillet local oxidation (FILOX), Vertical MOSFET incorporating dielectric pocket (DP-VMOST), vertical replacement gate (VRG) MOSFET, double and surround gate vertical MOSFET.

2.2 Vertical MOSFET with ion implantation

This category of VMOST structures had been demonstrated by Zhou et al. (2005), Gili et al. (2006a), Josse et al. (2001), Gili et al. (2003a), Kunz et al. (2004), Schulz et al. (2000a), Schulz et al. (2000b), Schulz et al. (2001) and Chen et al. (2002). In this approach, the channel(s) is(are) formed on the sidewall of mesa etched while source/drain regions are formed by self-aligned ion implantation as shown in Fig 2.1. The channel length is depends on the depth of ion implantation junction. As

the dimension becomes smaller, the junction of source and drain also becomes smaller.

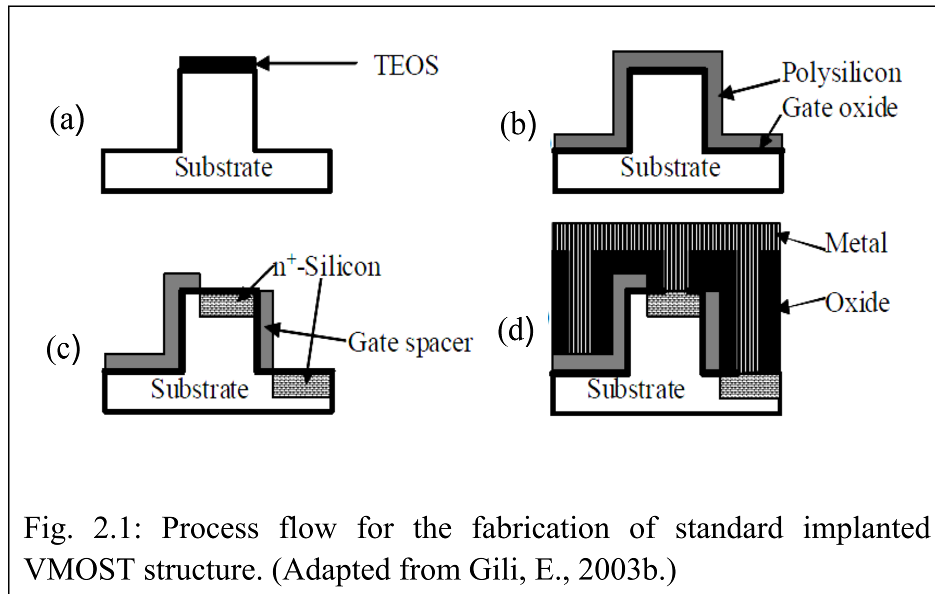
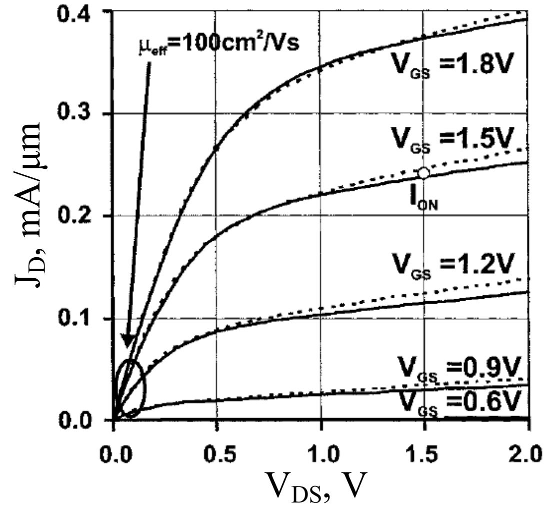


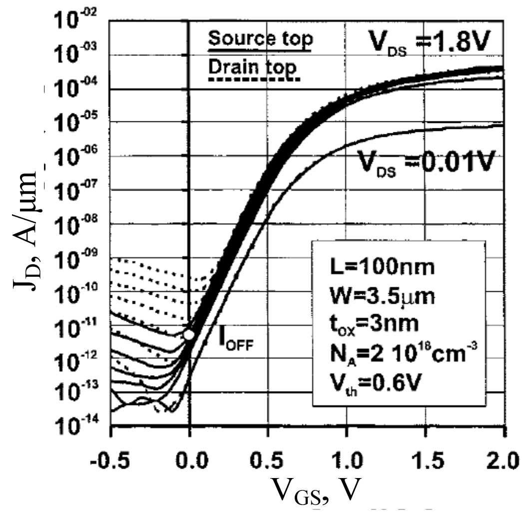
Fig. 2.1: Process flow for the fabrication of standard implanted VMOST structure. (Adapted from Gili, E., 2003b.)

According to Schulz et al. (2001), VMOST structure formed by ion implantation is CMOS compatible. An advantage of this process is the self-aligned source/drain regions by ion implantation. Through this method, the optimization of the direct current (DC) characteristics is difficult to achieve due to the one-dimensional doping profile of the channel length of VMOS (Behammer et al., 1998).

Fig. 2.2 shows the output and transfer characteristics of VMOST with ion implantation with channel length, L, of 100 nm, channel doping concentration, N_C, of 2 x 10^{18} cm^{-3} and gate oxide thickness, t_{ox}, of 3 nm. It is clearly showed that the results for drain on top (DOT) and source on top (SOT) are almost the same. Note that DOT is the drain contact on top pillar and the source contact on the etch side.



(a)



(b)

Fig. 2.2: (a) Output and (b) transfer characteristics for VMOST with ion implantation with channel length, L, of 100 nm, channel carrier concentration of 2 x 10^{18} cm^{-3} and gate oxide thickness of 3 nm. (Adapted from Schulz et al., 2001.)

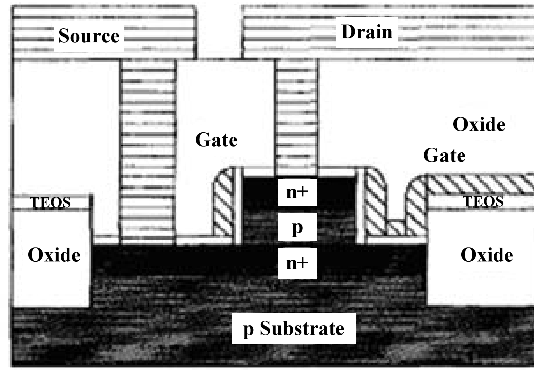
Meanwhile, SOT is the source contact on top pillar and the drain contact on the etch side. The threshold voltage, V_{th}, is 0.6 V with a low off-state leakage current density in two dimension, J_{off}, about 8 x 10^{-12} A/μm (defined at drain voltage, V_{DS} = 1 V) and drain current density in two dimension, J_D, of 120 μA/μm (defined at V_{GS} = 1.2 V). Low J_D is mostly due to the high V_{th} and also the rough sidewall of the mesa which

causes the mobility degradation. Moreover, the DIBL and subthreshold slope, S are 70 mV and 102 mV/dec, respectively.

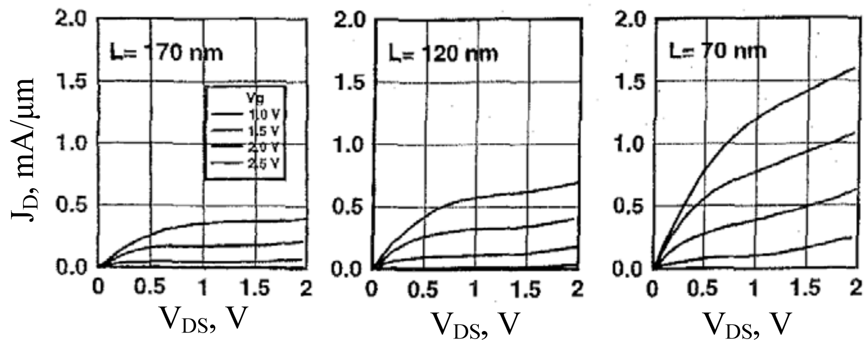
2.3 Vertical MOSFET with expitaxial layers

This category of devices had been demonstrated by Behammer et al. (1996), Klaes et al. (1998a) Klaes et al. (1998b), Risch et al. (1996), Schulz et al. (1998) and Moers et al. (1999). In this approach, the channel(s) is(are) formed by $n^+/p/n^+$ layers epitaxial growth and then mesa etched to form the channel region at sidewall. This shows that channel of VMOST is defined by growth layer. Instead of defining the source/drain regions using ion implantation, the doping profile is formed by in-situ doping during the epitaxial growth of $n^+/p/n^+$ layers. Basically, the epitaxial layers are grown using molecular beam epitaxial (MBE) (Gossner et al., 1995; Fink et al., 2002; Hansch et al., 1999;, Kaesen et al., 1998 and Fink et al., 2000) or chemical vapor deposition (CVD) (Behammer et al., 1996; Klaes et al, 1998a; Klaes et al., 1998b; Schulz et al., 1998 and Moers et al., 1999). The use of MBE allows very precise control of doping to investigate device physics associated with channel engineering. Therefore, it introduces a new way for control of doping profile especially with MBE that could be controlled very precisely, even at the atomic level. However, the epitaxial process is hardly CMOS compatible.

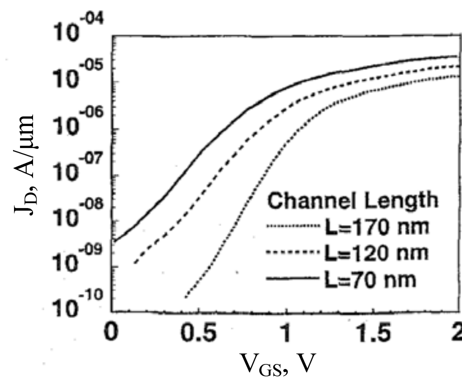
Fig. 2.3 shows the (a) schematic cross section of VMOST-EL; (b) Output and (c) transfer characteristics of (a) obtained by Risch et al. (1996). The VMOST-EL



(a)



(b)



(c)

Fig. 2.3: (a) Schematic cross section of VMOST-EL; (b) Output and (c) transfer characteristics of (a) obtained by Risch et al. (1996).

structures have channel lengths, L, of 170, 120 and 70 nm, with the channel doping concentration, N_C of 2 x 10^{18} cm^{-3}. Threshold voltage for L of 170, 120 and 70 nm at low drain voltage is 0.8, 0.6, 0.4 V, respectively. For L of 70 nm, saturation J_D of 0.5

mA/μm is obtained at gate voltage, V_{GS} = 1.5 V and drain voltage, V_{DS} = 1.5 V. According to Risch et al. (1996), the devices exhibit Kink effects due to the avalanche generation which charges the floating gate substrate more positively up to the onset of the parasitic bipolar transistor.

2.4 Vertical MOSFET with FILOX

The FILOX (Fillet Local Oxidation) process was demonstrated by Gili et al. (2003a), Gili et al. (2004a), Gili et al. (2004b), Kunz et al. (2004) and Tong (2004). The concept of introducing FILOX is to reduce the large overlapping capacitances between the gate and source/drain regions. Comparison between vertical MOSFET with and without FILOX is shown in Fig. 2.4. An oxide much thicker than gate oxide is grown on the top of source/drain regions. It is self-aligned to the pillar due to the nitride spacers.

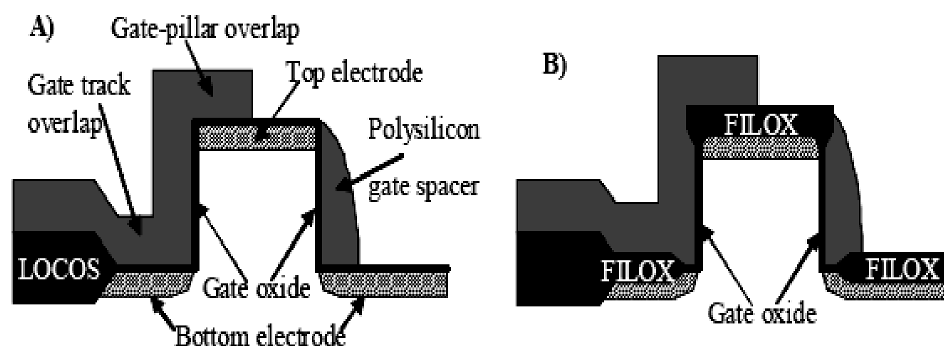


Fig. 2.4: Comparison between vertical MOSFETs structures: A) standard implanted, B) FILOX process. (Adapted from Gili, E., 2003b.)

These processes have the advantage that the FILOX oxidation is self-aligned to the pillar. The inherent overlapping capacitance between gate spacer and source/drain regions are decreasing as shown by Gili et al. (2004a). However, this process is hardly to be scaled due to the stress engendered by the nitride layer deposition on the pillar. Besides, the time for wet etch to remove the stress relief oxide without removing all the FILOX oxide is extremely hard to control with precision. Table 2.1 shows the results of the S, V_{th}, J_D for V_{GS}-V_t=1 V, J_{off} for V_{GS}=0 V for L of 125 nm with single gate, double gate and surround gate VMOST structures with FILOX. Due to the high V_{th}, the J_D of the devices is low.

Table 2.1: Measured parameters of typical transistors with estimated channel length of 125nm.(Adapted from Gili et al. 2004a.)

	z (µm)	**V_{DS} (V)**	**S (mV/dec)**	**V_{th} (V)**	**J_D (A/ µm)**	**J_{off} (A/ µm)**
Surround gate	24	0.025	107	1.36	6.13×10^{-6}	$< 10^{-14}$
Surround gate	24	1	109	1.20	7.68×10^{-5}	2.49×10^{-12}
Double gate	9	0.025	113	1.54	4.69×10^{-6}	$< 10^{-14}$
Double gate	9	1	111	1.44	7.20×10^{-5}	3.68×10^{-12}
Single gate	4.5	0.025	114	1.59	6.55×10^{-6}	$< 10^{-14}$
Single gate	4.5	1	117	1.11	8.22×10^{-5}	1.57×10^{-11}
(z = channel width, S = subthreshold slope, V_{th} = threshold voltage, J_D for V_{GS}-V_{th} =1 V, J_{off} for V_{GS} = 0 V)						

2.5 Vertical MOSFET incorporating dielectric pocket

The dielectric pocket (DP) concept was first proposed by Jurzak et al. (2000) and Jurczak et al. (2001) in conventional lateral MOSFET to suppress short channel effects (SCEs) and DIBL without increasing the channel doping. The DP was applied

in vertical MOSFET structure by Lamb et al. (2001), Donaghy et al. (2002), Donaghy et al. (2004), Jayanarayanan et al. (2006) and Gili et al. (2005). Fig. 2.5 shows the layout of vertical MOSFET incorporating dielectric pocket (DP-VMOST). The implication of DP in VMOST is considerably simpler compare to conventional lateral MOSFET. This is because the oxide pocket and the polysilicon drain of the device are deposited before dry mesa etched.

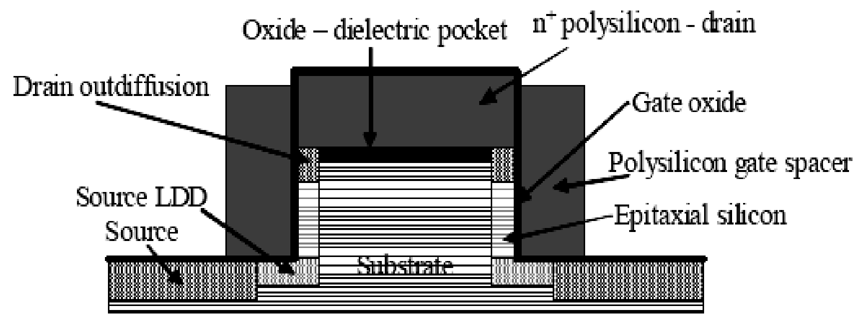


Fig. 2.5: Vertical MOS transistor with dielectric pocket. (Adapted from Gili, 2003b.)

The idea of DP is to allow a low doped channel region and thus a low threshold voltage. In realizing short channel VMOST, the high body doping is necessary to prevent SCEs and punch through. However, as the body doping increases, the mobility of electron will decrease. Moreover, the dielectric pocket blocks the out-diffusion of impurities from the drain in the body of the device and reduces the leakage current path existing in the middle of the body in standard structure. The main difficulty is the growth of a uniform epitaxial silicon layer on

silicon pillars. This could also prevent the scalability of this process to very thin pillars in order to obtain fully depleted devices.

For DP-VMOST, there are two main parameters that varied the device outputs. These two parameters are the body doping concentration and spacing between pocket and gate oxide. Fig. 2.6 shows the threshold voltage and off-state leakage current versus body doping concentration for 50nm VMOSTs with and without dielectric pocket obtained with ISE TCAD. In Fig. 2.6, it shows that VMOST with dielectric pocket improved the off-state leakage current and threshold voltage.

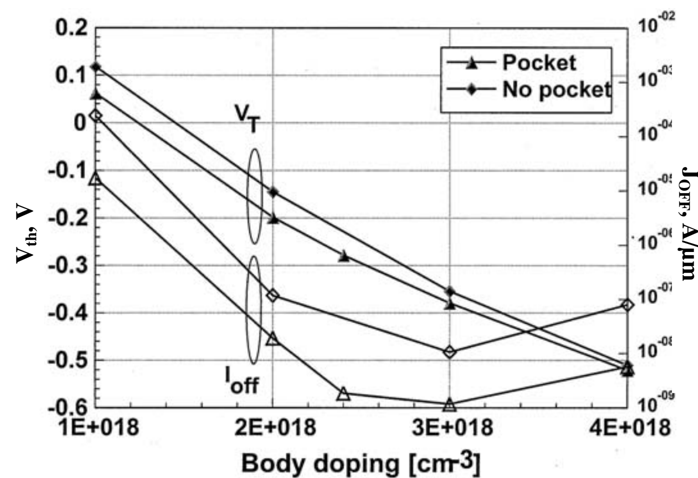
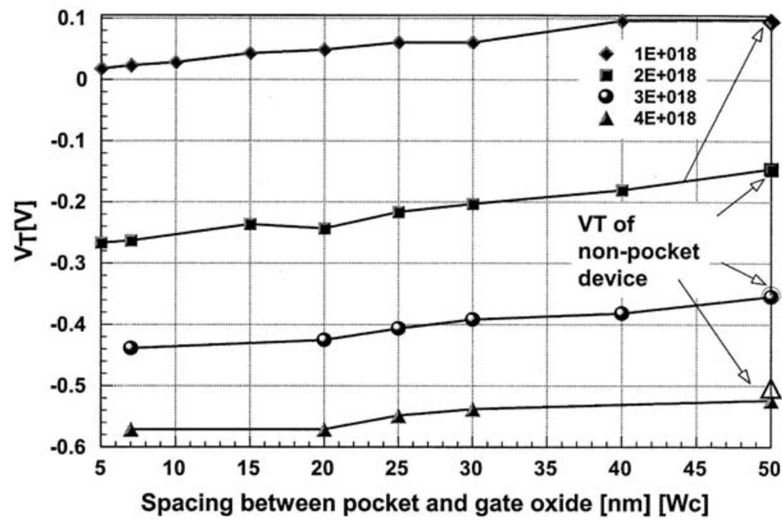


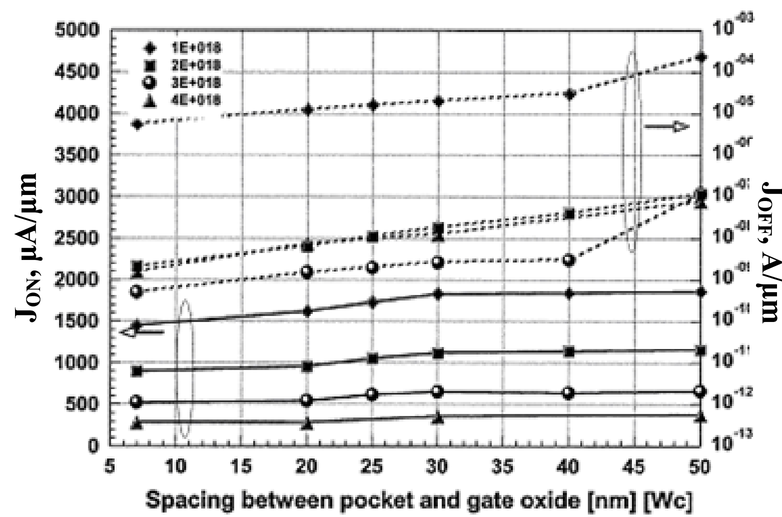
Fig. 2.6: Threshold voltage and off-state leakage current density in 2-D versus body doping for 50nm VMOSTs with and without dielectric pocket. (Adapted from Donaghy et al., 2004.)

The effects of the spacing between pocket and gate oxide on the threshold voltage, on-state drain current and off-state drain current are shown in Fig. 2.7. From Fig 2.7(a), it shows that the threshold voltage is decreased as the spacing between

pocket and gate oxide is increased until the same value with non-pocket device at 50nm. However, as the spacing between pocket and gate oxide is increased, both of the on-state drain current and off-state drain current also increased.



(a)



(b)

Fig. 2.7: Result for a p-channel VMOST with channel length 50nm, channel width 1μm, body doping varied from 1 x 10^{18} to 4 x 10^{18} cm^{-3} and drain voltage -1.0V (a) Effect of the spacing between pocket and gate oxide on the threshold voltage. (b) Effect of the spacing between pocket and gate oxide on J_{on} and J_{off}. (Adapted from Donaghy et al., 2004.)

2.6 Vertical replacement gate (VRG) MOSFET

The vertical replacement gate (VRG) MOSFET had been shown by Hergenrother et al. (1999), Hergenrother et al. (2001), Hergenrother et al. (2002), Oh et al. (2000) and Oh S.-H.(2001). The process to fabricate a vertical replacement gate MOSFET is extremely complex as shown in Fig. 2.8.

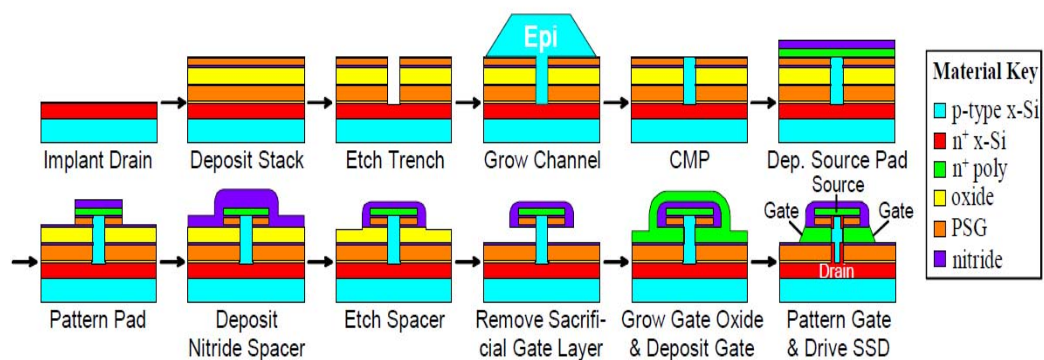


Fig. 2.8: Schematic of the vertical replacement gate (VRG) MOSFET front end process flow. (Adapted from Hergenrother et al., 1999.)

As in Fig. 2.8, after the deposition of oxide, PSG, nitride, oxide, nitride, PSG and nitride, then only etch to form the sidewall for the channel. Furthermore, PSG layers are used as solid source diffusion (SSD) to form self-aligned source/drain extensions.

However, there are a few unique advantages that are very attractive compared to other MOSFET structures. Those are (1) all critical transistor dimensions are controlled precisely without applying lithography and dry etch, (2) the gate length is defined by a deposited film thickness, independently of lithography and etch, and (3)

a high quality gate oxide is grown on a single crystal silicon channel. Besides the unique advantages, the vertical replacement gate MOSFET includes a self-aligned source/drain formed by solid source diffusion and small parasitic overlap, junction and source/drain capacitance. In addition, VRG MOSFET with double gate will produce larger drive current compared to single gate MOSFET structures.

Fig. 2.9 shows the (a) subthreshold and (b) J_D-V_{DS} characteristics for a VRG nMOSFET with L_G = 50 nm, t_{OX} = 28 Å and $N_A = 3.5 \times 10^{18}$ cm^{-3} at 1.5 V operation. The subthreshold is characterised with J_{off} = 13 nA/µm, DIBL = 90 mV and S = 105 mV/dec. However, due to the high channel doping concentration of $3.5 \times 10^{18} cm^{-3}$, the threshold voltage is V_{th} = 0.73 V. Both the high V_{th} and reduced surface mobility cause the low drive current density of the 50 nm VRG-nMOSFET that is 180µA/µm (at V_{GS} = 1.8 V) compared to 280µA/µm for channel length 100nm.

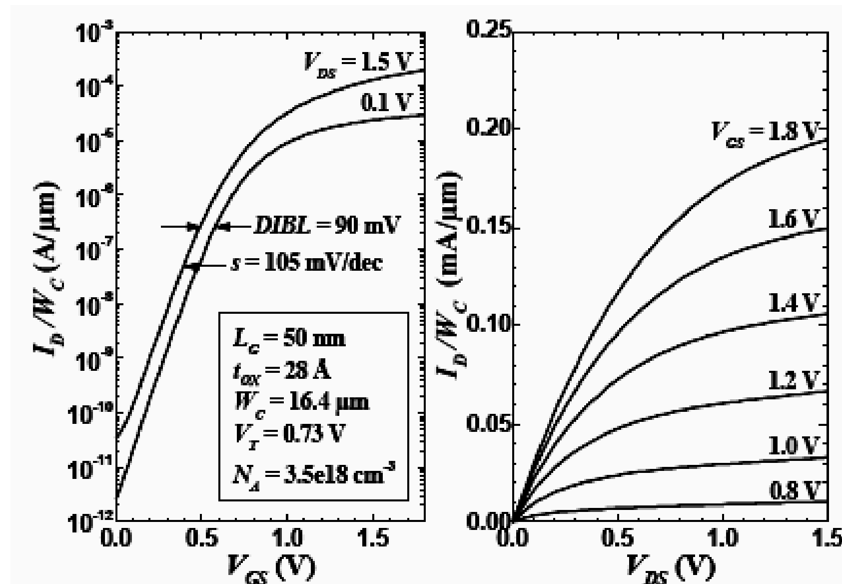


Fig. 2.9: Subthreshold and J_D-V_{DS} characteristics of a channel length 50nm VRG-nMOSFET. (Adapted from Hergenrother et al., 1999.)

2.7 Double and surround gate vertical MOSFET

The double and surround gate vertical MOSFET had been shown by Goebel et al. (2002), Zheng et al. (1998), Li et al. (2001), Takato et al. (1991), Jayanarayanan (2004), Hakim et al. (2006), Masahara et al. (2003) and Moers (2007). Fig. 2.10 shows the sketch of the double or surround gate VMOST. For the double and surround gate VMOST, it not only increases drive current per unit area but also has the possibility of realizing fully depleted and partial depleted devices without the need of SOI substrates. If the body pillar or ridge is narrow enough (about 30-70nm, depending on the body doping concentration), the depletion regions merge in the middle of the body (Jayanarayanan, 2004). Thus, it can suppress floating body effect for fully depleted devices and short channel effects.

One of the challenging process steps is the definition of very thin pillars or ridges. Even it can be done by direct write using electron beam lithography but this solution has low throughput. Besides, it is difficult to fabricate thin-pillar double and surround gate vertical MOSFETs with the electrode on the top of the pillar. In fact it is impossible to align a contact mask to the pillar due to its small dimensions. (Gili, 2004)

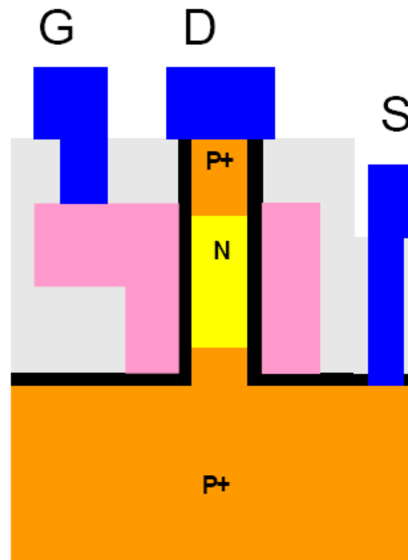


Fig. 2.10: Sketch of the double or surround gate VMOST. (Adapted from Jayanarayanan, 2004.)

2.8 Summary

In this chapter, the selected VMOST structures are reviewed. All of the structures are revised and some of the results are shown. It shows that a lot of works have been done on VMOST structures.

CHAPTER 3

THEORY OF MOSFET

3.1 Introduction

In this chapter, the principles theory of metal oxide semiconductor field effect transistor (MOSFET) will be discussed and only NMOSFET is to be considered. Basic principle of planar MOSFET operation will be described as it is similar to vertical MOSFET. It is followed by the short-channel effects (SCEs) of the MOSFET.

3.2 Basics principles of MOSFET operation

Fig. 3.1 shows the structure of an NMOSFET and the band diagram along the channel. The region under the oxide between the source and drain is referred to as the channel region. As shown in Fig 3.1, the n^+ drain and source are separated with p-type silicon. Thus, no current flows from drain to source in the channel region. This can be explained using the equilibrium band diagram along the channel. Electrons can not flow from source to drain due to the existence of the potential barrier.

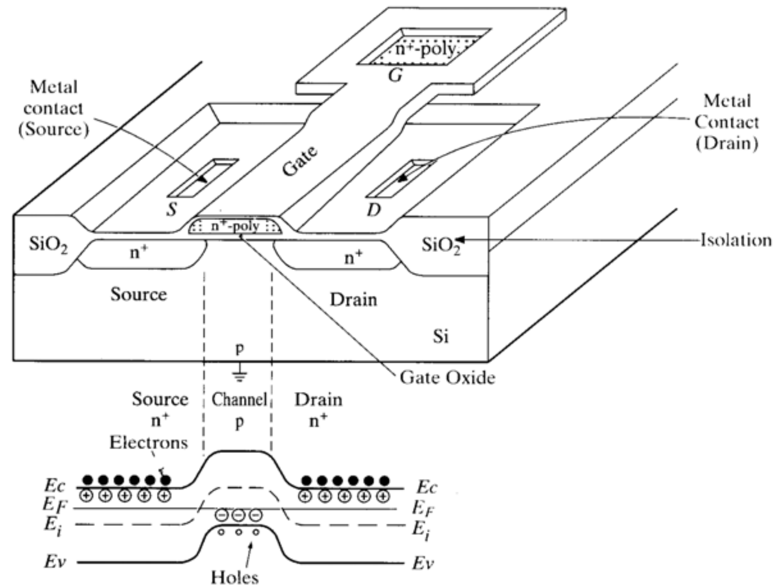


Fig. 3.1: Structure of an NMOSFET. Isometric view of device and equilibrium band diagram along channel. (Adapted from Streetman and Banerjee, 2000)

When a positive voltage is applied to the gate, a vertical electric field is induced in the oxide. This electrical field also penetrates the semiconductor, where electrons will be attracted below the oxide and hole will be repelled. Once the positive voltage is strong enough, an inversion layer will be created beneath the gate oxide. This inversion layer forms the channel that allows electrons to flow from source to drain. As the p-type channel region becomes n-type, the valance band moves down and far away from the Fermi level. The potential barrier for electrons between the source, channel and drain is decreased. Therefore, electrons can flow from source to drain. A change in the gate voltage alters the channel conductance and device current.

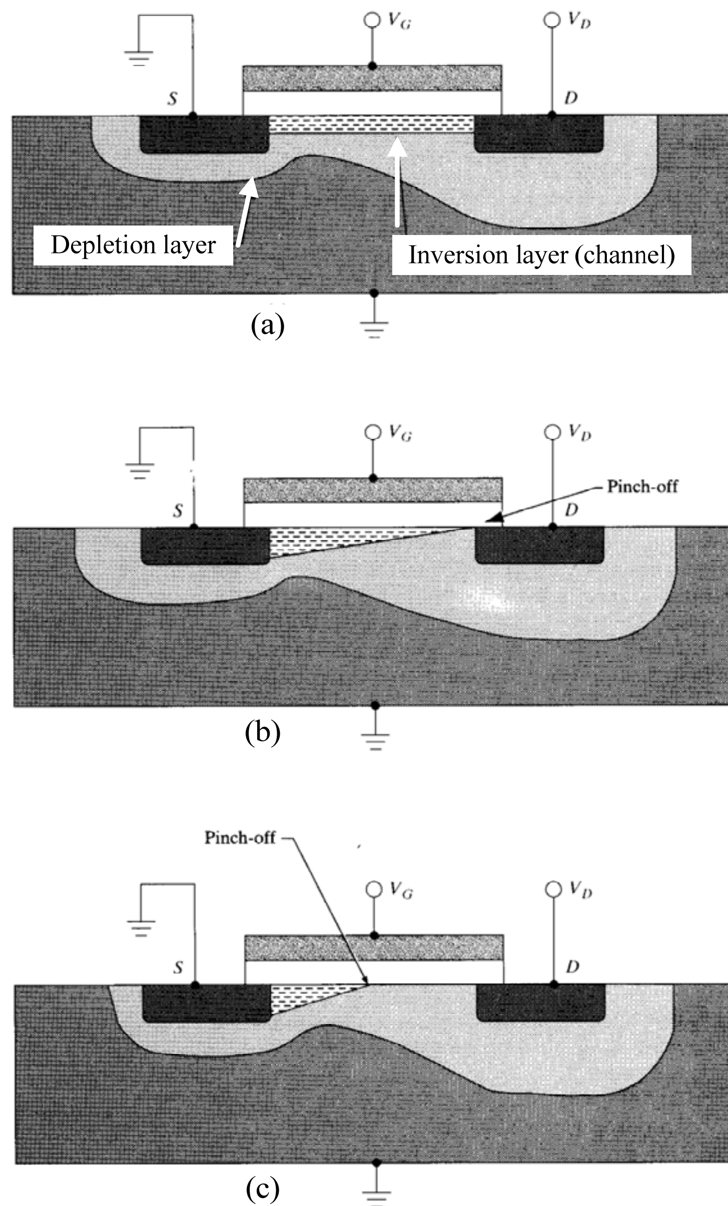


Fig. 3.2: Cross section of an n-channel MOSFET and I_D versus V_{DS} curve when $V_{GS} > V_{th}$ for (a) a small V_{DS} value, (b) a value of $V_{DS} = V_{DS}(sat)$ and (c) a value of $V_{DS} > V_{DS}(sat)$. (Adapted from Streetman and Banerjee, 2000)

The operation of an n-channel MOSFET can be separated into three different modes, depending on the voltages at the terminals as shown in Fig. 3.2. First, it is a linear region mode (Fig. 3.2(a)) where $V_{GS} > V_{th}$ and $V_{DS} < (V_{GS} - V_{th})$. When the