ANODIZATION OF ZIRCONIUM FOR THE FORMATION OF HIGH-K DIELECTRIC ZIRCONIA (ZrO_2) THIN FILM

BY

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I declare that the content presented in this thesis is the results of my own work which was done in Universiti Sains Malaysia unless informed otherwise. The thesis has not been previously submitted for any other degree.

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Noor Rehan Binti Zainal Abidin

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LIST OF ABREVIATIONS AND SYMBOLS

A	Area of the film (cm^2)
At%	Atomic percent
C	Capacitance
c	Cubic
d	thickness
DI	Deionize water
ε_o	Permittivity
h	hexagonal
I	Current (A)
ITRS	International Technology Roadmap of Semiconductor
J	Current density (A/cm^2)
k	Dielectric constant
m	monoclinic
MOS	Metal-oxide-semiconductor
OCP	Open circuit potential
θ	Angle or theta
PDM	Point defect model
rms	Root mean square
t	Anodization time/ tetragonal
V	Voltage
V_b	Breakdown voltage

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PENGANODAN ZIRKONIUM UNTUK PEMBENTUKAN LAPISAN NIPIS ZIRKONIA (ZrO_2) BERPEMALAR DIELEKTRIK TINGGI

ABSTRAK

Zirkonia (ZrO_2) merupakan bahan yang berpotensi di dalam aplikasi get dielektrik untuk masa hadapan. Dengan pengecilan ketebalan get dielektrik (<1.4nm), silikon dioksida (SiO_2) mengalami masalah kebocoran arus disebabkan oleh nilai pemalar dielektriknya yang rendah (k=3.9). ZrO_2 mempunyai potensi untuk menghalang masalah arus bocor kerana nilai pemalar dielektriknya yang tinggi (k=25) serta kestabilan termanya yang baik di atas substrat silikon (Si). Objektif utama kajian ini adalah untuk menghasilkan lapisan nipis ZrO_2 yang mepunyai sifat-sifat yang baik dan sesuai dengan aplikasi get dielektrik. Lapisan nipis ZrO_2 ini telah dihasilkan dengan menganodasikan lapisan nipis zirkonium (Zr) yang telah dipercitkan di atas substrate Si jenis-n. Selain daripada filem nipis, penganodan kepingan Zr turut dilakukan sebagai perbandingan kepada filem nipis. Proses penganodan dilakukan di dalam larutan beralkali sodium hidroksida (NaOH). Tiga parameter utama yang dikaji di dalam kajian ini adalah kesan perubahan voltan, perbezaan larutan yang digunakan dan juga masa ke atas lapisan nipis ZrO_2 yang terhasil. Berbanding dengan parameter yang lain, voltan didapati memberikan kesan yang besar ke atas sifat-sifat filem nipis ZrO_2 yang terhasil terutamanya pada fasa-fasa ZrO_2. Fasa-fasa ZrO_2 turut bertukar daripada fasa tetragonal atau kubik kepada fasa monoklinik pada voltan yang tinggi (>20 V). Ketebalan oksida yang terhasil didapati meningkat dengan peningkatan voltan setelah diukur menggunakan Filmetrik. Sifat elektrik bagi filem nipis ZrO_2 yang terhasil menunjukkan sampel yang dianodasi menjadi lebih berpenebat dengan peningkatan voltan. Sampel yang dianodasi pada voltan 40 V dan 50 V tidak menunjukan sebarang voltan runtuh. Ini menunjukan SiO_2 terbentuk pada voltan tinggi. Daripada kajian yang dilakukan, di dapati bahawa lapisan nipis yang dianodasikan pada voltan 20 V selama 30 minit di dalam larutan berkepatan 1 M NaOH mempunyai sifat-sifat yang baik dan sesuai bagi aplikasi get dielektrik. Ini menunjukkan bahawa lapisan nipis ZrO_2 dapat dihasilkan pada suhu bilik dengan menggunakan kaedah yang mudah, ringkas dan murah dengan sifat yang setanding dengan kaedah-kaedah yang lain.

ANODIZATION OF ZIRCONIUM FOR THE FORMATION OF HIGH-K DIELECTRIC ZIRCONIA (ZrO_2) THIN FILM

ABSTRACT

Zirconia (ZrO_2) is a promising material for future high-k gate dielectric applications. With the decreasing of the get dielectric thickness (<1.4nm), silicon dioxide (SiO_2) layer suffered from basic problem of high tunneling leakage current due to its low dielectric constant (k=3.9). ZrO_2 has a potential to overcome the tunneling leakage current problem since it has a high dielectric current (k=25) and good thermal stability on silicon (Si) substrate. The main objective of this work is to produce ZrO_2 thin film with good properties and suitable for get dielectric application. ZrO_2 thin film has been produced by anodizing zirconium (Zr) thin film sputtered on n-type Si substrate. Besides the thin film, anodization on Zr foil was also done as a comparison to the thin film. Anodization was done in alkaline solution of sodium hydroxide (NaOH). In this work, three mains parameters were studied; effects of different voltage, different concentration of solution and anodization time on the ZrO_2 thin film. Compared to other parameters, voltage was found to give a significant impact on the properties of the formed ZrO_2 thin film especially on the ZrO_2 phases. ZrO_2 phases transformed from tetragonal or cubic phase to monoclinic ZrO_2 at high voltage. Thickness of the oxide formed was found to increase with voltage as measured using Filmetric. Electrical properties of the formed ZrO_2 thin film show that the anodized samples became more insulated as the voltage increased with no breakdown voltage for samples anodized at 40 V and 50 V. This indicates that SiO_2 forms at higher voltage. From this work, thin film that has been anodized at 20 V for 30 minutes in 1 M NaOH posses a good properties and suitable for get dielectric application. This show that ZrO_2 thin film can be produced at room temperature using simple, easy and cheap techniques with comparable properties compared to other techniques.

CHAPTER 1

INTRODUCTION

1.1 Preface

Gate dielectric is one of the most vital components in metal-oxide-semiconductor (MOS) device that functions as an insulating layer to prevent current leakage from the gate into the channel. Since 1960 silicon dioxide (SiO_2) has been used almost exclusively as a primary gate dielectric material in MOS device due to its remarkable physical, electrical and interface properties in direct contact with silicon (Si) substrates (Kyu et al., 2005). In addition, SiO_2 possesses a good loss factor, excellent thermal stability at typical Si process temperature and easy physical processing (Armelao et al., 2005). Unfortunately, aggressive scaling down activity tends to cause an increase in gate leakage current. The resulting gate leakage current increases the power dissipation which leads to the undesired power consumption in MOS device and degrades the device performance. As a consequence of this issue, employing SiO_2 as gate dielectric material in MOS technology tends to be a difficult task. Therefore, many researchers and manufacturers are extensively investigating alternative materials to replace SiO_2 as a gate dielectric to reduce gate leakage current. High dielectric constant (high-*k*) materials have received considerable attention to overcome the problems associated with the extremely thin conventional SiO_2 gate dielectric. High-*k* materials may circumvent this problem since they can

provide physically thicker dielectric films to reduce leakage current so that smaller and faster devices can be manufactured (Houssa, 2004).

HfO_2 (Bennett et al., 2006), Ta_2O_5 (Atanasova et al., 2003), ZrO_2 (Jang et al., 2003), CeO_2 (Galata et al., 2007), Gd_2O_3 (Hsieh et al., 2006), La_2O_3 (Vellianitis et al., 2004) and Al_2O_3 (Hwu et al., 2005) are among the high-*k* materials that are currently under intense investigation. The candidate materials should satisfy challenging requirements as discussed in more detail in Chapter 2, such as high dielectric constant, good oxide-semiconductor interface, and thermal stability contact with Si. Among them ZrO_2 has been proposed for study in this research due to its remarkable properties for microelectronics applications, such as wide band gap of 5.16 – 7.1 eV which could result in high barrier height for tunneling and hence reduces the leakage current. It has a dielectric constant in the range of 15–22, which is high enough to achieve lower equivalent oxide thickness (EOT). Unlike TiO_2 and Ta_2O_5, ZrO_2 possess good thermal stability when in contact with Si. This makes ZrO_2 a good material that can be used in deep submicrometer MOS devices (Ray et al., 2006; Wallace et al., 2005; Wilk et al., 2001; Wong et al., 2006).

In addition to the material properties, processing techniques also give crucial impact on the gate oxide. Various techniques have been applied to fabricate ZrO_2 including physical deposition processes, such as thermal oxidation (He et al., 2005; Lyapin et al., 2005), pulsed laser deposition (PLD) (Filipescu et al., 2007; Wang et al., 2001) and sputtering using metal or oxide targets (Chen et al., 2007; Jeong et al., 2005; Kim et al., 2006; Sun et al., 2000) and chemical deposition processes, such as sol-gel (Armelao et al., 2005), molecular beam evaporation (Hong et al., 2003), chemical

vapor deposition (CVD) (Mays et al., 2004; Yu et al., 2003), atomic layer chemical vapor deposition (ALCVD) (Ferrari et al., 2002; Houssa, 2004; Rana et al., 2003), rapid thermal CVD (Chang et al., 2001) and spray pyrolisis (Garcia et al., 2004; Ortiz et al., 2005). In this research anodization has been proposed to be used as a technique in producing ZrO_2 thin film on Zirconium (Zr) film deposited on Silicon (Si) due to some advantages. By using this technique, the thickness and morphology of the films can be controlled by varying the parameters such as electrolyte and formation voltage. This technique also allows us to deposit a relatively uniform and smooth film surface even on complex shapes of substrate which is a very important requirement needed for very thin gate oxide (Ming et al., 1996). In addition, this technique is a low cost process compared to other techniques which need a relatively high-temperature heat treatment and expensive equipment (Li et al., 2006). The formation of ZrO_2 thin film by anodization on Zr foil has been studied previously for numerous applications especially as a protective coating (Habazaki et al., 2003). There is also a publication on the formation of anodic oxide of ZrO_2 on alumina (Al_2O_3) substrate (Shimizu et al., 1997). However, to the best of our knowledge, there is no publication on the formation of anodic oxide of ZrO_2 on Zr thin film deposited on Si to be used as dielectric compounds in MOS devices. Therefore, it is of interest to study the capability of the process in the formation of ZrO_2 thin film with properties suitable for gate oxide in MOS devices. Hence, in this research, our intention is to produce ZrO_2 high-*k* dielectric material through the study of various altered parameters by using the anodization technique.

1.2 Problem statement

ZrO_2 are known as one of the potential candidates to replace SiO_2 as a good material used as get dielectric in MOS device applications. There is a lot of research works had been done previously in order to form ZrO_2 thin film with a good properties using variety of formation techniques such as sputtering, PVD, CVD, spray pyrolysis and MBE. Apart from that, anodization process has been considered in this work as one of the alternative technique to form ZrO_2 thin film.

Anodization offer several advantages compared to other techniques. By using this technique, ZrO_2 can be form using simple instrument at room temperature. It is a low cost process compared to other techniques which need a relatively high-temperature heat treatment and expensive equipment (Li et al., 2006). A lot of reports had been published in anodization of bulk Zr to form ZrO_2 nanotubes however there is no report on anodization of Zr thin film sputtered on n-type substrate to form ZrO_2 thin film. Therefore, this is the challenge in this work in order to study the best condition to form ZrO_2 thin film using this technique. By referring to the reports of anodization of bulk Zr, a details study on formation of ZrO_2 thin film on Si substrates have to be carried out in order to obtain a good properties comparable with other methods.

1.3 Objectives of the research

The main objective of this research study is to form ZrO_2 thin film by anodizing Zr thin film sputtered on n-type Si substrate. In order to produce ZrO_2 thin film with good properties that suitable for get dielectric application. In order to achieve the main objective, several approaches have been use which is:

a) Anodizing Zr thin layer sputtered on Si substrate using anodization process under several different conditions.
b) Study the effect of different parameters (thickness, voltage, concentration and time of oxidation) in the formation of ZrO_2.
c) Propose a mechanism of formation of ZrO_2 thin films form by anodization process.

1.4 Approach of the research

In this research, ZrO_2 was formed by depositing Zr on Si substrate by sputtering process. This film was then anodized in aqueous electrolyte solution (NaOH) to form ZrO_2. A number of different parameters was studied in order to identify the effect of each parameter to the oxide formed including the thickness of the sputtered sample, formation voltage, concentration of the solution and post deposition annealing. All the samples were then characterized and analyzed to study the optical, physical and electrical properties of the oxide formed. The overall experiment parameters are stated in Chapter 3.

1.5 Dissertation structure

This dissertation is organized into 5 chapters as follows. Chapter 1 gives a general introduction to the current issues occurring in microelectronic industry associated to the research work. Problem statement, objectives, scope and approach of the research are also identified in this chapter. Chapter 2 generally presents a literature review covering vital information of ZrO_2 as a high dielectric constant material, the background and theory of anodization process and also addresses current and past researches that had been carried out worldwide. Chapter 3 comprises of the whole

experiment starting from the raw materials, sample preparation, design of experiment and also the characterization technique used to analyze the samples. Chapter 4 shows the interpretation of the research results and some discussions have been described for better understanding. Lastly, Chapter 5 summarizes the accomplishments in this dissertation and recommendation for future work.

CHAPTER 2

LITERATURE REVIEW

2.1 Metal-Oxide-Semiconductor (MOS) device

Metal-oxide-semiconductor (MOS) device or commonly referred as MOS capacitor is the most important component in metal-oxide-semiconductor field-effect-transistor (MOSFET). MOSFET is a type of semiconductor transistor widely used in advanced integrated circuit (IC). MOSFET is used because it can be scaled down to smaller dimensions than other type of devices hence miniaturization is possible (Sze, 2002). Therefore, an understanding of the behavior of MOS capacitor is important in order to understand the principal operation of MOSFET.

Figure 2.1 is a cross-section of the MOS capacitor. A MOS capacitor consists of a metal, an oxide, and a semiconductor layer. The semiconductor layer is usually in the form of a single-crystal Si substrate. This semiconductor layer's function is to perform transistor action. The main purpose of the oxide layer is to insulate the semiconductor layer from the metal layer. The oxide layer is usually made from SiO_2. The metal layer is employed as contact for supplying voltage inputs to the MOS capacitor. It is also referred as the gate terminal and is made from aluminum or poly-silicon material (Neamen, 2003).

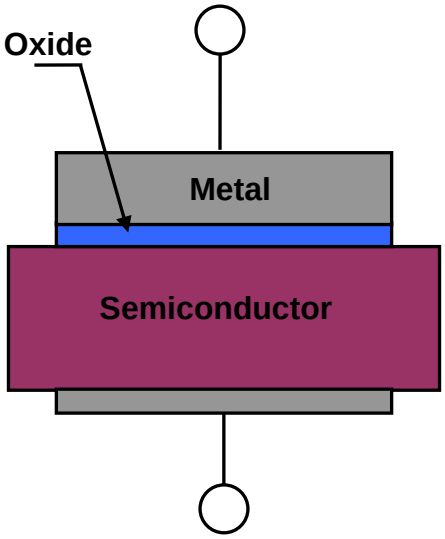


Figure 2.1: Schematic cross-section of MOS structure (Adapted from Neamen, (2003)).

The MOS capacitor functions as a device that can store electric charge. Therefore, it is most essential to understand the main feature of the MOS capacitor which is its changing capacitance with the applied voltage. Consequently, four modes of operation of the MOS capacitor need understanding (Taur et al., 2005). Depending on the applied voltage, they are named; (1) flat band, (2) accumulation, (3) depletion, and (4) inversion. In considering p-type semiconductor, all modes of operation can be defined as below:

(1) Flat band

The term flat band is given because the energy band diagram of the semiconductor is flat, which implies that no charge exists in the semiconductor making it an ideal capacitor. In this condition, the holes concentration is in equilibrium throughout the semiconductor because no field or charge is present. Cross-section and energy band diagram of the ideal MOS capacitor with $V_g = 0$ is shown in Figure 2.2. Since no current flows in the structure, the Fermi level remains constant in the semiconductor.

(2) Accumulation

Accumulation occurs when a negative voltage is applied between the gate and the semiconductor. When a negative voltage is applied to the gate, it creates an electric field in the oxide. The negative charge on the gate attracts holes from the substrate to the oxide-semiconductor interface as shown in Figure 2.2. Because of the low hole concentration in Si, the top of the valence bends upward and towards the oxide interface as shown in Figure 2.2. Due to the band bending, the Fermi level (E_f) at the surface is much closer to the valence band than is the Fermi level in the bulk Si. This results in a hole concentration much higher at the surface than in the bulk. Since that the excess holes are accumulated at the Si surface, it is therefore referred to as accumulation condition.

(3) Depletion

Depletion occurs when a positive voltage is applied to the gate. The positive charge on the gate repels the mobile hole from the semiconductor surface and makes the metal Fermi level move downward. The valence band at the surface is now farther away from the Fermi level and the hole concentration is lower at the surface than in the bulk. Therefore, the semiconductor is depleted of mobile carriers (hole) at the interface which acts as a dielectric because it can no longer contain or conduct charges. In effect, it becomes an insulator.

(4) Inversion

Inversion occurs when the applied voltage is beyond the threshold voltage. The positive gate voltage generates electron-hole pairs and attracts electrons towards the

gate. Since the oxide is a good insulator, these electrons accumulate at the substrate-oxide interface. The bands at the semiconductor bend more strongly resulting in a wider depletion region and more depletion charge. At a sufficiently high voltage, the intrinsic potential (E_i) can be below E_f indicating large concentration of electrons in the conduction band and the surface is depleted of holes.

Figure 2.2 shows a cross-section and an energy diagram of mode operation of MOS capacitor under different applied voltages for p-type semiconductor. Similar condition occurs in n-type semiconductor except that the polarities of voltage and band bending are reversed. Moreover, the roles of electrons and holes are interchanged.

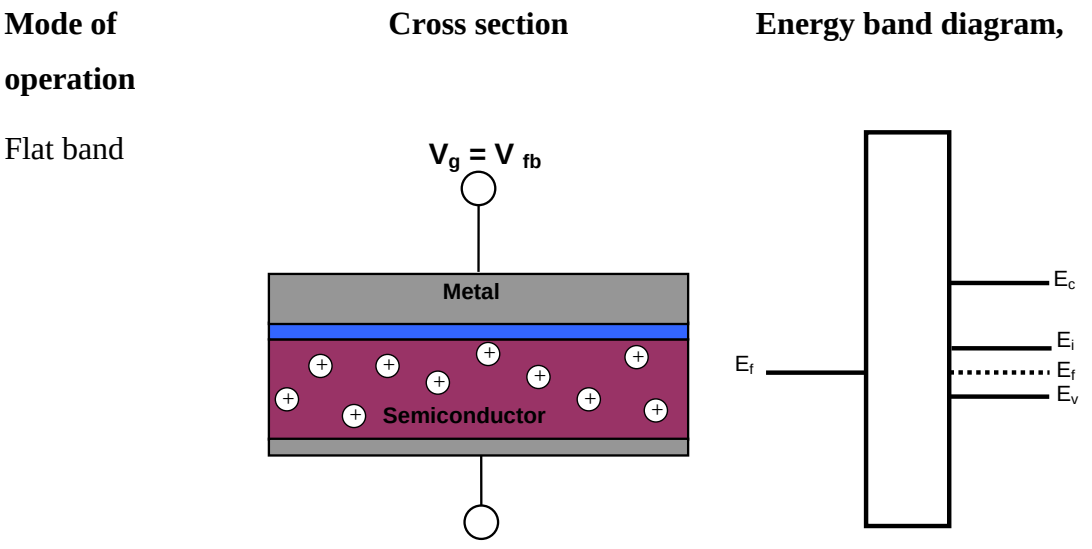


Figure 2.2: Cross-section and band diagram of different mode operations for p-type MOS capacitor (Adapted from Neamen, (2003) and Taur et al., (2005)).

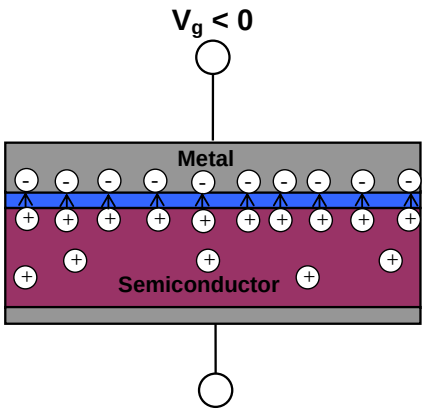
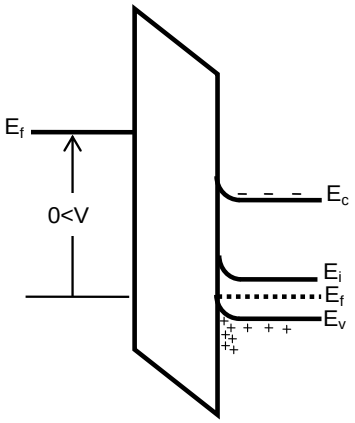
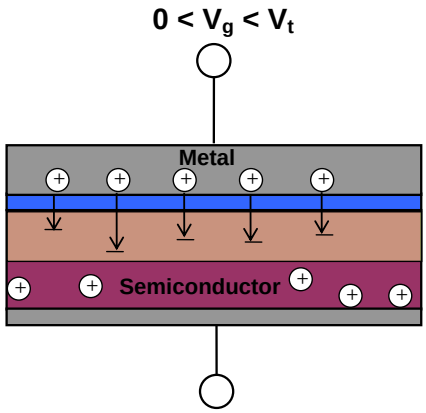
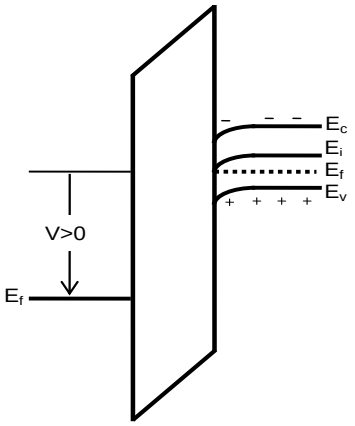
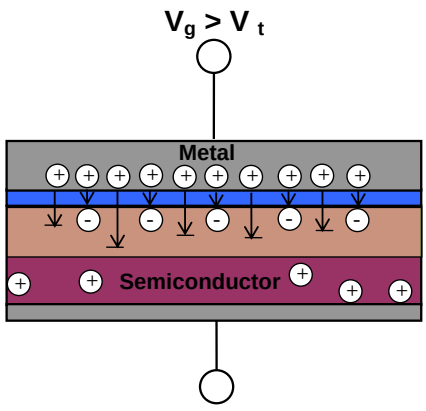
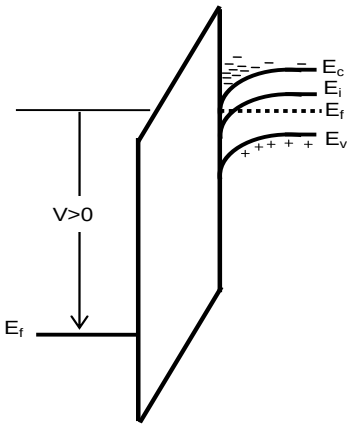
Mode of operation	Cross section	Energy band diagram,
Accumulation		
Depletion		
Inversion		

Figure 2.2 (continue): Cross-section and band diagram of different mode operations for p-type MOS capacitor (Adapted from Neamen, (2003) and Taur et al., (2005)).

2.2 Properties and limits of SiO_2 as a gate dielectric

As mentioned, SiO_2 has been used as a gate dielectric material in MOS capacitor. For more than 40 years due to its suitable physical and electrical properties. It has good interface properties on the Si substrate. Furthermore SiO_2 possesses several advantages such as; it can be grown thermally on Si substrate in an amorphous phase which is desirable to reduce charge leakage. It also has a high melting point, hence giving it an excellent thermal and chemical stability. SiO_2 could remain in an amorphous state at working condition. SiO_2 has a dielectric constant of 3.9. Moreover, the very large bandgap,E_g value of 9 eV makes SiO_2 an excellent electrical insulator for the gate oxide in a MOSFET (Degraeve et al., 2002).

However, SiO_2 major problem is high leakage current when made too thin due to direct tunneling of electrons through the thin SiO_2 layer. Decreasing the dimensions of the devices has become a subject of interest in semiconductor industry since a few years ago. Continuous efforts have been made to increase the number of devices on the same chip area. The aim of reducing the device size is to enhance functionality and performance of the devices at a lower cost. With a small size, more devices can be implemented in a small area of the Si substrate hence reducing the amount of power consumption. As devices become smaller, the higher operation speed can be achieved because of the decrease in the carrying, from source to drain (Wilk et al., 2001).

However, as the size of the MOS capacitor is made smaller, the thickness of the gate dielectric also decreases. The decreasing trend of the oxide thickness as proposed by International Roadmap of Semiconductor (ITRS) (ITRS, 2001, ITRS, 2004) is shown

in Figure 2.3. As seen, the gate dielectric needs to be approximately below 1.0 nm for sub 100 nm in year 2012. Unfortunately, this thickness will give SiO_2 a high leakage current problem, leading to unwieldy power consumption, reduced dielectric reliability, and breakdown of the device altogether. Basically, the leakage current occurs because of the low dielectric constant (k=3.9) of the SiO_2. Alternative materials of high-k value are therefore highly sought after.

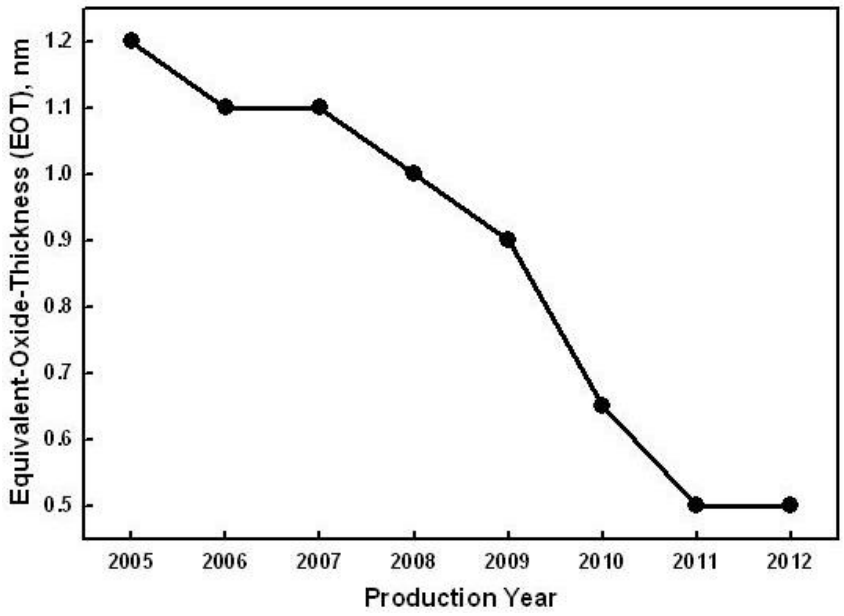


Figure 2.3: EOT of future generations of Si-based MOSFET technologies (ITRS, 2001, ITRS, 2004).

Significant research has been done on finding materials of high-k constant. The use of high-k materials is beneficial since thinner oxides can be used as gate dielectric. Since the insulating and dielectric behavior of high-k material is outstanding, the movement of the electrons through it is highly impeded. Thinner oxides can be used to fit the sub 100 nm MOSFET technologies.

2.3 Alternative high-*k* material for gate dielectric

Generally, materials possessing a dielectric constant value higher than that of SiO_2 are considered high-*k* dielectric material. High-*k* materials have been under intense investigation in order to find a replacement for SiO_2. One of the benefits of using high-*k* material as an alternative material for gate dielectric is that thicker films can be utilized to reduce leakage current while maintaining the same gate capacitance as thin SiO_2. As mentioned earlier, the MOS structure behaves like a parallel capacitor. Hence, when a voltage is applied to the gate, charges on the metal are compensated by opposite charges in the semiconductor. The capacitance of this parallel plate capacitor is given in Equation 2.1.

$$C = k \varepsilon_o A/t \qquad \text{(Eq. 2.1)}$$

C represents capacitance, *k* is dielectric constant, ε_o is permittivity of free space, A is capacitor area, and t is dielectric thickness. It shows that the capacitance value can be increased either by using a material of high *k* value or by reducing the thickness of the gate dielectric (t).

In the case of SiO_2, the *k* is 3.9 therefore the thickness can vary. However, reducing the thickness below its practical limit will cause a large leakage current across the gate dielectric due to direct tunneling. Hence, new materials of *k* higher than that of SiO_2 are needed to improve the device performance. This high-*k* material can attain the same dielectric capacitance of the SiO_2 by making it thicker than the SiO_2 layer. This can be achieved in the ratio of its dielectric constant to that of SiO_2, as shown in Equation 2.2. Equation 2.2 can be simplified to Equation 2.3. Equation 2.3 is often expressed in terms of the equivalent oxide thickness (EOT). EOT refers to the

thickness of the SiO_2 gate dielectric needed to obtain the same gate capacitance density as the high-*k* material in consideration (Houssa, 2004).

$$C_{SiO_2} = \frac{k_{SiO_2}\varepsilon_o}{t_{ox}} = C_{high\text{-}k} = \frac{k_{high\text{-}k}\varepsilon_o}{t_{high\text{-}k}} \quad \text{(Eq. 2.2)}$$

$$EOT = t_{high\text{-}k} = \frac{k_{high\text{-}k}}{k_{SiO2}} t_{SiO2} \quad \text{(Eq. 2.3)}$$

For example, by using ZrO_2 as a gate dielectric of *k* value 25, we can use a 6.4 nm thick oxide layer in order to achieve the same equivalent capacitance of a 1 nm thick SiO_2 layer. Therefore, it can be stated that the EOT of this ZrO_2 layer is 1 nm.

However, before a new high-*k* material can be used successfully in gate dielectric applications, many requirements have to be met first, as discussed in the next sub-section.

2.3.1 Requirements and promising material for alternative high-*k* gate dielectric materials

To be used as a gate dielectric material, the potential high-*k* materials must fulfill a set of requirements. These requirements have been reviewed in detail by Wilk et al., (2001), Wallace et al., (2002), Schlom and Haeni, (2002), Ray et al., (2006), Wong et al., (2006), and Droopad et al., (2005). According to the reports reviewed by those authors, it can be concluded there are 6 main requirements that have been used as

key guidelines for selecting an alternative gate dielectric material. These are as follows:

1. The material must possess a significantly higher *k* than amorphous SiO_2 (*k*=3.9).
2. The new material should be stable when in contact with Si.
3. The density of interfacial trap should be on par with SiO_2, and the trap levels within the dielectric should be low.
4. The conduction and valence band offset should be at least 1 eV (3.2 eV at the Si-SiO_2 interface) to provide a barrier with sufficient energy necessary for the gate action at the operational bias.
5. The electrical properties of the dielectric should be stable over a wide range of operating temperatures and operating frequencies.
6. The process to deposit the gate dielectric must meet the standard for uniformity and reproducibility set by the present gate dielectric deposition techniques and must meet these standards in a cost effective manner.

As mentioned above, the potential candidates must have a higher *k* than SiO_2. A dielectric constant of a material is measured in its bulk form. It must be stated that the dielectric constant of thin films could be different from that of bulk material. Figure 2.4 illustrates a plot of band gap against dielectric constant of several alternative materials considered to replace SiO_2. The trend shown is that materials of higher *k* tend to have lower band gaps. Dielectric constant is important in order to indicate the ability of the material to polarize in response to an applied voltage

(Eisenbeiser, 2005). Polarization will separate both positive and negative charges, leading to constitution of dipoles and provide more capacitance in capacitor. On the other hand, band gap is the energy difference between the valence band and conduction band. It determines the ability of electrons to flow between the two energy bands. Electrons are restricted in the flow from the valence band to the conduction band if the energy gap is large which reduce the leakage current problem. Therefore, both dielectric constant and band gap play important roles in selecting materials for gate dielectric.

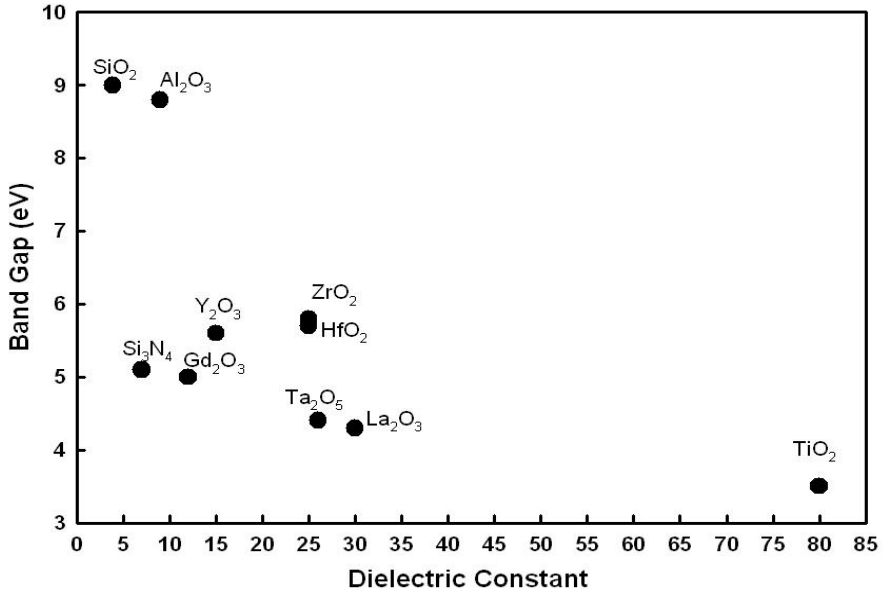
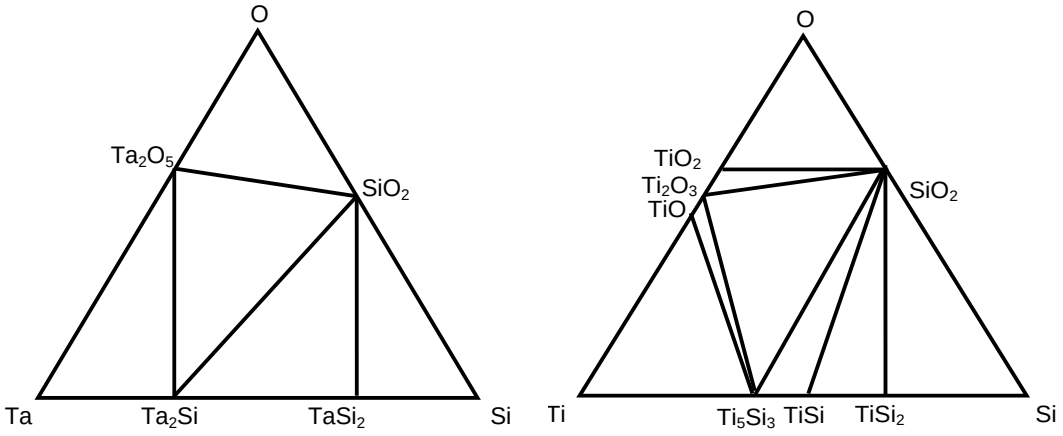


Figure 2.4: Plot of band gap and dielectric constant values of some potential high-k gate dielectric materials (Adapted from Kawamoto et al., (2002); Ray et al., (2006); Wallace et al., (2005)).

Besides the high-*k* value of, another requirement needed for the material to be a potential candidate for high-*k* gate dielectric is stability when in contact with Si. Materials need to be stable with Si to avoid formation of interfacial layer during deposition or in subsequent IC fabrication processes. This undesired interfacial layer could consist of SiO_2, silicide, or an alloy of high-*k* material and SiO_2. The formation

of an interfacial layer is highly undesirable since it will create an additional capacitor in series with the high-*k* layer and significantly reduces the overall effective dielectric constant. Therefore, the formation of interfacial layer should either be prevented or minimized.

The stability of high-*k* material on Si can be explained by referring to the ternary phase diagram. According to Schlom and Haeni, (2002) there should be a tie line between the stable metal oxide phase (high-*k*) and Si substrate in order to have a thermodynamically stable interface. Figure 2.5 and Figure 2.6 illustrate the ternary phase diagram of the Ta-O-Si, Ti-O-Si and Zr-Si-O system at 1000K respectively (Wilk et al., 2001). Figure 2.5 indicates that Ta_2O_5 and TiO_2 are not stable with SiO_2. Since there was no tie line between both oxides and Si when the thermodynamic equilibrium state was reached, they tend to separate into SiO_2 and metal oxide (M_xO_y) as well as silicide phases (M_xSi_y). ZrO_2 however, did have a tie line with Si as shown in Figure 2.6 and formation of $ZrSiO_4$ seemed to be stable in direct contact with Si. (Schlom and Haeni., 2002; Wilk et al., 2001).



(a) (b)

Figure 2.5: Ternary phase diagram of (a)Ta-O-Si and (b)Ti-O-Si systems (Adapted from Wallace et al., (2005)).

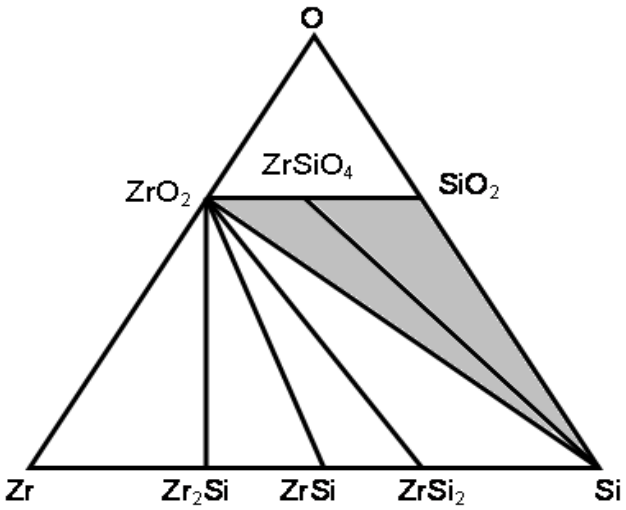


Figure 2.6: Ternary phase diagram of Zr-Si-O system (Adapted from Wallace et al., (2005)).

Apart from that, it is beneficial to choose an amorphous oxide as an excellent material for high-*k* gate dielectric. This is because polycrystalline or single crystal films could contain leakage paths at the grain boundaries or along crystal plane. Grain size and orientation variation in polycrystalline materials also cause significant variation in dielectric constant (Wallace et al., 2002). Amorphous materials are preferable because they can eliminate the stated disadvantages.

Figure 2.4 shows several possible materials of high-*k* dielectric value. Wong et al., (2006) have listed several oxides of high-*k* value. Oxides of materials from the following groups: IIIA (Al, Ga), IIIB (Sc, Y), IVB (Ti, Zr, Hf, Rf), VB (Nb, Ta) and lanthanoid (La, Ce, Pr anf Gd) are considered potential candidates. Characteristics and main features of potential high-*k* gate dielectric are compiled in Table 2.1. All the data present in the table were collected from several authors.

Table 2.1 Comparison of various relevant properties of some high-*k* candidates.

Material	**Dielectric constant (*k*)**	**Bandgap (eV)**	**Conduction Band offset (eV)**	**Merits**	**Drawbacks**	**References**
Silicon dioxide (SiO_2)	3.9	9	3.2	Excellent Si interface,	Low-*k*, EOT>0.8 nm	Porti et al., (2007)
Aluminum oxide (Al_2O_3)	9-10	8.8	2.1	E_g comparable to SiO_2, amorphous, good thermal stability	medium *k*	Shamala et al., (2007)
Gadolinium oxide (Gd_2O_3)	12	5.4	Not available	Good thermal stability with Si. high-*k*	Crystallization. Formatiopn of interfacial layer at Gd_2O_3/Si interface.	Kuei et al., (2008) Yue et al., (2008)

Table 2.1 (continue): Comparison of various relevant properties for some high-*k* candidates.

Material	**Dielectric constant (*k*)**	**Bandgap (eV)**	**Conduction Band offset (eV)**	**Merits**	**Drawbacks**	**References**
Yttrium oxide (Y_2O_3)	15	6	2.3	Large E_g	Low crystallization temperature, High D_{it}, silicide formation	Cheng et al., (2009)
Ytterbium oxide (Yb_2O_3)	~15	>5		High-*k* High resistivity Large E_g	Low crystallization temperature	Pan et al., (2009)
Hafnium dioxide (HfO_2)	25	5.7	1.5	Most suitable compared to other candidates	Crystallization, silicate and silicide formation. High trap density	Smirnova et al., (2008) Shaimeev et al., (2007) Chang et al., (2007)
Zirconium dioxide (ZrO_2)	~21 - 22	4.7-5.7	0.8-1.4	Similar to hafnia	Marginal stable with Si, crystallization, silicide formation	Kim et al., (2008)

Table 2.1 (continue): Comparison of various relevant properties for some high-*k* candidates.

Material	**Dielectric constant (*k*)**	**Bandgap (eV)**	**Conduction Band offset (eV)**	**Merits**	**Drawbacks**	**References**
Tantalum pentoxide (Ta_2O_5)	~17 - 29	4.4	0.38	High-*k*	Unacceptable ΔE_c not stable on Si,	Atanassova et al., (2007) Chandra et al., (2008)
Titanium dioxide (TiO_2)	~30 – 170 (depending on crystal structure & orientation)	3.0 – 3.8	<1	very high-*k*	Not stable on Si High leakage current Low band gap	Frank et al., (2009)
Lanthana (La_2O_3)	27	5.8	2.14	High-*k*, better thermal stability,	Moisture absorption, instable with Si,	Kim et al., (2005) Kim et al., (2008)
Strontium titanate ($SrTiO_3$)	300	3.3	-0.1	High-*k*	Low crystallization temperature.	Lin et al., (2007)

2.4 Zirconia

Zirconia (ZrO_2) is an interesting material which has attracted much attention due to its remarkable properties such as high mechanical strength, low thermal conductivity, extreme chemical inertness, excellent wear resistance, high refractive index (more than 2) and high transparency in the visible and near infra-red (IR) region. In fact the combination of electronic, optical and mechanical properties has led to its wide range of applications for example as a thermal barrier coating (Janos et al., 1999), corrosion protective coating (Gusmano et al., 2007), oxygen sensor (Hiroyuki et al., 2003; Spirig et al., 2007), catalyst support in automobile industry (Vera et al., 1998) and as ceramic biomaterial (Heuer et al.).

Recently, ZrO_2 has shown a prospective application in microelectronic industry. ZrO_2 is said to be a potential candidate to replace SiO_2. Here, the crystal structure, properties and deposition technique used in producing ZrO_2 for high-*k* gate dielectric is elucidated.

Pure bulk ZrO_2 exhibits three polymorphs of monoclinic, tetragonal and cubic symmetries. Figure 2.7 illustrates the crystal structure of each polymorph. The monoclinic phase is stable at room temperature and can transform to the tetragonal phase during heating at 1170 ^oC. At 2370 ^oC, the tetragonal phase transforms to the cubic phase. ZrO_2 melts at 2680 ^oC (Graeve, 2008).

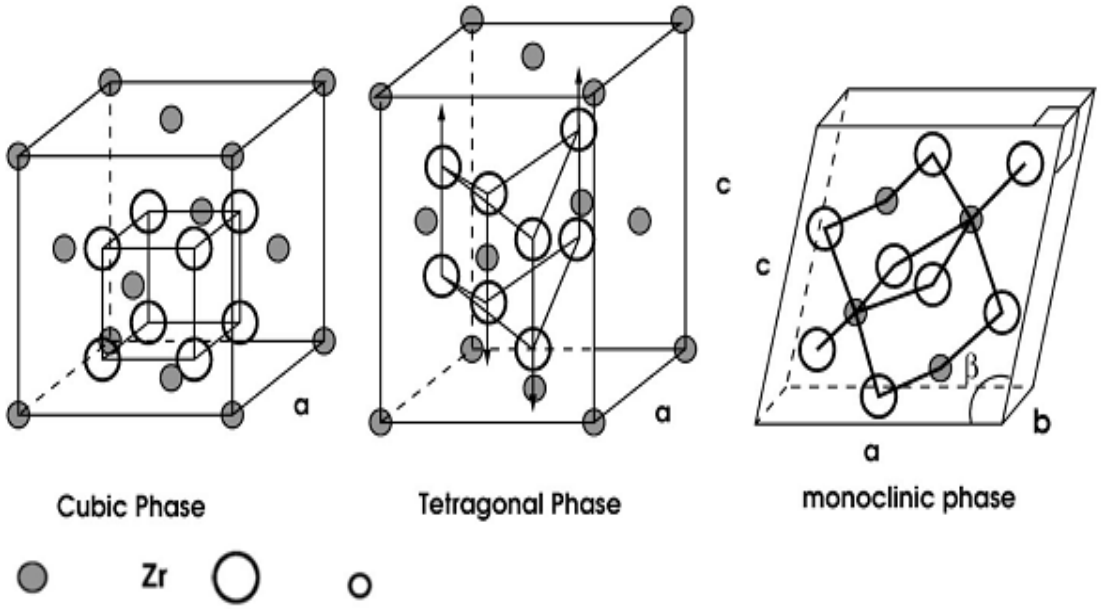


Figure 2.7: Crystal structure of the ZrO_2 phases: cubic, tetragonal and monoclinic (Zhao et al., 2002).

2.4.1 Properties of ZrO_2 as a potential candidate for high-*k* gate dielectric

As a promising candidate for alternative gate dielectric, ZrO_2.has several outstanding properties such as high dielectric constant (k = 20-25) which is high enough to achieve lower EOT. It has a wide bandgap (>5 eV) hence high potential barrier (>1 eV) and thus can reduce the problem of leakage current. In addition ZrO_2 has a good thermal stability on Si substrate with a small lattice mismatch of 2.1% with Si. Nevertheless, one major problem of ZrO_2 is its crystallinity. Amorphous ZrO_2 is not thermodynamically stable at room temperature. Most research reports have shown that deposited ZrO_2 film is of polycrystalline material consisting of mixtures of monoclinic, cubic, or tetragonal phases. Comparison of the material properties of ZrO_2 and SiO_2 is shows in Table 2.2.

Table 2.2: Comparison of SiO_2 and ZrO_2 material properties between (Wong et al., 2006).

Properties	**SiO_2**	**ZrO_2**
Structure	Amorphous	Depend on deposition methods
Dielectric constant	3.9	22-25
Bandgap (eV)	8.9	4.7-5.7
Lattice parameter (Å)	-	5.07-5.16
Formation temperature (^oC)	>700 ^oC	~350 ^oC
Crystallization temperature (^oC)	-	>350 ^oC
Stability with Si (kJ/mol) at 298K	Stable	Yes
Silicide formation	-	Yes
Hole barrier (eV)	4.2	2.5-2.9
Electro barrier (eV)	3.15	0.8-1.4
Interface trap density ($eV^{-1}cm^{-1}$)	~10^{10}	~10^{12}
Oxide trap density (cm^{-2})	~10^{11}	~10^{12}
Breakdown field (MV/cm)	~10	<4

2.4.2 Deposition techniques of ZrO_2 for high-*k* gate dielectric

Numerous techniques have been used when producing ZrO_2 films as a gate dielectric. Those techniques can be divided into physical, chemical and oxidation processes.