CFD SIMULATION OF UNDERFILL ENCAPSULATION PROCESS IN FLIP CHIP PACKAGING WITH VARIOUS DISPENSING METHODS

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CFD SIMULATION OF UNDERFILL ENCAPSULATION PROCESS IN FLIP CHIP PACKAGING WITH VARIOUS DISPENSING METHODS

by

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LIST OF SYMBOLS

SYMBOL	DESCRIPTION	UNITS
English Symbols		
A_1, A_2	Pre-exponential factors	1/s
B	Exponential-fitted constant	Pa.s
C_1, C_2	Fitting Constant	-
C_p	Specific heat	J/kg-K
E_t	Total energy	J/m^3
E_1, E_2	Activation energies	K
F	Front advancement parameter	-
g	Specific gravity	m/s^2
k	Thermal conductivity	W/m-K
k_1, k_2	Rate parameters described by an Arrhenius temperature dependency	1/s
m^*, n^*	Constants for the reaction order	-
n	Power law index	-
p	Pressure	Pa
r	Displacement of particle	Mm
T	Temperature	K
t	Time	s
T_b	Temperature fitted constant	K
u	Fluid velocity component in x-direction	mm/s
v	Fluid velocity component in y-direction	mm/s
w	Fluid velocity component in z-direction	mm/s
x, y, z	Cartesian coordinates	mm

Greek Symbols

α	Conversion of reaction	-
α_g	Degree of cure at gel	-
ΔH	Exothermic heat of polymerization	J/kg
η	Viscosity	Pa.s
η_0	Zero shear rate viscosity	Pa.s
ρ	Density	Kg/m^3
τ	Shear stress	Pa
$\dot{\gamma}$	Shear rate	1/s
υ	Kinematics viscosity	m^2/s
ν_{ad}	Artificial diffusity	-
Φ	Energy source term	J
τ^*	Parameter that describes the transition region between zero shear rates and the power law region of the viscosity curve	Pa
$\xi\eta\phi$	Uniform orthogonal computation space	-

LIST OF ABBREVIATIONS

		PAGE
2-D	Two-dimensional	21
3-D	Three-dimensional	12
ASIC	Application specific integrated circuit	3
C4	Controlled Collapse Chip Connection	4
CAE	Computer Aided Engineering	25
CBS	Characteristic based split	24
CCGA	Cast Column Grid Array	4
CFD	Computational Fluid Dynamic	11
COB	Chip on Board	4
CPU	Centre Processing Unit	5
CSP	Chip Scale Package	4

CV	Control Volume	36
DCA	Direct Chip Attach	4
FDM	Finite difference method	21
FEM	Finite element method	21
FVM	Finite volume method	12
GNF	Generalized Newtonian fluid	13
IC	Integrated circuit	1
I/O	Input / Output	1
PCB	Printed Circuit Board	1
PBGA	Plastic Ball Grid Array	4
PDA	Personal Digital Assistant	4
QFP	Quad Flat Pack	4
TAB	Tape Automated Bonded	4
VOF	Volume of fluid	13

SIMULASI CFD BAGI PROSES PENGKAPSULAN UNDERFILL DALAM PAKEJ FLIP CHIP DENGAN MENGGUNAKAN PELBAGAI KAEDAH SUNTIKAN

ABSTRAK

Trend utama dalam industri elektronik adalah untuk menghasilkan produk yang lebih pintar, ringan, berfungsian dan padat, serta lebih murah. Aliran ini telah memerlukan keperluan-keperluan pembungkusan ketat dan flip chip teknologi telah ditimbulkan sebagai satu pilihan baik bagi mengatasi isu ini. Bagaimanapun, satu isu serius dalam flip cip pembungkusan adalah perbezaan dalam pekali pengembangan terma antara cip silikon dan substrat organik, yang menghasilkan thermo mekanikal yang menekankan dan sebab-sebab keletihan dalam pateri sendi-sendi. Masalah ini diselesaikan dengan berkesan oleh underfill proses di mana ruang antara cip silikon dan PCB dipenuhi dengan underfill encapsulant yang membahagi-bahagikan semula teraruh menekankan dengan itu mempertingkatkan kebolehpercayaan pateri sendi-sendi. Dalam penyelidikan ini, kajian-kajian pada flip-chip 3-D underfill proses dibentangkan. Satu kaedah jumlah yang terhingga berdasarkan persamaan Navier-Stokes telah diaplikasikan untuk analisis aliran dalam underfill proses. Model aliran bendalir tanpa kesan pengawetan diambilkira dalam pertimbangan bagi reologi polimer. Kesan-kesan bagi pelbagai keadaan suntikan telah dikaji. Tambahan lagi, kesan aliran terhadap tatasusunan pateri telah dikaji. Pengesahan bagi perisian FLUENT tentang pengendalian polimer proses mengenyangkan telah dipersembahkan. Keputusan daripada simulasi berangka menunjukkan persetujuan yang baik dengan keputusan dari eksperiment. Keputusan kajian menunjukkan kaedah suntikan L memberi keadaan yang lebih baik dalam proses pengisian underfill. Lagipun, tatasusunan pateri dalam flip-chip memberi kesan ke atas proses

underfill konvensional. Tatasusunan pateri memberi kesan terhadap peningkatan masa pengisian dan justeru menyebabkan peningkatan dalam kos pembuatan. Manakala, cara pengisian underfill adalah sesuai untuk proses pengisian multichip. Kebaruan kerja ini adalah dengan menggunakan FLUENT untuk cara pengisian underfill dalam industri mikroelectronik.

CFD SIMULATION OF UNDERFILL ENCAPSULATION PROCESS IN FLIP CHIP PACKAGING WITH VARIOUS DISPENSING METHODS

ABSTRACT

The major trend in electronic industry is to make the products smarter, lighter, functional and highly compact, at the same time cheaper. This trend has necessitated stringent packaging requirements and the flip-chip technology has emerged as a promising option to tackle this issue. However, a serious issue in flip-chip packaging is the difference in the coefficient of thermal expansion between the silicon chip and the organic substrate, which generates thermo-mechanical stresses and causes fatigue in solder joints. This problem is effectively solved by the underfill process in which the space between the silicon die and the PCB is filled with the underfill encapsulant that redistributes the induced stresses thereby enhancing the solder joints reliability. In this research, the studies on the 3-D flip chip underfill process is presented. A finite volume method based on Navier-Stokes equation has been applied for the flow analysis in the underfill process. The fluid flow models without curing effect (Cross model) is take into consideration the polymer rheology model. The effects of different dispensing and injection situation have been studied on conventional and pressurized underfill process. In addition, the effect of the solder bump array has been studied. Verification of FLUENT software on handling polymer filling process has been performed. The numerical results showed good agreement with the experimetal results. The results showed that the L-dispensing and injection situation give better filling on underfill filling process. Moreover, the solder bump array gives the effect to the underfill flow during the conventional underfill process. The solder bump array significantly influence the filling time, thus it may effecting the manufacturing costs. However, pressurized underfill method is found suitable for

multichip underfill process. The novelty of this work is the used of FLUENT for prediction of flip chip underfill process in microelectronics industry.

CHAPTER 1

INTRODUCTION

1.1 Introduction

In the early 1960's, various ideas were tried out in the semiconductor industry for connecting the new Integrated Circuits (IC) to printed circuit boards (PCB) in the microelectronic devices technology. One of the main semiconductor companies in early 1960's, IBM developed the flip chip package. Development of the flip chip had enriched and improved the microelectronic technology. In recent years, the flip chip technology has switched over to the interconnection of chip and the printed circuit board and also the sizing factor of the flip chip packages. The interconnections of the chip represent the most important input/output (I/O) in flip chip packages. The interconnection in flip chip packages is also called solder bumps. Thus, the reliability of the flip chip package is an important issue in the manufacturing process. The fracture and failure of the interconnectors causes malfunction of the chip and also increases the manufacturing cost. To overcome these problems, underfill encapsualant has been applied in the flip chip technology. The main function of underfill encapsulant is to protect the chip from moisture, ionic contaminants, radiation, thermal expansion, shock, and vibration. During the manufacturing process, underfill encapsulant is dispensed to fill the space between chip and substrate around the solder interconnectors. Choosing the right dispensing types and method are imperative to properly underfilling a flip chip.

1.2 Electronic packaging, integrated circuits (ICs) and flip chip.

Electronic packaging is defined as a house that is built in the electronic system to protect and enclose the components in the electronic product. Besides,

electronic package is also a part of the microelectronic system. Typically the microelectronic system refers to the micro devices of electronic products measured in micrometers (µm), such as integrated circuit (IC). IC is a miniaturized electronic circuit on a thin substrate of semiconductor material that contains the combination of many circuits or components such as transistors, resistors, inductors, capacitors, etc. IC is also known as microchip, silicon chip or chip in electronic technology. Electronic package functions as a house for electronic system and protects the electronic components from hostile environment and mechanical effects such as thermal and vibration besides providing a structural support and electrical insulation. Moreover, it provides heat dissipation, signal timing and power distribution for the whole system to function properly.

Integrated circuits (ICs) are processed from a large piece and thin substrate of semiconductor material. The semiconductor substrate is called wafer. Wafer is made out of pure silicon and it is prepared into a circular shape with diameter 3 to 12 inches. Typically the wafer is sliced into thickness 0.75mm and polished to obtain a flat surface. After wafer processing, the wafer is mount and cut by fully automatic dicing saw which is tipped with synthetic diamond. Thousands of individual dies are cut from a wafer at the end of the dicing process. The individual die piece is transformed into the IC package in the final stage of the IC fabrication process. In the final stage, the die piece is attached to the package or support structure by different operations such as wire bonding and flip chip according to the design of IC package. Testing and assembling to the system board process is performed to ensure proper function of the IC package as a microelectronic component. Figure 1.1 describes the entire fabrication process to form an IC package.

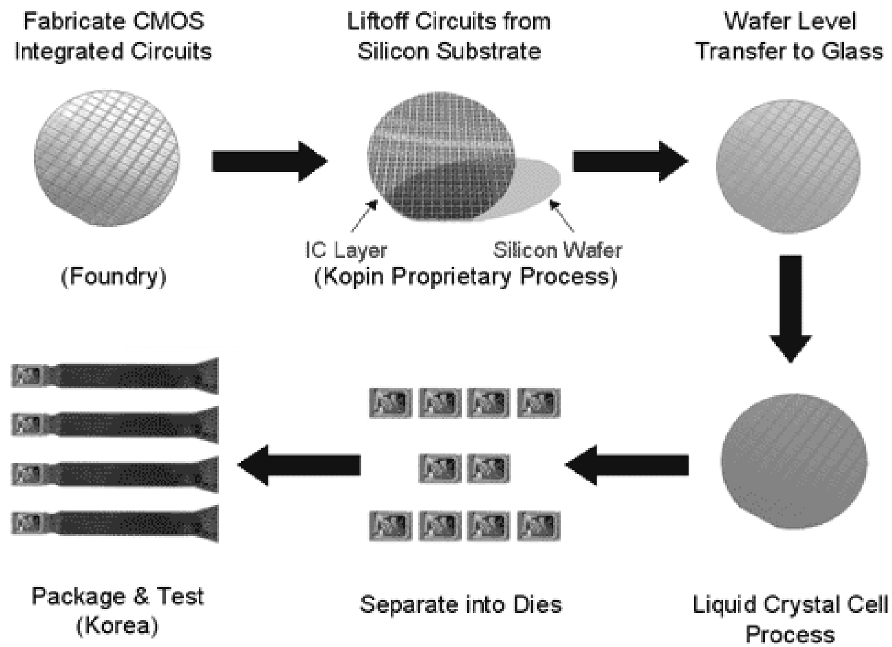


Figure 1.1 IC fabrication process (www.kopin.com).

Development of different IC technologies is required for different IC devices and applications. The major IC devices include microprocessor and application-specific IC (ASIC). Nowadays, the trend of electronic products is towards the miniature and compact product. Electronic products such as computer, notebook, PDA (Personal Digital Assistant) and cell phone have improved the life quality and convenience. Thus, these types of products require smaller, thinner and powerful IC packages. The IC scale has been scaled down year by year. Figure 1.2 shows the development of IC scale.

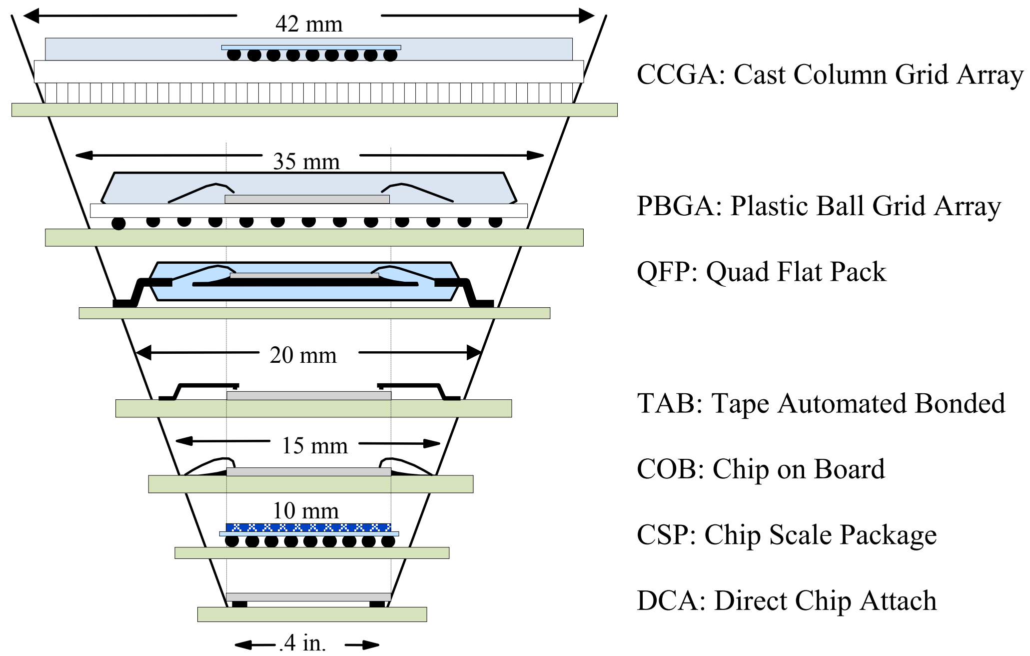
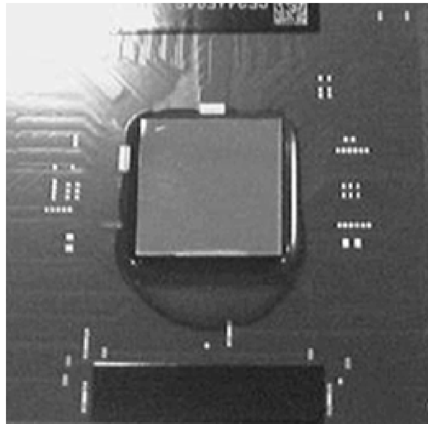
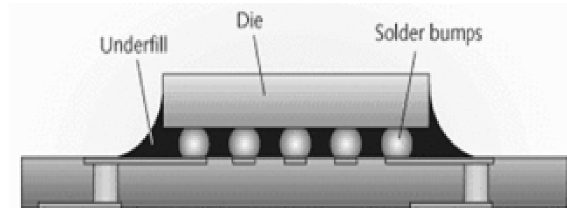


Figure 1.2 Development of IC scale.

Flip chip is one of the methods for interconnecting of semiconductor devices, such as IC packages. It is also known as Controlled Collapse Chip Connection, C4. In this method, the top surface of silicon chip is faced down and deposited with the solder bumps to mount on the external circuit. The solder bumps are aligned with the external circuits and the solder is flowed to complete the interconnection between silicon chip and external circuit. Flip Chip package is shown in Figure 1.3. Illustration of flip chip packaging shows that the solder bumps are located between the die and substrate or PCB within a certain gap height. The solder bumps function as a connector and provide a space between the chip and the board. In the final stage of assembly process, the space is filled with a non-conductive "underfill" material to join the entire surface of the chip to the substrate. This process enforces the strength of connection between the chip and substrate. Moreover, the underfill material protects the solder bumps from moisture and environmental hazards. The most important function of underfill material is to indemnify for thermal expansion in between silicon chip and the substrate. Underfill mechanically engages the chip and

substrate, so differences in thermal expansion do not break the electrical connection of the bumps.





(a) (b)

Figure 1.3 Flip chip CPU package (a) (www.intel.com) and illustration of Flip Chip packaging (http://ap.pennnet.com).

During underfilling process, underfill material may be needle-dispensed along the edges of each chip or injected by pressure. Another method known as no-flow underfilling has also been introduced recently. In the conventional underfill process, underfill is drawn into the space by capillary action, and then it will be heat-cured to form a permanent bond. Nowadays, the advancements in electronic packaging caused the dispensing process become a critical part of the manufacturing line. Therefore, the popularity of flip chip underfilling has led to complications such as the need of rigorous attention to accuracy and effectiveness to the assembly line in the microelectronic industry. Although the underfilling process has become a manufacturing variable, many of the dispenser manufacturers have developed high accuracy dispenser machines that have greatly ameliorated underfilling flip chips while maintaining productivity. In addition, improvements of underfill materials have also reduced many of the common process control issues.

1.3 Flip chip underfill filling process

This subsection gives an overview of underfill processes that are available in the semiconductor and flip chip packaging technology. The purpose of underfilling is to increase the strength of solder bumps and protect the flip chip and solder bumps from various hazardous conditions such as thermal expansion, mechanical and environmental conditions. Besides, underfilling also increases the reliability of the flip chip packages and minimizes the product reject costs. There are three types of underfilling processes, conventional underfill, pressurized underfill encapsulation and no-flow underfill.

1.3.1 Conventional underfill process

In conventional underfilling, flip chip is conveyed into the dispensing equipment. To provide the good underfill flow, the die is heated to the desired temperature or heated during dispensing process. Then, the flip chip is located by an automated vision alignment system to ensure the location of flip chip to the solder bumps correctly. After the flux dispensing, solder bump reflow and flux cleaning processes, the underfill material is dispensed on one or more sides of the flip chip such as L and U type dispensing, sometimes in multiple dispense passes. The underfill material flows via capillary action under the flip chip to fill the space between chip and substrate. Finally, the filled underfill is cured in a microwave oven at the recommended temperature. Figure 1.4 illustrates the steps in conventional underfill process.

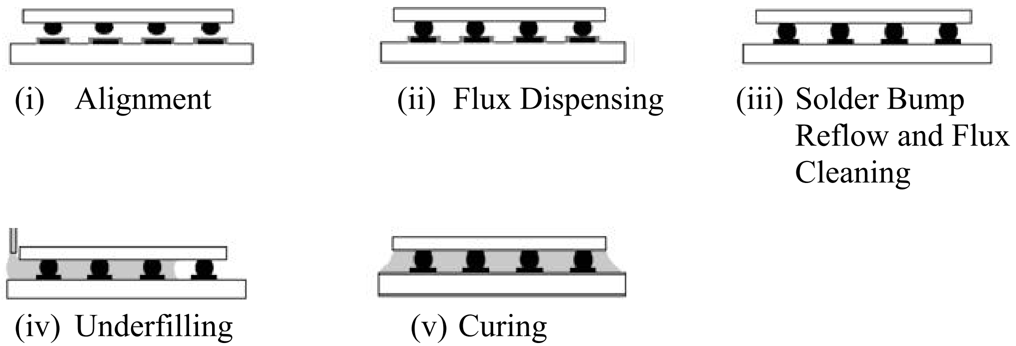


Figure 1.4 Conventional underfill process (Wan et al., 2007).

1.3.2 Pressurized underfill encapsulation process

Pressurized underfill encapsulation is another method that has been proposed by previous researchers. In order to improve the efficiency of flip chip package during underfill process, some researches were proposed on investigating and creating different processes (Han and Wang, 1997). Pressurized underfill is designed to increase the force of the capillary action when the undefill material flows through the under-chip space. External pressure is applied to replace the capillary force and to increase the flow rate of the underfill process. It also minimizes the filling time of each underfill process. This concept is similar to the injection molding process in which molten plastic is injected to the mold. In the pressurized underfill process, the specific mold is designed accordingly to the silicon chip size. The chip's mold is clamped and fixed to the chip before the encapsulant is dispensed into the mold. Figure 1.5 illustrates the process of pressurized flip chip underfilling.

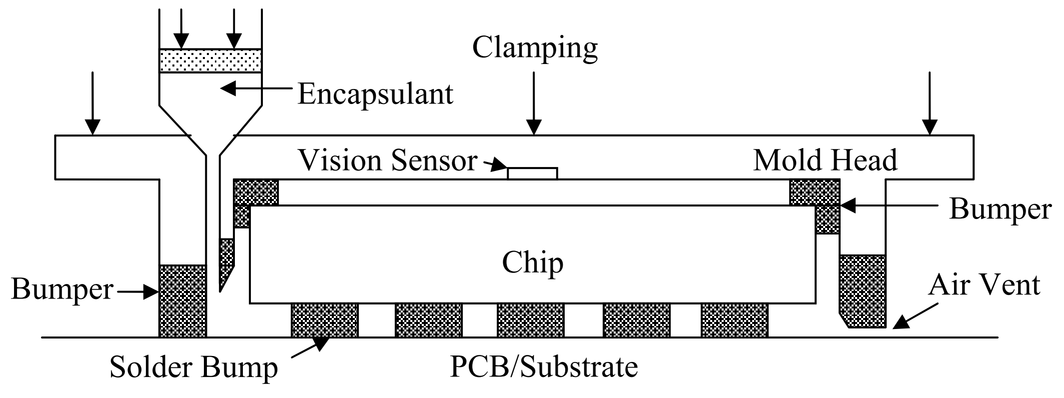


Figure 1.5 The pressurized process of underfill (Han and Wang, 1997).

1.3.3 No-flow underfill process

Manufacturing cost is an important concern for manufacturers. Elimination of certain processes reduces the cost and time of filling. In flip chip technology, the low cost flip chip assembly process is being developed. This process significantly lowers the costs and reduces the cycle time. No-flow underfill is referred to the flip chip assembly process without capillary action when underfill material fills the under-chip space. This process is also known as compression flow underfill or direct pressurized underfill process. The first no-flow underfill for flip chip packages was reported by Wong and Badwin, 1996. Flip chip assembly process has much difference compared to conventional and pressurized underfill methods. In this assembly technique, the underfill is applied on the substrate/PCB prior to chip placement. After the underfill dispensed silicon chip is placed on the substrate, it is pressed to squeeze the underfill material to fill the under-chip space. Reflow and curing processes are performed at the final stage of the underfill process. Figure 1.6 shows the no-flow underfill process.

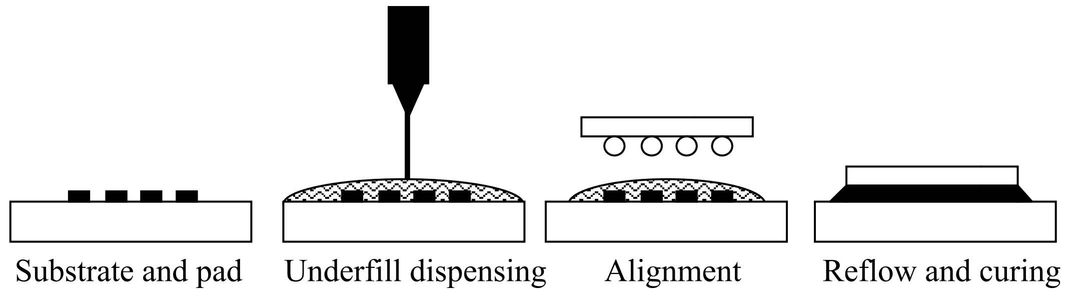


Figure 1.6 No-flow underfill processes (Wan et al., 2007).

1.4 Underfill background and problems

Underfill is a famous technique used for protection of flip chip packaging. This technique provides great impact on the reliability of electronic devices and also improves the reliability of the flip-chip interconnect systems. Three types of underfill processes have been discussed in section 1.3. Conventional underfill is the most familiar technique because of its development and the availability of dispensing machines in the current industry. This technique has been developed and practiced for nearly 20 years (Wan et al., 2007). Figure 1.7 shows the schematic of the conventional underfill encapsulation process.

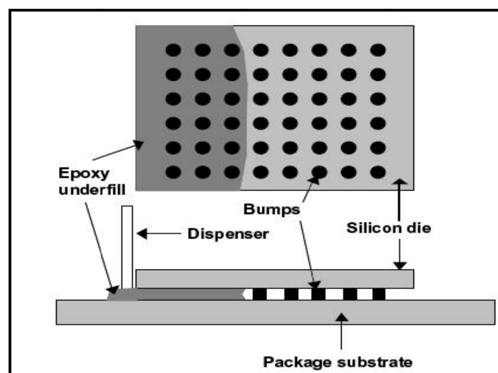
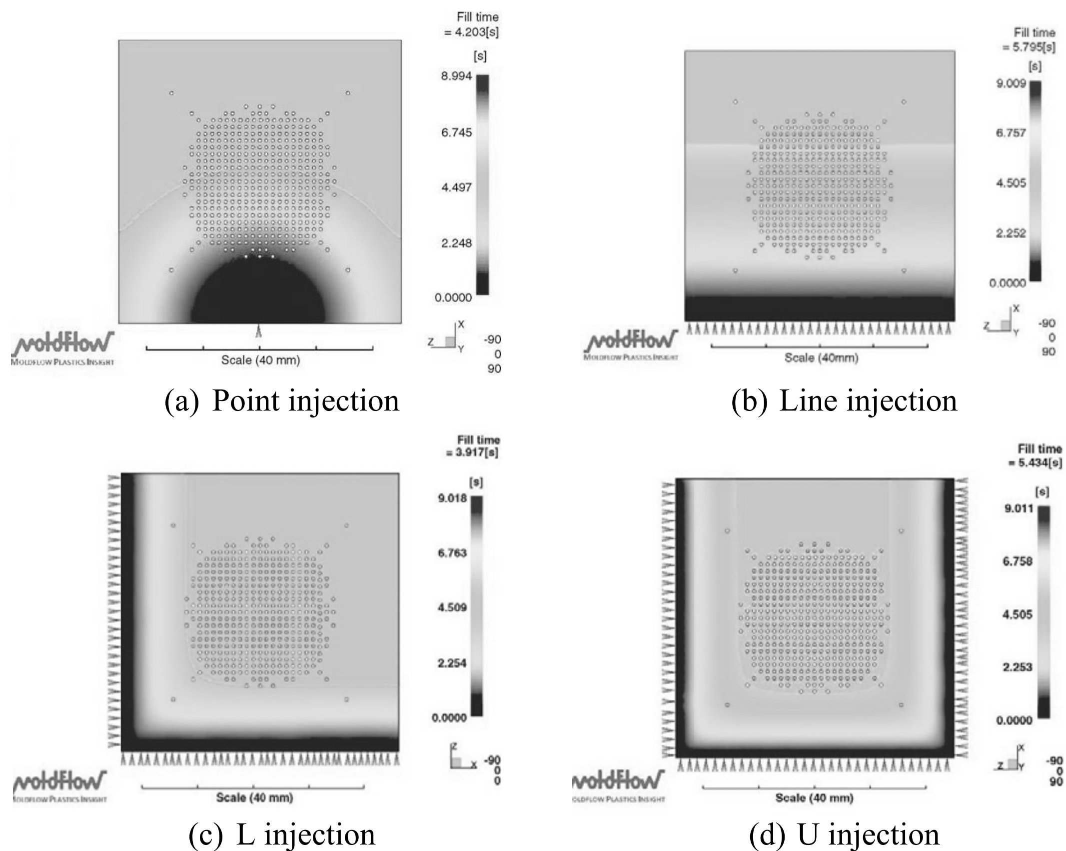


Figure 1.7 A schematic of the underfill encapsulation process: (a, top) shows the top view of the underfill material flowing between the bumps and (b, bottom) shows the cross-section. (Pantuso et al., 2003)

Although the conventional flip chip underfill technique has been practiced nearly 20 years, it is still deffficult to optimize and observation of fluid flow during the process especially for small scale flip chip packages. The design of the flip chip package and the number of the solder bumps in flip chip package affect the fluid flow behaviour during underfilling process. Besides, the dispensing pattern may cause the void at the central region of flip chip package. Void in the package causes defect and failure of the flip chip package. To minimize the impacts of this problem, numerical analysis for underfill process is needed. Many softwares have been developed for the underfill process, such as PLICE-CAD, MoldFlow, Cadmould, C-mould, MAGMAsoft etc. Figure 1.8 shows the predicted melt front advancement using MoldFlow software.



(a) Point injection (b) Line injection

(c) L injection (d) U injection

Figure 1.8 Predicted melt front advancement of pressurized underfill on different injection type using Mold Flow software. (Shen et al., 2006)

1.5 Problem statement

Flip chip underfilling process has become an important process in microelectronic industry. In fact, flip chip provides superior electrical performance due to the shorter electrical connection. Flip chip package is able to provide high input/output capacity and smallest possible package size for microelectronic systems. Due to the requirement of the microelectronic products, continuous improvement is required for flip chip underfill process and flip chip design. Filling time, size of the flip chip and the simple design with high reliability etc. are the issues addressed by the researchers. Besides, void and defect during flip chip underfill process will cause the malfunction and low reliability of the flip chip.

Computational modeling on underfill flow analysis has provided the solutions and the understanding on the effects that cause problems in underfill process. Therefore, the present study is aimed to develop the three dimensional flip chip underfill model and to study the flow profile, filling time; different dispensing types and different arrangements of flip chip solder bumps in flip chip underfill process. The CFD code, FLUENT 6.3 is utilized in the investigation. This work is expected to provide the improvement and guideline for flip chip underfill process in microelectronic industry and introduce the CFD code in handling the underfill problem. Figure 1.9 shows the three dimensional of flip chip meshed model.

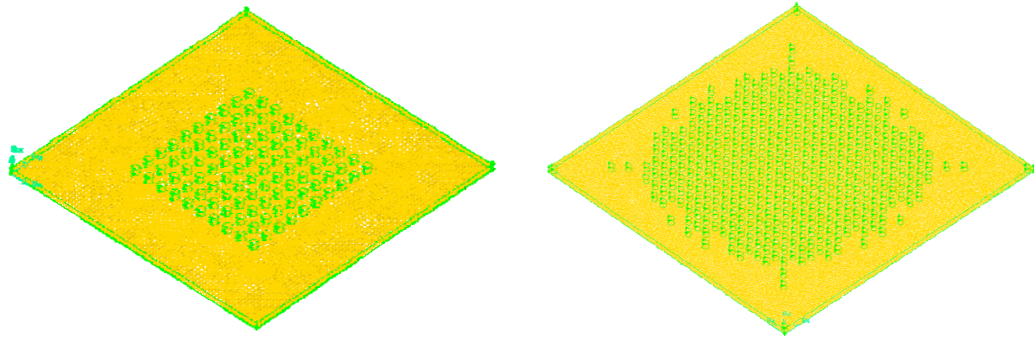


Figure 1.9 Different types of flip chip meshed model package.

1.6 Objectives of the study

The present study has four main objectives as mentioned below:

1. To validate the CFD software based on finite volume method (FVM), non-isothermal, incompressible flow to analysis of mold filling for 3D injection molding and flip chip underfill process.
2. To study the flow behavior of capillary driven and pressurized flip chip underfill processes.
3. To investigate the effects of different dispensing and injection types on the underfill flow.
4. To study the effects of the solder bumps array to underfill flow for three different solder bumps array packages.
5. To investigate the flow behavior of multichip underfill under capillary effect and pressurized conditions.

1.7 Scope of the research work

In this research work, the simulation of fluid flow is focused on generalized Newtonian fluid (GNF) by considering cross viscosity model. This research also concentrates on different dispensing and injection types for conventional and

pressurized underfill process. The validation of the CFD software on solving polymer flow behavior is performed with the injection molding experiment and the flow behavior of the underfill process is compared with that obtained by the previous researchers. The effect of solder bump array on the underfill flow and filling time in conventional underfill technique is also included in the investigation. Volume of fluid (VOF) technique is used to track the melt front of the underfill material.

1.8 Thesis outline

This thesis is organized in five chapters. Brief presentation about IC packaging, flip chip underfill, background, objectives and scope of research have been introduced in chapter one. Literature study of flip chip underfill process is presented in chapter 2. In chapter 3, the methodology in mathematical modeling and numerical method is highlighted. The comparison of experimental results and simulated results are presented in chapter 4. The effect solder bump approach in conventional underfill process is also discussed in this chapter. Lastly, concluding remarks and recommendation for future works are described in chapter 5.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

The current trend of electronic devices is towards faster smaller and cheaper components, such as personal computer, laptop, cell phones, PDA, etc. More strict requirements on the electronic packaging are needed in the electronic industry. Flip chip technology is one of the methods to make the trend possible because of the powerful electrical performance in flip chip package and the high capacity of input/output and also the smallest possible package size (Wan et al., 2007). In 1960s, controlled collapse chip connection (C4) has been successfully invented by IBM; the silicon chip is connected with solder bumps to substrate for electricity supply. C4 flip chip package is built with diameter, 100-250 micro meters and height; 50-200 micro meters (Gordon et al., 1997). Figure 2.1 illustrate the C4 flip chip packaging.

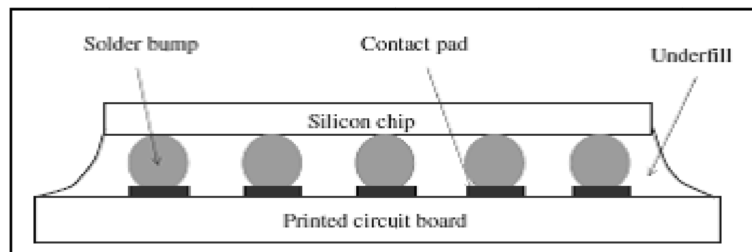


Figure 2.1 Illustration of C4 flip chip packaging (Wan et al., 2007).

In this chapter, substantial previous works will be discussed. The main concerns in flip chip underfill are the flow behavior, its effect by the measureable parameters, namely, viscosity, contact angle, filler size and distribution (Fine et al., 2000). Surface tension coefficient and curing kinetics also affect the flow in underfill process (Han and Wang, 1997). The effect of solder bump pitch on the underfill flow was reported by Young and Yang (2002) who found that the solder bumps, chip and

substrate acted as resistances to the underfill flow and the filling time was affected by bumping pitch, bump diameter and gap size.

The flow analysis has been improved when Wan et al. (2005) reported that resistance of the solder bump to the flow was negligible when the clearance between two bumps was greater than 60-70 µm. Besides, the research work also showed the assumption of steady flow in flip chip underfill was reasonable. An improvement of the flow characteristics in flip chip encapsulation has been mentioned by Wan et al. (2005); the power law model showed better prediction of flow behavior.

The simulation of the underfill flow aided by commercial software becomes one of the important milestones in flip chip underfill technology. Simulation helps prediction of the melt front advancement of underfill and problems such as void formation during underfilling process. Various commercial softwares such as Moldflow, MAGMAsoft, Cadmould have been utilized in flip chip underfilling process (Shen et al., 2004). Investigations through experiments and simulations have improved the flip chip technology in several ways.

2.2 Conventional underfill

Capillary action and various measurable parameters play an important role on the flow behavior and filling time in conventional flip chip underfill. The understanding of the capillary action helps improvement of the flip chip and solder bump design and the selection of the material for flip chip package. Therefore, the review of capillary action in flip chip underfill is made and presented in subchapter 2.2.1.

2.2.1 Capillary action

Han and Wang (1997) had developed a model for capillary driven encapsulation. Comparison of simulation and experimental work indicated that the model developed was adequate for melt front prediction in flip chip underfill. Investigation on the anisotropic effects of capillary action in the flip chip has been performed by Young (2003). Underfill encapsulant was filled by a capillary flow in flip chip underfill process. Young found that the capillary action was different in different directions. The critical value for capillary flow was found in 45° direction. Modified Hele-Shaw flow model was applied in Young's work.

Young (2004) also studied capillary rise of liquid in a cylinder bank. Calculations were done by considering the local geometric variation of the flow channel and the position dependent equivalent capillary pressure. Estimation of the capillary pressure was done by considering the rate of filling of several layers of cylinder and it was applied to the flip chip underfill system.

Experimental verification of model for underfill flow driven by capillary forces in flip chip packaging has been reported by Wan et al. (2008). The mismatch with the Washburn model was investigated in the experiment. Non-Newtonian behavior was confirmed on the underfill fluid in flip chip packaging and the Washburn model was only applicable on Newtonian fluid. Besides, power law model was found applicable in rheology behavior of underfill material.

Conventional capillary flow underfill in flip chip packaging has been studied numerically by Hashimoto et al. (2008). The flow behavior and filling time of underfill material and also the fluid dynamic force acting on the solder bump were

investigated. In addition, no-flow underfill has also been reported by Hashimato et al. (2008).

2.2.2 Numerical analysis

Substantial research has been carried out in the numerical modeling of flip chip underfill process. An excellent review of the various models to describe the properties of underfill flow driven by capillary action is provided by Wan et al. (2007). Zhang and Wong (2004) reviewed the recent advances in the material design, process development and reliability issues of flip-chip underfill, especially in no-flow, molded and wafer-level underfills.

Nguyen et al. (1999) used plastics integrated circuit encapsulation computer aided design (PLICE-CAD) for numerical analysis and the results were validated with the flow front observation experiment. The two-phase flow was solved by volume of fluid method in the simulation. Geometrical factors such as bumps and die edges were taking account into the simulation. Different solder bumps patterns have been used in the simulation studies.

Hashimoto et al. (2008) developed a computational fluid dynamics (CFD) solver for the underfill flow simulation of both capillary flow and no-flow types. Surface tension and contact angle effects were considered in the analysis. In this work, Hashimoto et.al found the potential of the CFD solver for predicting the underfill flow for both types of underfill methods.

A 3D transient heat transfer and cure kinetic coupled finite element model was developed by Liu et al. (2004) to study the microwave curing process of underfill material in flip-chip packaging. Yong (2003) investigated the anisotropic effects of the capillary action induced by the solder bumps using a modified Hele–

Shaw flow model, considering the flow resistance in both the thickness direction and the restrictions between solder bumps. A study on no-flow underfill by Lu et al. (2002) focused on the relationship between the material properties and reliability, and on how underfill entrapment might affect the thermal–mechanical fatigue life of flip chips.

Meuwissen et al. (2006) proposed a constitutive finite element model for predicting the stresses in thermosetting resins during and after cure of flip-chip underfilling process.The thermal fatigue properties of the solder joints with various underfills were evaluated by Noh et al. (2008) using thermal shock test. Wang (2007) investigated the effects of yield stress of underfill on filler settling and the effects of shear thickening of underfill at large shear rates on flow voids. The effects of viscoelastic properties of underfill resin on mechanical responses and residual stresses of flip chip packages were studied by Sham et al. (2007).

Palaniappan et al. (1999) studied the effect of the cure parameters on a selected commercial underfill and correlated those properties with the stress induced in flip chip assemblies during processing. Lin et al. (2007) attempted to combine capillary force, pressure difference, and inertia effects to enhance the flow rate and reduce the filling time in flip-chip underfill packaging. Recently, electromigration phenomena in Sn–3Ag–0.5Cu and in solders in flip chip joints were investigated by Yamanaka et al. (2009).

2.3 Pressurized underfill

Appreciable studies on mold flow in flip chip packages had been carried out by Shen et al. (2001) using CAE software. Important processing parameters such as injection temperature, mold temperature, injection orientation etc. were analyzed.

Flip chip underfilll encapsulation was studied by Han and Wang (1997) on the forced-injection encapsulation using finite element method. Hele-Shaw technique was used to solve the flow field.

Flow behavior was investigated from the experiment using actual chip and encapsulants. Shen et al. (2001) have studied the flip chip encapsulation process using commercial software, Mold flow. Flow visualization of the processes was studied on different injection situations. Shen et al. (2006) found that the injection situation was a main factor for processing parameters. L line injection was found to be the best injection situation for underfill encapsulation of flip chip. Besides, the experimental work has been performed by Shen et al. (2004) and found that the numerical results were closer to the experiment on the flow characteristic. The material Hitachi Chemical CEL-9000-XU (LF) was used in the studies.

Commercial software Mold flow was used by Shen et al. (2001) to analyze the flip chip package on the shape and arrangement of solder ball. Taguchi method was applied by Shen et al. (2004) on the mold filling process of flip chip. Shen found that the central injection situation of flip chip was better than ¼ injection and corner injection situation. However, in another flip chip underfill encapsulation studies, Shen et al. (2006) found the inverse relationship between flow time and injection pressure. The experimental result showed that the free surface on the thickness direction was concave for the underfill encapsulation process. They also showed that the contact angles of the free surface in different injection pressures were the same and capillary effect was a main issue in the underfill flow process.

Numerical formulation with the coupled finite element method (FEM) and the volume of fluid (VOF) technique was applied in the Pantuso et al. (2003) work

on underfill encapsulation modeling. Rheologic kinetic models were used to model the material behavior. The numerical results showed the applicability of the models to the underfill encapsulation process.

On the other hand, fluid flow in the flip chip underfilling encapsulation has been studied by Kulkarni et al. (2006). Two-dimensional numerical model was built to investigate the mould filling behavior during the underfill process. Studies on polymer rheology in mold filling during encapsulation of electronic packages have been reported by Abdullah et al. (2005, 2007).

Wan et al. (2005) studied the underfill flow characteristics in flip chip encapsulation and Power-law constitutive equation was applied. Study on the injection molding in the microchip encapsulation has been reported by Han et al. (2000, 2002).

2.4 Fluid flow models of flip chip underfill

Multifarious research effort has been performed in underfill simulation for various types of flip chip package and measureable parameters. The earliest model used in simulation is Hele-Shaw approximation. In the Hele-Shaw approximation, two parallel flat plates are separated by a small distance or gap. A gapwise-averaged mass and momentum-conservation equation by neglecting the gapwise component of the flow is used in the Hele-Shaw model. The inertia effect is negligible in the assumptions of Hele-Shaw approximation because of the thickness of the model is relatively small compared to its width and length and viscous effect of fluid dominates the flow (Wai, 2003).

Hele-Shaw approximation includes continuity equation, momentum equation and energy equation. Typically, the incompressibility of fluid is taken into account in continuity equation. The momentum equation in x and y directions is obtained from continuity equation. However, in z direction, a simple uniform pressure is used for gapwise direction. For energy equation, the similar method will be applied. Normally, Hele-Shaw approximation applied in two-dimensional (2-D) modeling.

Besides Hele-Shaw approximation, another set of equations is also used to describe the flow of fluids that is Navier-Stokes equations. These equations are the fundamental partial differentials equations obtained by combining the fluid kinematics and constitutive relation into the fluid equation of motion. Navier-Stokes equations are flexible than Hele-Shaw approximation, because it can be applied either in 2-D or in 3-D purpose for underfill modeling. Application of Navier-Stokes equations in simulation could also be solved by using Finite Element Method (FEM), Finite Volume Method (FVM) and Finite Difference Method (FDM) (Abdullah, 2007).

Han and Wang (1997) developed the 3D models for numerical analysis by using finite element method based on a generalized Hele-Shaw method. The finite element method was employed to solve the flow field in underfill process. Finite element method was applied on capillary flow and force-injection encapsulation in their analysis. Fine et al. (2000) used Hele-Shaw and Washburn models for flow characteristic predictions. The modified Hele-Shaw flow was used in the underfill viscous flow between parallel plates and solder bumps by Young and Yang (2002). Estimation of the flow resistance by chip, bumps and substrate and prediction of the flow front was performed in their model. Besides, Young and Yang (2002) also

reported that the filling flow in fine pitch bumps was faster in some bump arrangements.

Pantuso et al. (2003) presented large-scale numerical models for underfill encapsulation processes. Finite element method has coupled with the volume of fluid technique and also generalized Hele–Shaw equations were included in the formulation. Besides, rheologic kinetic model was used to describe the material behavior for prediction of material bulk properties (i.e. viscosity) and reactions models during the curing process (i.e. gel time). Simulations work was presented and the applicability of the models to the underfill encapsulation process was proven.

Wan et al. (2008) has carried out experimental investigation on underfill flow driven by capillary force in flip-chip packaging. The mismatch with the Washburn model was also observed in their investigation. The experiment of results, confirmed that the underfill flow shows a complex non-Newtonian behavior and Washburn model is applicable only for Newtonian flow prediction. In addition, they also reported that the measured data on a test bed could be used to validate the theoretical findings.

Wan and Zhang (2005) had presented an analytical model for the prediction of the underfill flow characteristics in a flip-chip package driven by capillary action. A non-Newtonian fluid property was considered for the analytical model. The power-law constitutive equation was utilized in their studies. Good agreement of the simulation result as compared to other researcher experiment was obtained. This showed that the power-law model was better than Washburn model in predicting underfill flow characteristics in the flip chip packaging. Besides, various parameters such as solder bump pattern bump pitch bump diameter, gap height and process

viarables such as flow front and filling time were found to affect the flip chip package. Thus, the consideration on those parameters and variables is needed for package design and process optimization.

Shen et al. (2004) presented the analysis for flow visualization of the solder ball and chip between numerical simulation and experiment. Finite element method has been applied for simulation for three-dimensional inertia-free, incompressible flow of moving boundaries. Different injection situations which are one line injection, L line injection, U line injection and central point injection location were used in this simulation. However, different parameters such as mold temperature, injection temperature, and injection pressure and also injection time were considered for injection process. The simulation and experimental results were in good agreement.

Furthermore, Shen et al. (2006) also reported the analysis of underfill encapsulation by experiment and 3D simulation. Finite element method was applied in simulation. Four injection situations were selected, namely central point, one line, L-line, and U-line injection types. In the work, solder ball arrangement, injection pressure; solder ball size, and injection situation were used in the simulation for processing parameters. They found that the experiment of results were closer to 3D simulation results and L-Line was identified as the best underfill injection situation. Flow time was greater for alternate arrangement of solder ball and was inversely proportional to the injection pressure. Concave behavior in underfill flow was observed for free surface in the thickness direction. However, the contact angle of free surface remained constant for various injection pressures during underfill encapsulation. These results indicated that capillary effect was the main factor for flow situation in underfill process. In addition, Shen et al. (2006) emphasized the

analysis for underfill encapsulation between the solder ball and chip. The concepts and ideas presented in this work were almost similar to those discussed above. Different types of flip chip package were used in the simulation.

Kulkarni et al. (2006) had focused on fluid flow in underfilling encapsulation process. Characteristic based split (CBS) method and finite element method were used to solve the conservation equations of mass, momentum and energy and obtained the velocity and pressure profile in 2 dimensional underfill encapsulation model. Flow front was tracked by pseudo-concentration approach which based on the VOF technique. Moreover, the fluid front was tracked in each time step. Mould compound region and air region was represented by a particular value of the pseudo-concentration variable. Simulation for particular flip chip package showed a good agreement with experimental values.

2.5 Front tracking technique

Interface tracking have been solved using various techniques such as the marker-and cell (MAC), the flow-analysis-network (FAN), the VOF and the pseudo concentration methods. Typically these methods are incorporated in volume tracking method which is based on fixed mesh such as finite difference, finite element and finite volume methods. Several front tracking methods reported in previous works are presented in the following paragraph.

VOF method has been used by Nguyen et al. (1999) to track the two-phase flow field in three dimensional flow solvers. Pantuso et al. (2003) reported numerical formulation using FEM coupled with VOF technique. The VOF was used to solve the transport equation and the fluid front surface was reconstructed. FEM with VOF methods are familiar in the numerical analysis of underfill flow (Shen et al., 2004).

However, Hashimoto et al. (2007) reported numerical analysis using finite difference method (FDM) incorporating the pseudo compressibility approaches for conventional and no-flow underfill simulation. Pseudo-concentration based on VOF technique to track the fluid front for each time step has been reported by Kulkarni et al. (2006) in their numerical simulation of underfill encapsulation process based on characteristic split method (CBS).

2.6 Cross viscosity model

Cross viscosity is one of the rheological models that have been used for modeling the fluid behavior in polymer rheologies in the change of viscosity. Verhoyen and Dupret (1998) introduced the Cross viscosity for injection moulding process to analyze the influence of the polymer viscosity on the flow. Besides, the Cross model can be used without involving higher computational cost during the calculations. Cross viscosity model has been taken into account by Rahman et al. (2008) for injection moluding simulation analysis with the aid of Moldflow software. The investigation was focus on injection moulding process for window frame fabrication. Zdanski and Vaz Jr. (2009) reported the investigation on sudden expansion of polymer melt flow. In their investigation, the generalized Newtonian fluid was taken consideration into simulation and Cross viscosity model was applied for fluid behavior modeling. The relationship between viscosity-shear rate and the operational shear rate ranges of several rheometers and polymer processing operation as shown in Figure 2.2 were reported by Laney and Reilly (1998). Cross viscosity model has been used by Chang et al. (2004) in modeling the fluid flow of mould filling for microchip encapsulation process. The epoxy molding compound is assumed as the generalized Newtonian fluid.