DEVELOPMENT OF SPACER FREE SELF-ALIGNED CONTACT IMPLANTATION FOR POWER DEVICES

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DEVELOPMENT OF SPACER FREE SELF-ALIGNED CONTACT IMPLANTATION FOR POWER DEVICES

by

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DECLARATION

I declare that this is a result of my own research and does not contain any materials previously published, written or produced by another person except where due reference is made in the text. All the sources in this thesis are totally PRIVATE and CONFIDENTAL.

Sign : _____
Candidate's Name :
Date :

Witness : _____
Sign :
Supervisor's Name :
Date :

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LIST OF SYMBOLS & ABBREVIATIONS

BJT	Bipolar junction transistor
BPSG	Borophosphosilicate Glass
BSG	Boro-silicate glass
C_{DS}	Drain-to-source capacitance
C_{GD}	Gate-to-drain capacitance
C_{GS}	Gate-to-source capacitance
Ciss	Input capacitance
Coss	Output capacitance
Crss	Reverse transfer capacitance
CoolMOS	Cool- Metal-oxide-semiconductor field-effect transistor
CVD	Chemical Vapour Depostion
D-MOSFET	Depletion -Metal-oxide-semiconductor field-effect transistor
DOE	Design of experiment
E-MOSFET	Enhancement- Metal-oxide-semiconductor field-effect transistor
FT	Functional Test
GTO	Gate-turn-off thyristors
HCI	Hydrochloride acid
HDPCVD	High-density plasma chemical vapor deposition
HF	Hydroflouric acid
H_2	Hydogen flow
IGBT	Insulated gate bipolar transistor
LPCVD	Low Pressure Chemical Vapour Deposition
LTO	Low temperature oxide

MOS	Metal-oxide-semiconductor
MOSFET	Metal-oxide-semiconductor field-effect transistor
O_2	Oxygen
P++	Contact (Boron)
PCM	Process Control Monitoring
POSA MOS	Polysilicon oxidation self-aligned MOS
$POC1_3$	Phosphorus oxygen chloride
PSG	Phosphosilitcate Glass
Q_{DS}	Drain-to-source charge
Q_{GD}	Gate-to-drain charge
Q_{GS}	Gate-to-source charge
R_a	Accumulation resistance
R_B	Base Resistance
RCT	Reverse-conducting thyristors
Rc (M1/N+/P++)	Contact resistance- metal/source/contact
Rc (M1/P++)	Contact resistance -metal/contact
Rc (M1/S1)	Contact resistance-metal/ polysilicon
R_{ch}	Channel resistance
R_{DS}(on)	Drain to source resistance (on)
R_{epi}	"JFET" component-resistance of the region between the two body regions, drift region resistance
R_n	Source diffusion resistance
R_s	Source contact resistance
Rs (N+/P++)	Sheet resistance- source/contact
Rs (S1)	Sheet resistance-polysilicon
Rs (P++/P-)	Sheet resistance-contact /body

Rs (P++)	Sheet resistance- contact
R_{sub}	Substrate resistance
R_{wcml}	Sum of bond wire resistance, the contact resistance between the source and drain metallization and the silicon, metallization and leadframe contributions. These are normally negligible in high voltage devices but can become significant in low voltage devices
RTA	Rapid thermal annealing
R_{TH}	Thermal impedance
SiO_2	Silicon dioxide
SOI	Silicon-on-insulator
SJ	Super junction
TEOS	Tetraethylorthosilicate
$TiSi_2$	Titanium disilicide
USG	Undoped Silicate Glass
UPS	Uninterruptible power supplies
V_{BE}	Base to emitter voltage
V_{DS}	Drain-to-source voltage
V_{GS}	Gate to source voltage
V_{TH}	Threshold voltage
SEM	Scanning Electron Microscope
STD	Standard

PEMBANGUNAN KONSEP MENJAJARKAN PENIMPALAN KONTAK BAGI TRANSISTOR KUASA TINGGI

ABSTRAK

Mengoptimasi skema proses integrasi bagi sesebuah teknolgi merupakan salah satu faktor penting untuk mengurangkan bilangan kecatatan dan kitaran masa dalam bidang fabrikasi wafer. Dalam pengajian sarjana ini, aliran proses yang dioptimasi bagi menjajarkan penimpalan kontak telah dikaji bagi teknologi Infineoen CoolMOS. Selepas mengaji 3 idea yang berlainan dengan insentif, konsep yang paling berpotensi tinggi dipilih bagi pengoptimasian dan pencirian lanjutan di peringkat wafer dan poduk. Teknologi pada masa kini menggunakan dinding-tepi penjarakan, di mana ia dibentuk melalui taburan silikon dioksida dan diikuti oleh pengoressan oxida bukan isotropik bagi membentuk lubang penimpalan kontak. Dalam konsep pertama dan kedua, oksida polisilikon dan kaca silikate tanpa dop (USG) masing-masing digunakan untuk menggantikan penjarakkan and menjalankan penimpalan kontak. Penghadan peralatan fabrikasi dan pengaruh terhadap percirian wafer menyebabakan konsep-konsep ini tidak dapat dilaksanakan sepenuhnya dalam pengeluaran. Konsep ketiga menjalankan skema pengintegrasian tanpa penjarakkan dinding tepi. Penimpalan kontak dijalankan selepas proses pengoressan kontak lubang polisilikon. Dengan mengaplikasikan konsep ini, sebilangan langkah proses boleh disingkirkan. serta bilangan kecatatan dalam wafer dan kitaran masa untuk menfabrikasikan sesuatu transistor boleh dikurangkan. Pencirian insentif peringkat wafer dan produk mendedahkan 1:1 yang cirinya bersesuian dengan pretasi produk konsep asal serta pertimbangan khas telah diberikan bagi menganalisakan parameter transistor seperti rintangan keadaan aktif, voltan permulaan dan pengaliran arus. Kesemua keputusan telah dibentangkan and dibincangkan dengan teliti bagi memaparkan potensi baik konsep baru ini.

DEVELOPMENT OF SPACER FREE SELF-ALIGNED CONTACT IMPLANTATION FOR POWER DEVICES

ABSTRACT

Optimization of the process integration scheme for a technology is one of the key factors within wafer fabrication in order to reduce defect density and production cycle time. Within this master study, an optimized process flow for the self-aligned contact implantation was evaluated for the Infineons CoolMOS technology. After intensive feasibility investigations of 3 different ideas, the most promising concept was further optimized and characterized on wafer level as well as in the final product. The current technology utilizes side-wall spacers, which are formed by deposition of silicon dioxide followed by an anisotropic oxide etched prior to contact-hole implantation. Within the first and second concept, the original spacer process block spacer was replaced with an alternative spacer fabricated by oxidation of the gate polysilicon and deposition of undoped silicate glass (USG), respectively. Limitations of certain fabrication tools as well as influences on the device characteristics did not allow these concepts to be executed in the production. The third and the most promising concept facilitates contact implantation after the polysilicon contact hole-etch process. By applying this concept, a number of process steps can be removed, which as a consequence greatly reduces the frontend defect density of the wafer as well as cycle time to fabricate the transistor. Intensive characterization of wafer and dies revealed a 1:1 match to the current product performance and special consideration has been given on the analysis of the transistor parameters, such as ‘on resistance’, ‘threshold voltage’ and ‘transconductance’. The results are presented and discussed clearly showing the potential of the new concept.

CHAPTER 1

INTRODUCTION

1.1 Project Introduction

Semiconductor power devices are electronic components used as rectifiers or switches in electronic circuits. A majority of these devices are made of silicon however other materials, such as silicon carbide is under development. With the development of power semiconductor technology, the power handling capabilities and the switching speed of the power devices have improved tremendously (Spulber *et al.*, 1999).

Semiconductor power devices can be divided widely into three types; which are diodes, transistors and thyristors. A diode is a two-terminal pn-junction device and it serves three purposes: (1) general purpose diodes, (2) high speed (or fast recovery) diodes and (3) Schottky diodes. General purpose diodes are used in low-speed applications whereas fast-recovery diodes are essential for high-frequency switching. Schottky diodes have low on-state voltage and very small recovery time (Muhammad, 2004).

A thyristor has three terminals, which are an anode, a cathode and a gate. The thyristors can be divided into many types, such as line-commutated thyristors, gate-turn-off thyristors (GTO), reverse-conducting thyristors (RCT) and others. Conventional thyristors are designed without gate-controlled turn-off capability, in which the conducting state of the thyristor can be recovered from its nonconducting

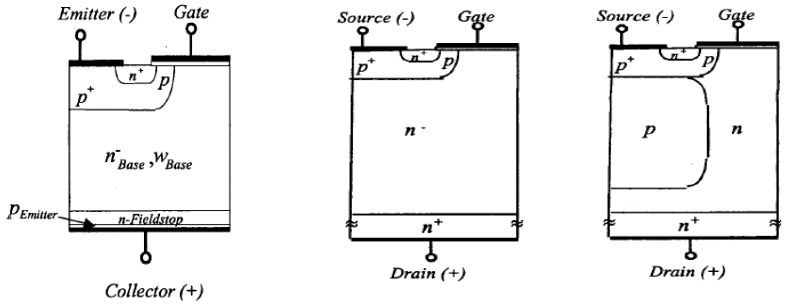
state when the current is brought to zero by other means. GTOs are designed to have both controlled turn-on and -off capability. Thyristors have lower on-state conduction losses and higher power handling capability compared to transistors.

On the other hand, transistors generally have superior switching performances in terms of faster switching speed and lower switching losses. Some common power transistors are metal-oxide-semiconductor field-effect transistor (MOSFET), bipolar junction transistor (BJT) and insulated gate bipolar transistor (IGBT). Generally, transistors are built using a vertical structure; whereas lateral structure is used for small-signal applications. BJT is a current-controlled device, in which amount of collector current is controlled by base current. An IGBT is inherently faster than BJT. However, the switching speed of IGBTs is inferior to that of MOSFETs (Appendix 1.1).

The two basic types of MOSFET are depletion (D) and enhancement (E) MOSFET. The D-MOSFET operates in the depletion or enhancement mode whereas the E-MOSFET only operates in the enhancement mode and has no depletion mode. N-channel MOSFET operates in depletion mode when a negative gate-to-source voltage is applied and when a positive gate-to-source voltage is applied, an enhancement mode is obtained. For an n-channel MOSFET, the channel is induced by the application of a gate to source voltage, V_{GS} greater than the threshold value, V_{TH}. Power transistors are designed to achieve higher current, voltage and power capability by creating shorter channel between drain and source.

In this project, COOLMOS 600V have been used in the evaluations. CoolMOS virtually combines the low switching losses of a MOSFET with the low on-state losses of an IGBT (Figure 1.1) (Muhammad, 2004). In comparison with classical MOS

structure, CooLMOS, incorporates two additional p- columnar layers sandwiched between n-type drift regions. The on-resistance could be reduced by a factor of 5 in comparison to the classical device due to the super-junction formation. This is achieved by controlling the charge between the p- and n-type layers in such a way that the n-type doping concentration is increased beyond the upper limit set by the breakdown voltage considerations of a conventional power MOSFET (Lorenz *et al.*, 1999).



(a) (b) (c)

Figure 1.1: Cross section of conventional (a) Field-stop IGBT, (b) D-MOSFET and (c) CoolMOS (Deboy *et al.*, 1998).

A sufficient contact between source and drain is crucial for the functioning of these devices. A widely used concept to achieve this is to align the contact implantation on the polysilicon gate and source region through a spacer formed by Tetraethylorthosilicate (TEOS)-based silicon dioxide and followed by an anisotropic etch of the oxide. For n-type transistors this contact implantation is also referred to P++ implantation.

The advantage of having a spacer is to avoid an additional photolayer which is required to align the contact implantation away from the channel region. Additionally, the spacer is able to effectively isolate the contact implantation from the channel area

(Figure 1.2) and that is why the concept is also referred to self-aligned contact implantation. This means that they prevent dopants from diffusing under the gate during the implantation of the highly doped source regions and affects the device performance. The shallow diffused P++ surface below the source region helps to reduce the P-base sheet resistance and its contact resistance (Shenai,1992)[a]. With the spacer concept, the base length (R_{base}) of the transistor inherent parasitic bipolar structure can be minimized to the outer most extent. Thus, no latch-up phenomenon within the specified safe operating area of the transistor will be occurred (Deboy *et al.*, 1998).

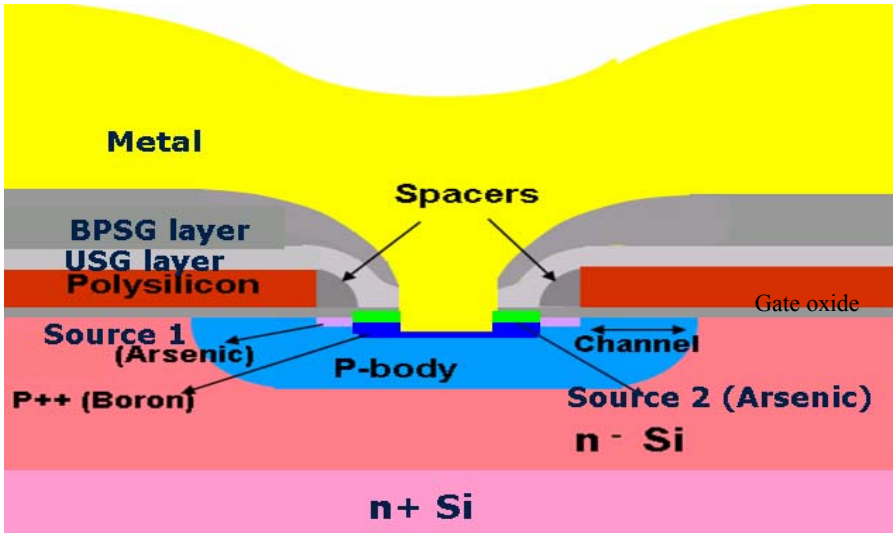


Figure 1.2: Cross section of power transistor device (Trobin W, 2005)

1.2 Problem Statement

Structure of power devices are often modified to make them operate at higher current density and lower on resistance. In this thesis, electrical and dynamic results of power transistors fabricated without using sidewall spacers have been reported. Side

wall spacers are formed by TEOS based silicon dioxide and followed by anisotropic etch of the oxide. The advantage of this concept without spacer is that no additional photolayer for the alignment is needed. However, relatively thick spacer oxide, which is formed by TEOS based oxide deposition may increase defect density of the product and rather extensive maintenance of the tool is required.

In the past, DMOSFET cells with shallow p+ diffusion have been demonstrated using a polysilicon mask (Nakagawa *et al.,* 1986) and Phosphosilitcate Glass (PSG) spacers (Mori *et al.*, 1988) to block boron implant. However, these approaches lead to degradation of cell packing density, complex processing, and poor wafer yield. To reduce the gate resistance and to improve the source contact resistance, refractory metal/silicide technologies have been used (Shenai *et al.* 1989 [a] ,Shenai *et al.* 1989 [b] ,Shenai *et al.* 1989 [c]). Spacers are made by dry etching, which happens much faster in the vertical direction (depth) than in the lateral directions. Since the TEOS-based silicon dioxide layer is thicker next to the gate electrodes, it will take much longer time to etch it. If the etching is stopped once the silicon wafer is reached, TEOS-based silicon dioxide will still be left next to the gate electrodes. These are the oxide spacers.

The built of spacers involves many processes, such as TEOS-based silicon dioxide deposition, anisotropic etch of TEOS-based silicon dioxide, furnace anneal and various cleaning steps. These processes eventually increase the possibility of defect density during the production run. Besides, the quality of the deposited oxide is not that good; a densification is required. Starting with the 250 nm technology node, the oxide spacers become unsuitable for three reasons, which are field oxide loss, high thermal budget and oxide spacers are vulnerable. The part of the field oxides is also lost during

the dry etch step. The dopants, implanted in the source extensions module, will diffuse deeper into the silicon wafer as a consequence of heating (densification, re-oxidation etc.) This is unacceptable in small technology nodes, whereby very small source extensions are required. When a process step or module involves a lot of heating it is said to have a high thermal budget. Moreover, oxide spacers are vulnerable to HF dips. Unfortunately such HF dips are necessary during consecutive process steps. Each HF dip reduces the spacer further. The spacer block removal eliminates spacer subsequent process steps such as anisotropic plasma etch, furnace anneal, various cleans from the production process. The spacer removal enables implantation combination in a single process. This eventually achieves self-aligned contact implantation, optimize costs and defect density at Infineon's production site in Kulim.

Therefore, three concepts have been developed in order to replace this spacer process and eliminate its subsequent process steps from the production process. The elimination of these processes eventually optimizes the production costs of wafers. After a string of pre-evaluations for these three concepts, the most promising concept is chosen to perform the self-aligned contact implantation. The novel concept describes the new behaviour of the electrical, dynamic characterization and avalanche ruggedness. Special consideration has been given on the analysis of the transistor parameters, such as 'on resistance', 'threshold voltage' and 'transconductance' The concept undergoes well planned production runs, simulations and extensive characterization in order to achieve self-aligned contact implantation, optimize costs and defect density at Infineon's production site in Kulim.

1.3 Objectives

The main objective is to introduce a new concept of self-aligned contact implantation for Infineon power devices. The goal of this project is to eliminate side wall spacers by process modification and utilization of existing layer in the fabrication process. The concepts are formulated to create a kind of spacer from part of gate silicon.

The designs of experiments have been carried out to accomplish the following proposed objectives:

- To eliminate TEOS-based silicon dioxide side wall spacers, which are formed by Low Pressure Chemical Vapour Deposition (LPCVD) and followed by anisotropic etch.

- By removing spacer block, other subsequent process steps which form spacer are taken away from the production process. The subsequent process are anisotropic plasma etch, furnace anneal, and various cleans.

- To combine Source 1 and Source 2 implantation in a single process and attain a matching device performance with respect to standard device performance.

1.4 Scope of the Project

The scope of the project is to fabricate power transistors with the elimination of TEOS-based silicon dioxide sidewall called spacers. The project examines three different concepts used to replace spacer and its subsequence process steps from the production process. The first concept replaces side wall spacers by polysilicon oxide, whereas the second concept describes the usage of self-aligned Undoped Silicate Glass (USG) as self-aligned spacers and finally the third concept comprises contact implantation into contact hole structure that has been built during the device fabrication. The barriers of the concepts into realization and the most promising concept will be discussed in the results and discussion section.

Some important considerations are taken into account as the concepts above are performed. The designs of experiments are constructed based on these considerations. The first concept is to grow oxide on the polysilicon layer by polysilicon oxidization. This oxide growth functions as self aligned spacers and even as a dielectric layer, which could eventually remove USG deposition layer. The topology of oxide growth on top of polysilicon is examined. The experiment investigates the drawbacks of this concept as high thermal budget and duration is required in order to grow oxide layer on the polysilicon. The other considerations, such as influence of high thermal on other properties, especially arsenic diffusion on source region are analyzed via simulation tool.

The second concept, whereby USG deposition on polysilicon which functions as dielectric layer are used as self-aligned spacers despite of TEOS-based silicon dioxide

spacers. The implantation energy required for P++ contact (Boron) penetration into USG layer and source region is analyzed with a professional simulation tool. Various implantation energy have been used accordance to USG depth. The influence of contact implantation with varied USG side wall width are investigated as it would eventually increases the effective boron concentration on the channel and affects the electrical parameters of the device.

In the third concept, the contact implantation is facilitated into the contact hole. The design of experiments are carried out to implant P++ on different process, which are after contact hole with resist and contact hole without resist. The suitable process for P++ implantation is determined. Contact implantation together with the adaptation of the source implantation and diffusion conditions are required to attain a matching device performance with standard device. Other considerations such influence on contact hole trench etch specification and misalignment of contact hole overlay are taken into account.

By removal of TEOS-based silicon dioxide deposition process, other subsequence processes such as etch, annealing and cleaning processes can also be taken away from the current flow. Besides, the TEOS-based silicon dioxide spacer elimination enables the merge of Source 1 and Source 2 in a single process. Several wafer level simulations and tests such as ICECREM simulation, Process Control Monitoring (PCM), Functional Test (FT), cross sections, reliability and avalanche test are conducted in Kulim Infineon. In PCM test, the parameters given consideration are P++ contact resistance, sheet resistance and polysilicon sheet resistance. On the other hand, parameters on the threshold voltage, on resistance and transconduction are given

priority in FT test. Devices performance and reliability for the most promising concept is evaluated based on the electrical characterization and avalanche capability. Chip level assembly is done Malacca Infineon and full characterization is carried out in Munich, Germany.

1.5 Outline of the thesis

This thesis is divided into 5 main chapters, whereby Chapter 2 details the relevant literature review of the project and Chapter 3 briefs on the methodology of the project. Chapter 4 comprises the front end electrical results, cross sections and simulation results which are obtained from the performed design of experiments. In addition and chip level full electrical characterization has also been included. In this chapter, the results are displayed and discussed. Finally, Chapter 5 presents the conclusion and recommendations to further improvise the research work.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Chapter 2 describes the power transistor CoolMOS basics, spacer fabrication and function, polysilicon oxidation, dielectric layer deposition, ion implantation and diffusion on the source region. In the CoolMOS basics section, structure principles of operation, static characteristics, dynamic characteristics, device ruggedness and applications are discussed. The subtopics such as spacer and polysilicon oxidation elaborate the spacer and polysilicon oxidation fabrication process. In addition, the dielectric layers deposition method especially Undoped Silicate Glass (USG) and Borophosphosilicate Glass (BPSG) layers are also been detailed. The related journals on the P++ implantation and arsenic implantation on the source region are included in the chapter as well. Generally this chapter reviews the related journals, articles and literature on the project work.

2.2 CoolMOS Basics

2.2.1 Structure

The super junction (SJ) device concept is gaining interests for high voltage power devices applications (Chen *et al.*,1991; Tihanyi *et al.*,1995; Coe, 1998; Fujihira,1997). The conceptual structure was realized later on, and it was called the

CoolMOS or super junction MOSFET (Lorenz *et al.*, 1999; Deboy *et al.,* 1998). The SJ-MOSFET or CoolMOS broke the limitation in reducing conduction resistance and has 5- 100 times lower specific on-resistance than conventional high voltage MOSFETs (Lorenz *et al.*, 1999). Moreover, the majority carrier current conduction causes the switching performance of the CoolMOS is like that of a conventional MOSFET. Unlike the IGBT, CoolMOS exhibits no tail current at turn-off. The CoolMOS virtually combines the low switching losses of a MOSFET with the on-state losses of an IGBT. Many studies on the static breakdown voltage of the CoolMOS have been published (Spulber *et al.,* 1999; Lorenz *et al.*, 1999; Deboy *et al.*,1998).

In the CoolMOS device, the drift region of the conventional power MOSFET is replaced by a "superjunction," or known as a combination of n and p strips in parallel (Lorenz *et al.*, 1999; Deboy *et al.*,1998) as shown in Figures 2.1 and Figure 2.2. The device concept is generated based on charge compensation in the drift region of the transistor (Deboy *et al.*,1998). The doping of the vertical drift region is roughly increased by one order of magnitude and this counterbalances additional charge by the implementation of fine structured columns of the opposite doping type. However, the blocking voltage of the transistor remains unchanged. The charge compensating columns do not add to the current conduction during the turn-on state. Nevertheless the radically increased doping of the drift region allows the above mentioned reduction of the on-resistance.

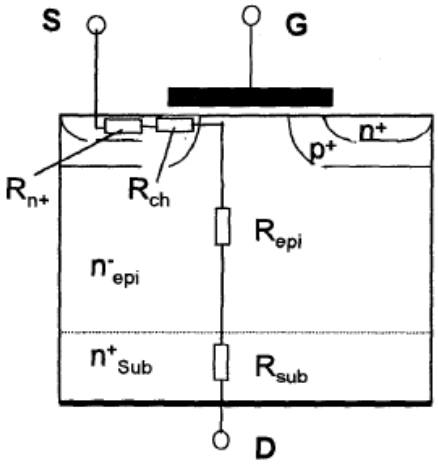


Figure 2.1: State of the art 600 V-MOSFET with series of resistance (Deboy *et al.*,1998)

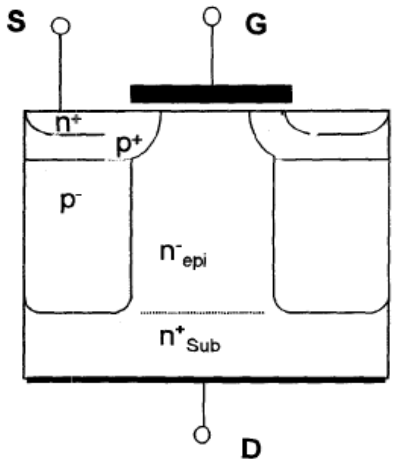


Figure 2.2: Cross Section of a 600V- CoolMOS with p-n columns (Deboy *et al.*,1998)

2.2.2 Principles of Operation

2.2.2.1 On state

During on state, electrons flow from the source, under the gate electrode (through the CoolMOS channel), through the drift region (the n part of the superjunction), to the drain terminal (Figure 2.3). Therefore the device is considered to be made up of an "intrinsic" MOSFET and a drift region. It requires a gate voltage more positive than V_{TH} to create an electron channel. At the threshold voltage of the "intrinsic" MOSFET, the device turns on and the current rises with initially in addition saturates when the resistance of the drift region starts dominating. As drain-to-source voltage (V_{DS}) increases, the inversion-layer charge density at the drain end of the channel is reduced and therefore drain current (I_D) does not increase linearly with V_{DS}. When V_{DS} reaches $V_{GS}-V_{TH}$, the channel is "pinched off" at the drain end, and I_D

saturates (it does not increase with further increases in V_{DS}) (Figure 2.4) (Barkhordarian , 2009).

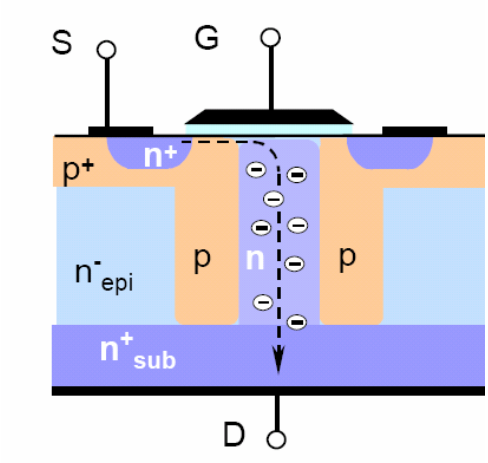


Figure 2.3: Electrons flow from the source of the CoolMOS high voltage power MOSFET (Lorenz *et al.*, 1999)

During turn-on the space charge layer is removed in both devices by the injection of electrons through the channel region. The CoolMOS requires additionally the diffusion of holes from the p-well into the p-column. A good ohmic contact is therefore required (Lorenz *et al.*, 1999).

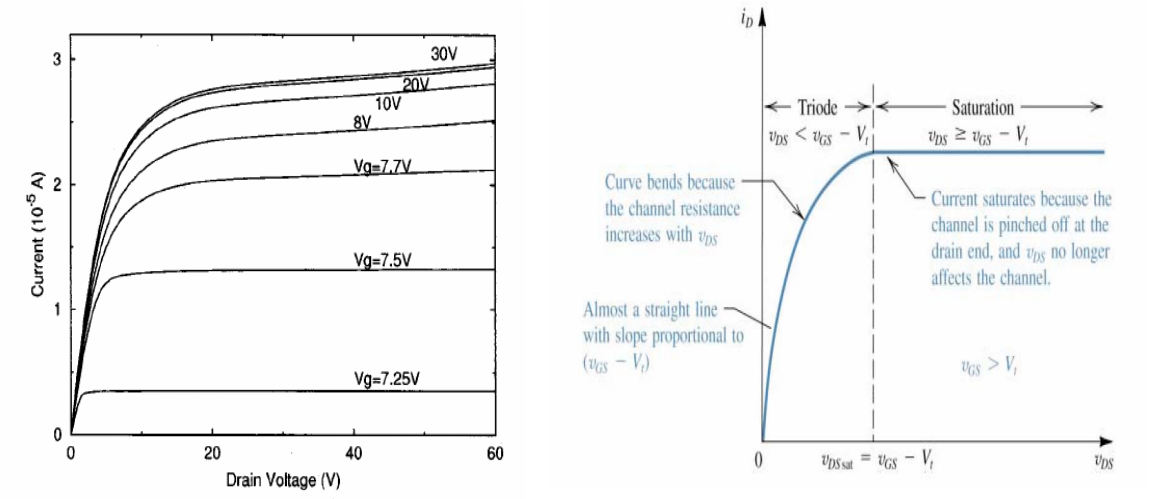


Figure 2.4: Output characteristics of the CoolMOS transistor (Daniel *et al.*, 2002)

2.2.2.2 Off state

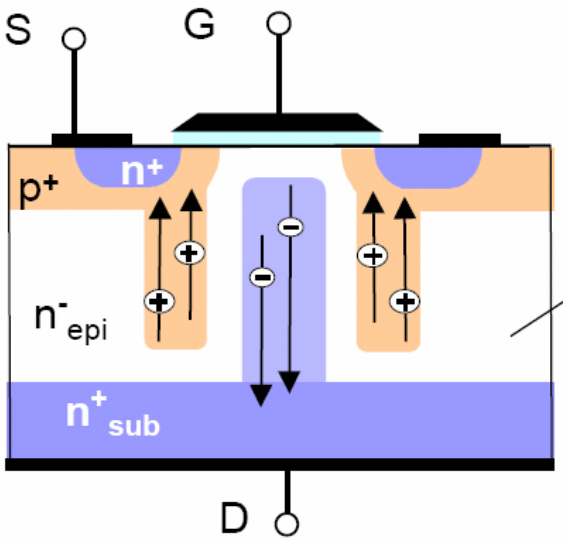


Figure 2.5: Current flow during turn-off in a CoolMOS device (Lorenz *et al.*, 1999)

Without a gate-to-source voltage applied, no current can flow between the source and drain regions. The CoolMOS depletes completely at very low voltages without current flow through high field regions (Figure 2.5) (Lorenz *et al.*, 1999).

2.2.3 Static Characteristics

2.2.3.1 On-resistance

The resistance of the voltage sustaining in drift zone rules the on-resistance of a conventional high voltage power MOSFET. The thickness and doping level on the epi layer determines the blocking capability of this drift region. The layer thickness must be increased and the doping level must be simultaneously reduced in order to increase the blocking voltage. The resistance of the transistor therefore increases disproportionately strongly as a function of its blocking capability (Figure 2.6) (Lorenz *et al.*, 1999). Accordingly the drift zone causes over 95 % of the total on resistance for example in a

600-V transistor. The main emphasis in improving the transistors performance must therefore be directed towards reducing this drift region resistance (Lorenz *et al.*, 1999).

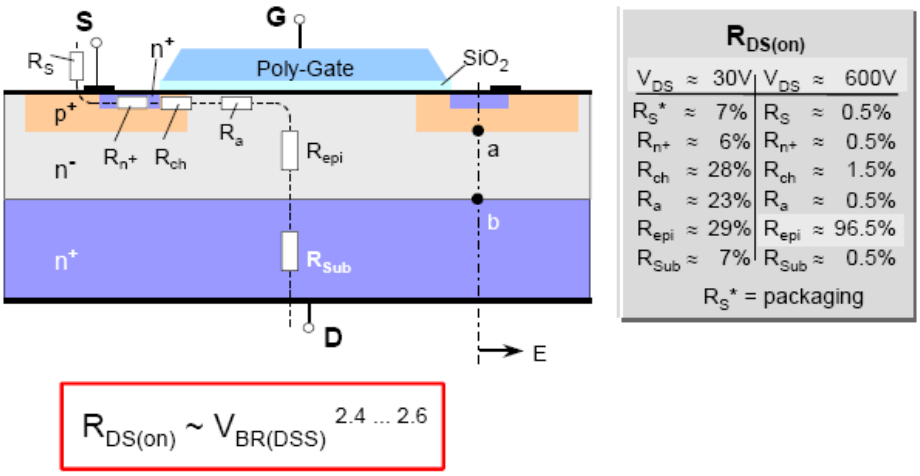


Figure 2.6: Components of the overall $R_{DS}(on)$ in conventional power MOSFETs for low and high voltage devices (Lorenz *et al.*, 1999)

The on-state resistance of a power MOSFET is made up of several components as shown in Figure 6:

$$R_{DS}(on)=R_S+R_n+R_{ch}+R_a+R_{epi}+R_{sub}+R_{wcml} \quad (1)$$

where:

R_s = Source contact resistance
R_n= Source diffusion resistance
R_{ch} = Channel resistance
R_a = Accumulation resistance
R_{epi} = "JFET" component-resistance of the region between the two body regions, drift region resistance
R_{sub} = Substrate resistance
R_{wcml} = Sum of bond wire resistance, the contact resistance between the source and drain metallization and the silicon, metallization and leadframe contributions. These are normally negligible in high voltage devices but can become significant in low voltage devices.

Figure 2.7 shows the relative importance of each of the components to R_{DS}(on) over the voltage spectrum. The figure shows the epi resistance and JFET component dominates the R_{DS}(on) at high voltages. This element is higher in high voltage devices due to the higher resistivity or lower background carrier concentration in the epi. The R_{DS} (on) is dominated by the channel resistance and the contributions from the metal to semiconductor contact, metallization, bond wires and leadframe at lower voltages. At lower breakdown voltage devices, the substrate contribution becomes more significant (Barkhordarian , 2009).

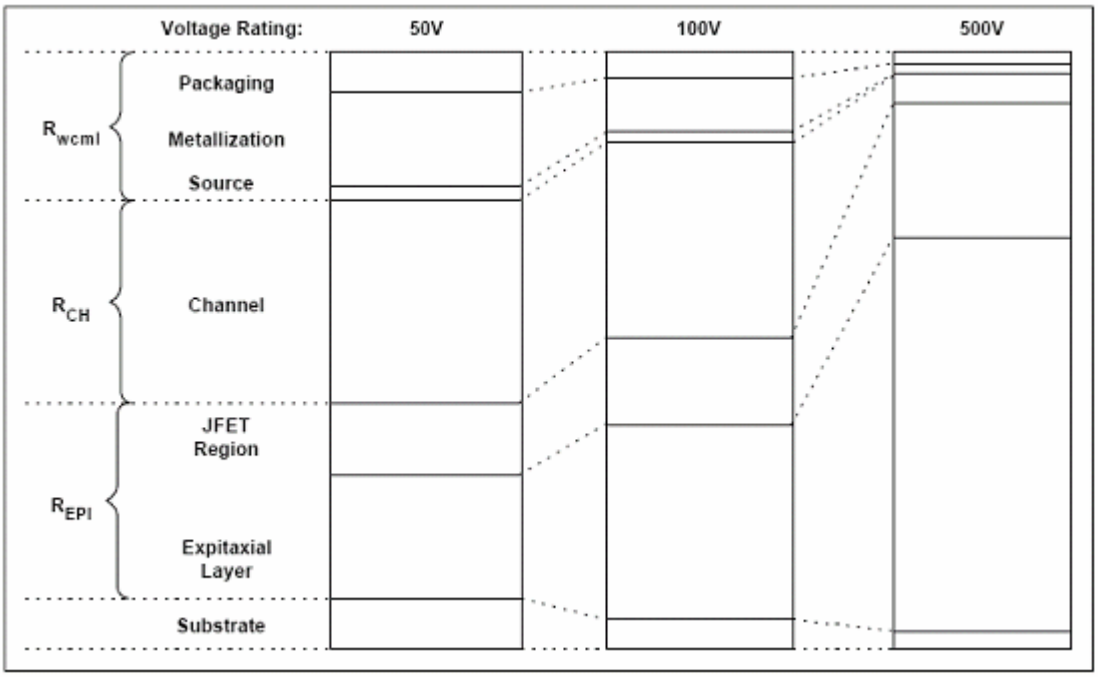


Figure 2.7: Relative contributions to R_{DS}(on) with different voltage ratings (Barkhordarian, 2009)

2.2.3.2 Breakdown voltage

B_{VDSS} , is the voltage at which the reverse-biased body-drift diode breaks down and significant current starts to flow between the source and drain by the avalanche multiplication process, while the gate and source are shorted together (Barkhordarian, 2009). The drain voltage is entirely supported by the reverse-biased body-drift p-n junction and no channel is formed under the gate at the surface for drain voltages below B_{VDSS} and with no bias on the gate. Poorly designed and processed devices cause two phenomena: punch-through and reach-through. Punch through is observed as the depletion region on the source side of the body-drift p-n junction reaches the source region at drain voltages below the rated avalanche voltage of the device. This contributes soft breakdown characteristics which provide a current path between source and drain. The leakage current flowing between source and drain is denoted by I_{DSS}. Therefore, a tradeoffs to be made between R_{DS} (on) that requires shorter channel lengths and punch-through avoidance that requires longer channel lengths. On the other hand, as the depletion region on the drift side of the body-drift p-n junction reaches the epilayer-substrate interface before avalanching takes place in the epi, the reach-through phenomenon occurs. Once the depletion edge enters the high carrier concentration substrate, a further increase in drain voltage will cause the electric field to quickly reach the critical value where avalanching begins (Barkhordarian, 2009).

The doping of the current conducting n-regions can be enhanced inverse proportional to their width (Deboy *et al.*, 1998). The electric field inside the structure is fixed by the net charge of the two opposite doped columns and thus a nearly horizontal field distribution can be achieved if both counterbalance each other perfectly. For

higher blocking voltages only the depth of the columns has to be increased without the necessity to alter the doping. This leads to a linear re1ationship between blocking voltage and on-resistance (Figure 2.8). By using this technique, 1000 V CoolMOS will offer a R_{DS} (on) reduction in the range of one order of magnitude versus conventional technologies.

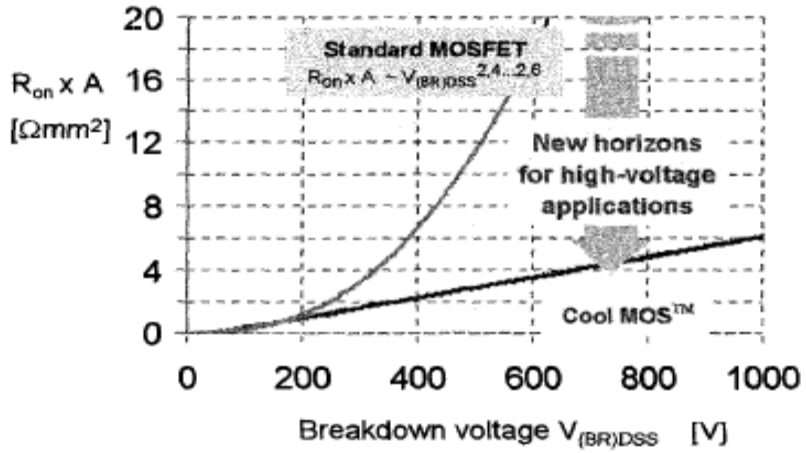


Figure 2.8: COOLMOS technology offers a linear relationship between blocking voltage and on-resistance (Deboy *et al.*, 1998)

2.2.3.3 Transconduction

Transconductance is a measure of the sensitivity of drain current to changes in gate-source bias. This parameter is normally quoted for a V_{GS} that gives a drain current equal to about one half of the maximum current rating value and for a V_{DS} that ensures operation in the constant current region. The gate width influences transconductance, which increases in proportion to the active area as cell density increases. The photolithography process control and resolution is the limiting factor for even higher cell densities that allows contacts to be made to the source metallization in the center of

the cells. Channel length also affects transconductance. Reduced channel length is beneficial to both gfs and on-resistance, with punch-through as a tradeoff. Finally, the lower the gate oxide thickness, the higher is the transconduction (Barkhordarian , 2009).

2.2.3.4 Threshold voltage

Threshold voltage, V_{TH}, is defined as the minimum gate electrode bias required to strongly invert the surface under the poly and form a conducting channel between the source and the drain regions. V_{TH} is usually measured at a drain-source current. Common values are 2-4V for high voltage devices with thicker gate oxides, and 1-2V for lower voltage, logic-compatible devices with thinner gate oxides. The trend is toward lower values of R_{DS}(on) and V_{TH} are useable in portable electronics and wireless communications where battery power is at a premium (Barkhordarian, 2009).

2.2.3.4 Dynamic characteristics

As the CoolMOS is used as a switch, its basic function is to control the drain current by the gate voltage. The time required to establish voltage changes across capacitances determines the switching performance of a device. Typical values of input (Ciss), output (Coss) and reverse transfer (Crss) capacitances given in the data sheets are used by circuit designers as a starting point in determining circuit component values (Figure 2.9). The datasheet capacitances are defined in terms of the equivalent circuit capacitances as:

$$Ciss = C_{GS} + C_{GD}, C_{DS} \text{ shorted} \quad (2)$$
$$Crss = C_{GD} \quad (3)$$
$$Coss = C_{DS} + C_{GD} \quad (4)$$

Gate-to-drain capacitance, C_{GD}, is a nonlinear function of voltage and it provides a feedback loop between the output and the input of the circuit. C_{GD} is also known as the Miller capacitance because it causes the total dynamic input capacitance to become greater than the sum of the static capacitances. Figure 2.10 shows a typical switching time test with the components of the rise and fall times with reference to the V_{GS} and V_{DS} waveforms. The time taken to charge the input capacitance of the device before drain current conduction can start is referred as turn-on delay, td (on). Similarly, turn-off delay, td (off), is the time taken to discharge the capacitance after it is switched off (Barkhordarian, 2009).

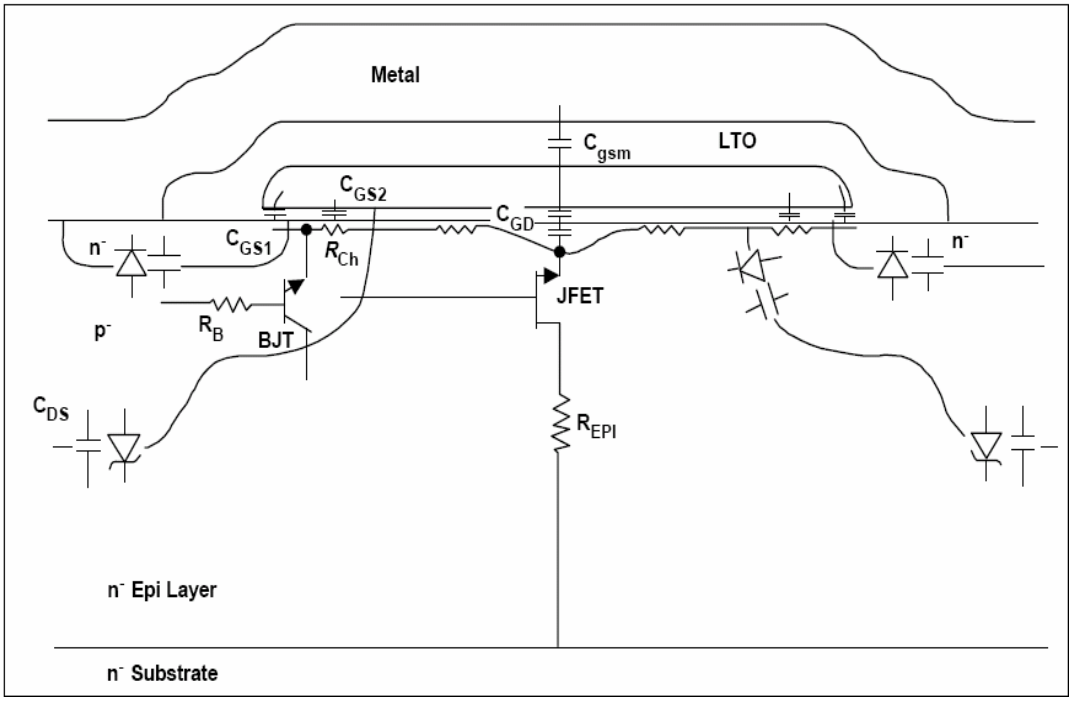


Figure 2.9: Power MOSFET Parasitic Components (Barkhordarian, 2009).

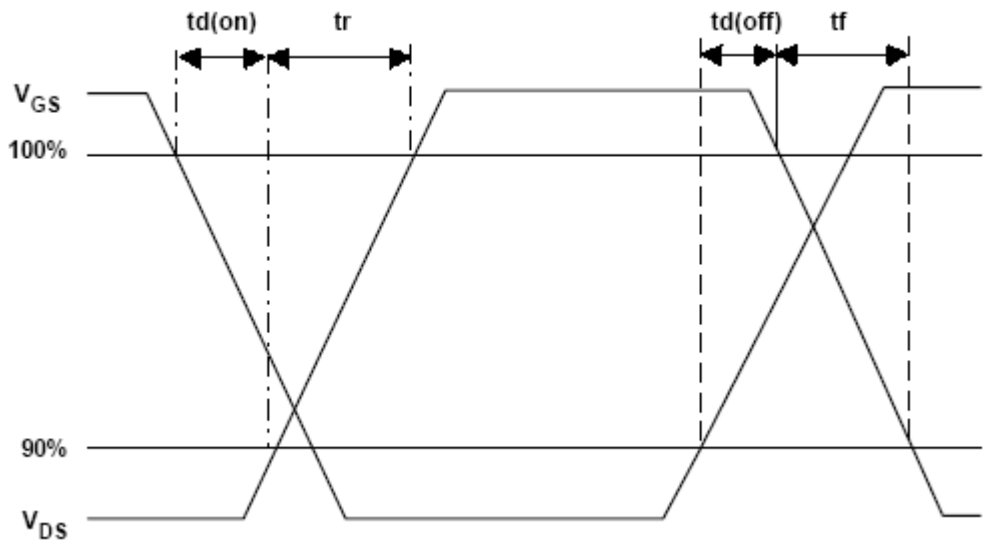


Figure 2.10: Switching Time Test V_{GS} and V_{DS} Waveforms (Barkhordarian , 2009).

2.2.3.5 Switching behavior

Input capacitance values normally do not provide precise results when comparing the switching performances of two devices from different manufacturers. A more helpful parameter from the circuit design point of view is the gate charge rather than capacitance. V_{GS} starts to increase until it reaches V_{TH}, the drain current starts to flow and the C_{GS} starts to charge. During the period t_1 to t_2 (Figure 2.11), C_{GS} continues to charge, the gate voltage continues to rise and drain current rises proportionally. At time t_2, C_{GS} is completely charged and the drain current reaches the preset current I_D and stays constant while the drain voltage starts to drop. Figure 2.11 shows the reference to the equivalent circuit model of the MOSFET and it explains that with C_{GS} fully charged at t_2, V_{GS} becomes constant and the drive current starts to charge the Miller capacitance, C_{GD}. This goes on until time t_3.

The Miller capacitance charge time is larger than that for the gate to source capacitance C_{GS} due to the rapidly changing drain voltage between t_2 and t_3 (current = Cdv/dt). As soon as both of the capacitances C_{GS} and C_{GD} are fully charged, gate voltage (V_{GS}) starts increasing again until it attains the supply voltage at time t_4. Time t_3 is corresponding to the gate charge (Q_{GS} + Q_{GD}) which is bare minimum charge required to switch the device on. The use of a higher gate voltage than the bare minimum required for switching is recommended in a good circuit design practice and therefore the gate charge used in the calculations is Q_G corresponding to t_4. The benefit of using gate charge is that the designer without difficulty calculate the amount of current required from the drive circuit to switch the device on in a desired length of time because Q = CV and I = C dv/dt, the Q = Time x current. For example, a device with a gate charge of 20 nC can be turned on in 20 μs if 1ma is supplied to the gate or it can turn on in 20 ns if the gate current is increased to 1 A. These simple calculations would not have been probable with input capacitance values (Barkhordarian, 2009).

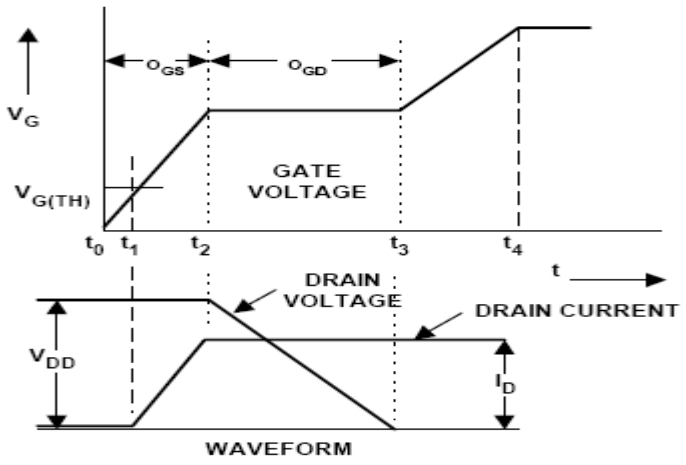


Figure 2.11: Gate Charge Test, (b) Resulting Gate and Drain Waveforms (Barkhordarian, 2009).

The characteristic output capacitance displays the nonlinear spread of the space charge layer as a function of voltage. Its main contribution is the drain/source capacitance (Figure 2.12). The significantly increased internal surface of the pn-junction cause the capacitance illustrates large values at small voltages. As the internal p/n-striped structure starts to deplete, both the reduction of this surface and the expansion of the space charge layer width lead to a strongly nonlinear performance of the output capacitance (Lorenz *et al.*, 1999).

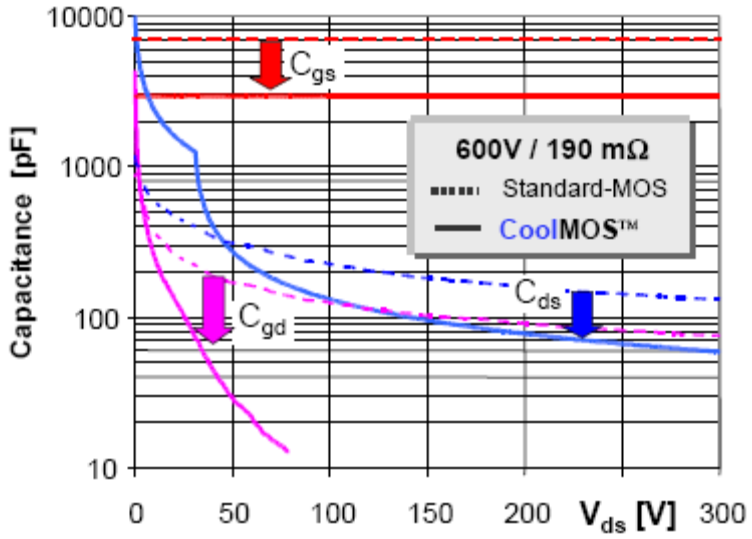


Figure 2.12: CoolMOS offers a substantial reduction of gate-source and "Miller" capacitance, C_{GS} and C_{GD} respectively, as well as a very favourable nonlinear behavior of the drain-source capacitance C_{GD}.(Lorenz *et al.*, 1999)

2.2.3.6 Device Ruggedness

From the customer's viewpoint, device ruggedness is an essential criteria. CoolMOS transistors propose an avalanche energy per chip area which is very close to the thermal limit of zener clamped devices. A self aligned spacer technology is used to