Second Semester Examination
2017/2018 Academic Session

May/June 2018

EEE348 – INTRODUCTION TO INTEGRATED CIRCUIT DESIGN
(PENGANTAR REKABENTUK LITAR BERSEPADU)

Duration : 3 hours
(Masa : 3 jam)

Please ensure that this examination paper consists of THIRTEEN (13) pages and appendix ONE (1) pages of printed appendix material before you begin the examination.

[Sila pastikan bahawa kertas peperiksaan ini mengandungi TIGA BELAS (13) muka surat dan SATU (1) muka surat lampiran yang bercetak sebelum anda memulakan peperiksaan ini.]

Instructions: This question paper consists of **FIVE (5)** questions. Answer **ALL** questions. All questions carry the same marks.

[***Arahan:*** *Kertas soalan ini mengandungi* ***LIMA (5)*** *soalan. Jawab* ***SEMUA*** *soalan. Semua soalan membawa jumlah markah yang sama.]*

In the event of any discrepancies, the English version shall be used.

[Sekiranya terdapat sebarang percanggahan pada soalan peperiksaan, versi Bahasa Inggeris hendaklah digunapakai.]

1. (a) In integrated circuit (IC) design, there are several design implementation choices providing different trade-off points.

Dalam rekabentuk litar bersepadu (IC), terdapat beberapa pilihan implementasi rekabentuk yang memberi kelebihan/kekurangan yang berbeza.

(i) Draw a chart of digital circuit implementation approaches in integrated circuit design.

Lukis satu carta pilihan implementasi litar digital dalam Rekabentuk Litar Bersepadu (IC).

(16 marks/*markah*)

(ii) Draw a general design flow in cell-based design implementation approach.

Lukis satu carta alir umum dalam kaedah implementasi rekabentuk berasaskan sel.

(14 marks/*markah*)

(iii) Field Programmable Gate Arrays (FPGAs) can be grouped into three (3) main categories based on the implementation technology: fuse-based FPGAs, non-volatile memory-based FPGAs, and volatile memory-based FPGAs. Discuss the differences as well as provide one (1) advantage and one (1) disadvantage of these FPGA technologies.

Field Programmable Gate Array (FPGA) boleh dibahagikan kepada tiga (3) kategori utama berdasarkan teknologi implementasi: FPGA berasaskan fius, FPGA berasaskan memori tak kekal, dan FPGA berasaskan memori kekal. Bincangkan perbezaan serta berikan satu (1) kelebihan dan satu (1) kelemahan ketiga-tiga teknologi FPGA ini.

(20 marks/*markah*)

(b) Semiconductor memories can be classified into two (2) main categories: Random Access Memory (RAM) and Read Only Memory (ROM).

Memori semikonduktor boleh diklasifikasikan kepada dua kategori utama: Random Access Memory (RAM) dan Read Only Memory (ROM).

(i) List down different types of ROM-based Memory.
Senaraikan jenis-jenis memori berasaskan ROM.

(12 marks/*markah*)

(ii) Describe major differences between Static RAM (SRAM) and Dynamic RAM (DRAM).

Terangkan perbezaan utama antara Static RAM (SRAM) dan Dynamic RAM (DRAM).

(12 marks/*markah*)

(iii) With **appropriate diagrams and a truth table**, describe the design and the operation of a 2-bit row address decoder of a NOR-based ROM to select one of four (2^2) Word Lines (WL).

*Dengan **gambarajah-gambarajah yang sesuai dan satu jadual kebenaran,** terangkan rekabentuk dan operasi 2-bit dekoder lajur alamat dalam suatu ROM berasaskan logik NOR untuk memilih salah satu daripada empat (2^2) garis kata.*

(26 marks/*markah*)

2. (a) Figure 2.1 shows a stick diagram of the Pull-Up Network (PUN) of a CMOS logic circuit.

Rajah 2.1 menunjukkan gambarajah lidi bagi Rangkaian Tarik-Naik (PUN) suatu litar logik CMOS.

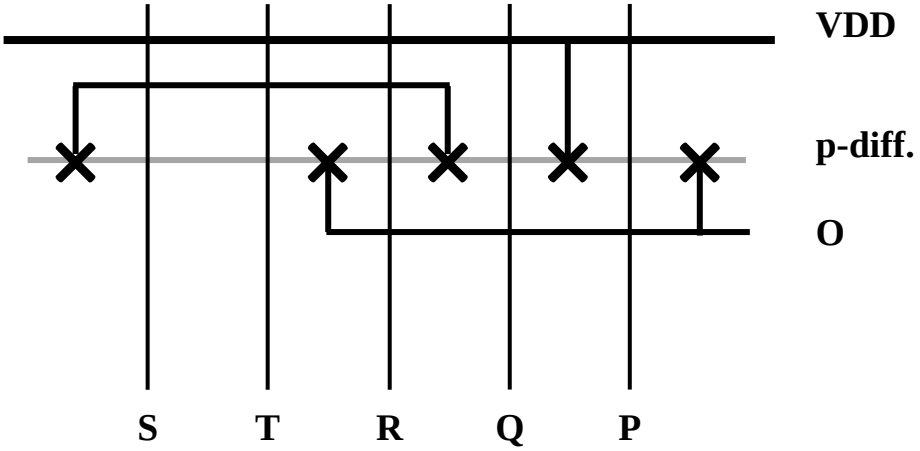

Figure 2.1: Stick diagram of PUN of a CMOS logic circuit

Rajah 2.1: Gambarajah lidi bagi PUN suatu litar logik CMOS

(i) Draw the corresponding transistor-level schematic consisting of Pull-Up Network (PUN) and Pull-Down Network (PDN).

Lukis litar skema peringkat transistor yang terdiri daripada Rangkaian Tarik-Naik (PUN) dan Rangkaian Tarik-Bawah (PDN).

(20 marks/*markah*)

(ii) Derive the Boolean logic function for the output O.

Terbitkan fungsi logik Boolean bagi output O.

(6 marks/*markah*)

(iii) Complete the PDN section for the given stick diagram.

Lengkapkan bahagian PDN bagi gambarajah lidi yang diberikan.

(14 marks/*markah*)

(b) Figure 2.2 shows a stick diagram of the Pull-Up Network (PUN) of a CMOS logic circuit using a random polysilicon ordering.

Rajah 2.2 menunjukkan gambarajah lidi bagi Rangkaian Tarik-Naik (PUN) suatu litar logik CMOS menggunakan susunan rawak polisilikon.

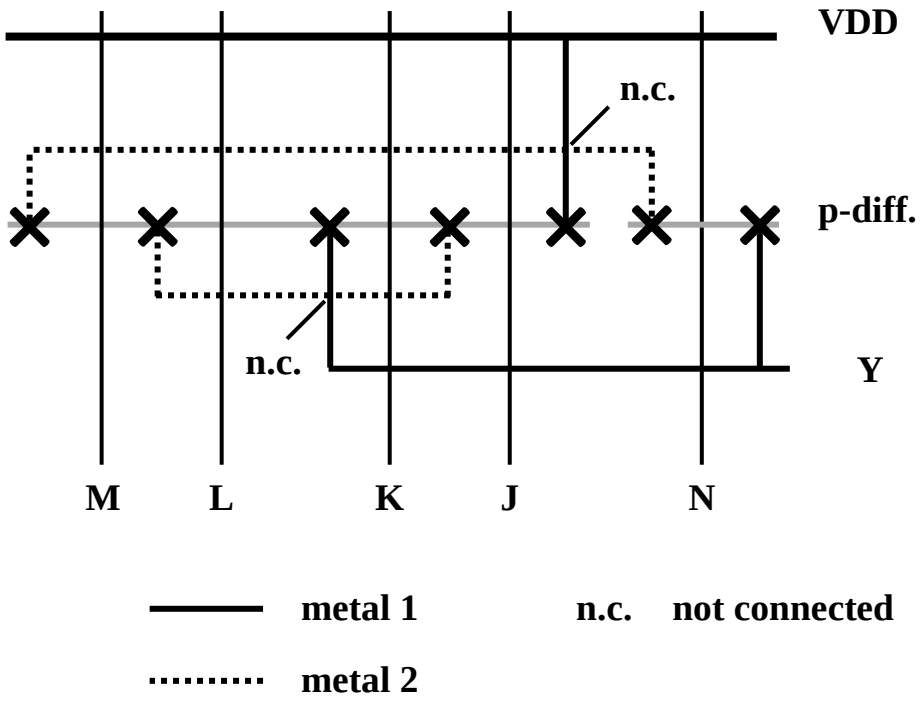

Figure 2.2: Stick diagram of PUN of a CMOS logic circuit

Rajah 2.2: Gambarajah lidi bagi PUN suatu litar logik CMOS

(i) List three (3) disadvantages of random polysilicon ordering in CMOS layout.

Senaraikan tiga (3) kelemahan susunan rawak polisilikon dalam susun atur CMOS.

(6 marks/*markah*)

(ii) Draw the corresponding transistor-level schematic consisting of Pull-Up Network (PUN) and Pull-Down Network (PDN).

Lukis litar skema peringkat transistor yang terdiri daripada Rangkaian Tarik-Naik (PUN) dan Rangkaian Tarik-Bawah (PDN).

(20 marks/*markah*)

(iii) Derive the Boolean logic function for the output Y.
Terbitkan fungsi logik Boolean bagi output Y.

(6 marks/*markah*)

(iv) Find a common Euler path for both PUN and PDN for an optimum gate ordering.

Cari satu laluan Euler yang sama bagi kedua-dua PUN dan PDN bagi susunan get yang optimum.

(8 marks/*markah*)

(v) Draw a complete stick diagram based on the found Euler path in (iv).

Lukis satu gambarajah lidi lengkap berdasarkan laluan Euler yang dijumpai dalam (iv).

(20 marks/*markah*)

3. The CMOS technology consists of 2 types of transistors, the nMOS and pMOS that is fabricated in a single substrate. Hence the process suits for logic circuit design and fabrication.

Teknologi CMOS terdiri daripada 2 jenis transistor iaitu pMOS dan nMOS yang difabrikasi dalam satu substrat tunggal. Maka, proses ini adalah bersesuaian untuk rekabentuk dan fabrikasi litar logik.

(a) Draw the schematic of a 2-input NAND gate that consist of nMOS and pMOS.

(20 marks/*markah)*

Lukis gambarajah skematik get logik NAND 2-input yang mengandungi nMOS dan pMOS.

(b) Illustrate, **via proper diagrams** the NAND gate operation for each input condition tabulated in the truth table below.

(40 marks/*markah)*

Lukis gambarajah-gambarajah operasi get NAND untuk setiap keadaan input yang dipaparkan dalam jadual kebenaran di bawah.

A	B	Y
0	0	
0	1	
1	0	
1	1	

(c) Figure 3 below illustrates the Top View of an inverter.

Rajah 3 di bawah mengambarkan pandangan atas satu penyongsang.

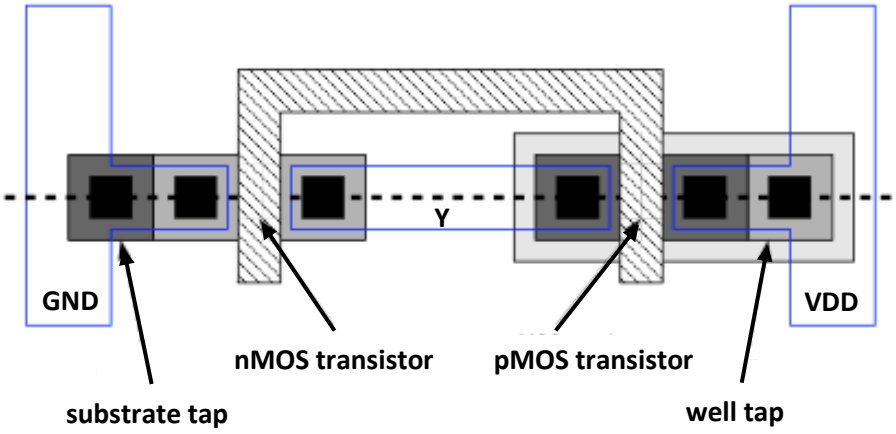

Figure 3

Rajah 3

(i) Draw the schematic for the layout above.

Lukis gambarajah litar untuk susun atur di atas.

(10 marks/*markah*)

(ii) Draw and the label the Cross Section of the inverter along the dashed line

(30 marks/*markah)*

Lukis dan labelkan keratan rentas penyongsang di sepanjang garis putus yang ditunjukkan dalam rajah di atas.

4. (a) Consider following Verilog modules. Draw the waveform for the input signal CLK and the output signal OUT.

Diberi modul-modul Verilog seperti berikut. Lukis gambarajah gelombang untuk isyarat masukan CLK dan juga isyarat keluaran OUT.

```
module q4a(out, clk, rst, in0, in1);
   output out;
   input clk, rst;
   input [3:0] in0, in1;
   wire  a, b;

  sub1 m1(a, clk, rst, in0);
  sub1 m2(b, clk, rst, in1);
  sub2 m3(out, a, b);

endmodule

module sub1(out, clk, rst, in);
   output out; reg out;
   input clk, rst;
   input [3:0] in;
   reg [3:0] t1, t2, t3;
   reg x, y;
```

```
always @(posedge clk)
   begin
   if (rst == 0)
   t1 <= in;
   t2 <= t1;
   t3 <= t2;
   end

always @(t3)
            begin
            x = t1<=t2;
            y = t2<=t3;
            case({x,y})
               2'b11: out = 1'b1;
               default: out = 1'b0;
            endcase
            end

endmodule

module sub2(out, a, b);
output out;
input  a, b;

assign out = a & b;
endmodule

module tb_q4a;
   wire OUT;
   reg CLK, RST;
   reg [3:0] IN0, IN1;
```

…10/-

```
q4a dut(OUT, CLK, RST, IN0, IN1);

always
  #1 CLK = ~CLK;

initial begin
   CLK = 0; RST = 1;
   #2 IN0 = 10; IN1 = 9;
   #2 IN0 = 8; IN1 = 5; RST = 0;
   #2 IN0 = 4; IN1 = 3;
   #2 IN0 = 2; IN1 = 1;
   #2 IN0 = 1; IN1 = 3;
   #2 IN0 = 9; IN1 = 14;
   #2 IN0 = 4; IN1 = 11;
   #2 IN0 = 2; IN1 = 9;
   #2 IN0 = 4; IN1 = 11;
   #2 $stop;
end

endmodule
```

(80 marks/*markah*)

(b) Design a digital circuit based on following specification using Verilog HDL.

(i) There are two inputs (***in1*** and ***in2***). Each of the inputs is an integer number in the range of 0 to 15.

(ii) An output ***out*** is equal to 1 when ***in1*** is equal to ***in2*** and both inputs are even numbers. Otherwise ***out*** will be equal to 0.

(iii) You have to use the concept of connection of gates and no need to write the test bench.

Rekabentuk sebuah litar digital berdasarkan spesifikasi berikut dengan menggunakan Verilog HDL.

(i) *Terdapat dua masukan (**in1** dan **in2**). Setiap masukan adalah nombor integer di antara 0 hingga 15.*

(ii) *Keluaran **out** adalah bersamaan dengan 1 apabila **in1** adalah sama dengan **in2** dan kedua-dua masukan adalah nombor genap. Selain daripada itu **out** adalah bersamaan dengan 0.*

(iii) *Anda dikehendaki menggunakan konsep "connection of gates" dan tidak perlu menulis "test bench".*

(20 marks/*markah*)

5. (a) Design a digital circuit based on following specification using Verilog HDL. You have to use the concept of connection of instances for the top level module, where the top level module only consists of the instances of low level module. As for the low level module, you may use any type of description. You need to develop also the test bench to verify the designed circuit. No need to test all combinations.

The circuit has an input ***t***, where ***t*** is an integer number in the range of 0 to 15. An output ***out*** is based on following conditions:-

If $0 \leq t \leq 3$, ***out*** = ***t***
If $4 \leq t \leq 7$, ***out*** = 2***t***
If $8 \leq t \leq 11$, ***out*** = 4***t***
If $12 \leq t \leq 15$, ***out*** = 8***t***

Rekabentuk sebuah litar digital berdasarkan spesifikasi berikut dengan menggunakan Verilog HDL. Anda dikehendaki menggunakan konsep "connection of instances" untuk modul peringkat atasan, yang mana modul peringkat atasan hanya mengandungi beberapa "instances" bagi modul peringkat bawahan. Untuk modul peringkat bawahan, anda boleh menggunakan mana-mana jenis deskripsi. Anda juga dikehendaki membangunkan "test bench" untuk mengesahkan litar yang telah direka. Tidak perlu untuk membuat pengesahan untuk kesemua kemungkinan.

Litar tersebut mempunyai satu masukan ***t****, di mana* ***t*** *adalah nombor integer di antara 0 hingga 15. Keluaran* ***out*** *adalah berdasarkan situasi berikut:-*

Sekiranya $0 \leq$ ***t*** ≤ 3, ***out*** = ***t***
Sekiranya $4 \leq$ ***t*** ≤ 7, ***out*** = 2***t***
Sekiranya $8 \leq$ ***t*** ≤ 11, ***out*** = 4***t***
Sekiranya $12 \leq$ ***t*** ≤ 15, ***out*** = 8***t***

(80 marks/*markah*)

(b) Consider following Verilog modules. Determine the values of OUT in decimal at simulation time of 0, 1, 2 and 3.

Diberi modul-modul Verilog seperti berikut. Tentukan nilai bagi OUT di dalam desimal pada waktu simulasi 0, 1, 2 dan 3.

```
module q5b(out, a, b, seq);
   output [2:0] out;
   reg [2:0] out;
   input [1:0] a, b;
   input [3:0] seq;
   wire [1:0] cnt;
   always @(cnt)
        case(cnt)
```

```
                3: out = a * 2;
                2: out = a + 2;
                1: out = b + 2;
                0: out = b * 2;
                default: out = a;
        endcase
    assign cnt = (seq[3]&seq[2]) + (seq[2]&seq[1]) + (seq[1]&seq[0]);
endmodule

module tb_q5b;
   wire [2:0] OUT;
   reg [1:0] A, B;
   reg [3:0] SEQ;

   q5b dut(OUT, A, B, SEQ);
   initial begin
        A = 2 ; B = 3;
        SEQ = 4'b1111;
     #1 SEQ = 4'b0111;
     #1 SEQ = 4'b1010;
     #1 SEQ = 4'b0110;
     #1  $stop;
   end
endmodule
```

(20 marks/*markah*)

Course Outcomes (CO) – Programme Outcomes (PO) Mapping

Pemetaan Hasil Pembelajaran Kursus – Hasil Program

Questions ***Soalan***	**CO**	**PO**
1	1	1
2	1	1
3	2	1
4	3	1
5	3	1
6	-	-