Second Semester Examination
2017/2018 Academic Session

May / June 2018

EEE 552 – SIGNAL INTEGRITY FOR HIGH SPEED DIGITAL DESIGN

Duration : 3 hours
[Masa : 3 jam]

Please ensure that this examination paper consists of **TWELVE (12)** pages and **TWO** pages of printed appendices material before you begin the examination.

Instructions: This question paper consists of **FIVE (5)** questions. Answer **ALL** questions. All questions carry the same marks.

You are not allowed to take this question paper out of the examination hall.

1. (a) A transmission line is often modelled as an RLGC distributed circuit.

(i) Explain why is it necessary to distribute the RLGC parameters compared to lumping them into single elements.

(2 marks)

(ii) Explain the difference between what is modelled by the R and the G.

(2 marks)

(iii) A lossless transmission line is designed to have a characteristic impedance of 50 Ω on a material with a dielectric constant of 4.

(iii.i) Calculate the per-unit length capacitance and inductance of this line.

(3 marks)

(iii.ii) If the rise time of the signal is 500 ps, what is the minimum number of segments that is needed to model a 10 cm long transmission line? (Note that the delay of an LC segment of a transmission line is given by $\sqrt{LC}$.)

(3 marks)

(b) A transmission line setup and its corresponding bounce diagram is shown in Figure 1. Based on the information given:

(i) Calculate the value of the load impedance Z_L. (1 marks)

(ii) Calculate the value of the source impedance Z_S. (1 marks)

(iii) Calculate the value of the source voltage V_S. (1 marks)

(iv) Sketch the transient response at $z = 3l/4$ for $t = 0$ to $t = 3$ ns. (4 marks)

(v) If Z_L is replaced with a 50 Ω resistor, sketch the new bounce diagram and the corresponding transient response at $z = 3l/4$ for $t = 0$ to $t = 3$ ns. (3 marks)

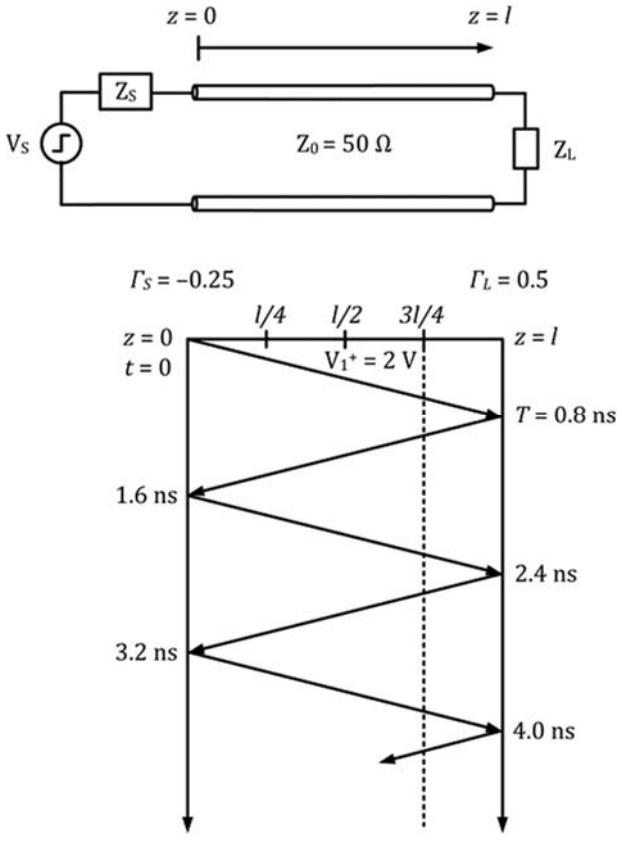


Figure 1

2. (a) Calculate the *S*-parameters for the circuit shown in Figure 2.1. Assume a reference impedance of 50 Ω.

(4 marks)

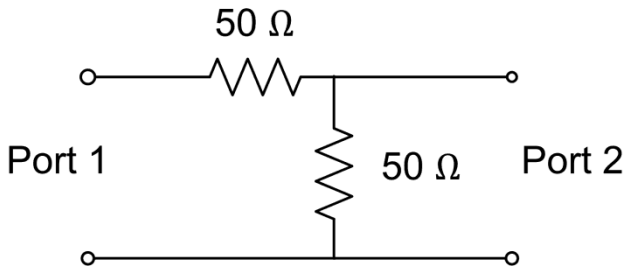


Figure 2.1

(b) A 2-port, 50 Ω network analyzer is used to measure the S-parameters of a 50 Ω transmission line by connecting port-1 and port-2 to each ends of the line.

(i) What is the magnitude of S_{11}? (1 marks)

(ii) If the S_{11} (magnitude and phase) is plotted on a Smith Chart, how will it look? Explain in words or sketch a picture.

(2 marks)

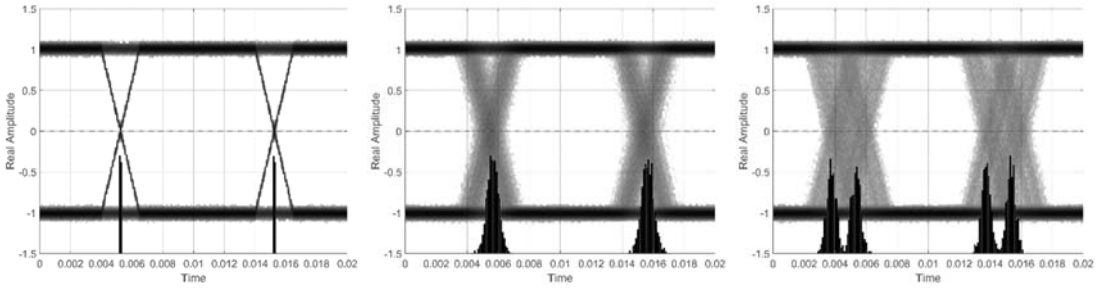
(iii) If port-2 of the network analyzer is disconnected and the S_{11} is remeasured:

(iii.i) What is the new magnitude of S_{11}? (1 marks)

(iii.ii) If the new S_{11} (magnitude and phase) is plotted on a Smith Chart, how will it look? Explain in words or sketch a picture.

(2 marks)

(c) The eye diagrams (and the histogram at the eye crossings) of three different high-speed systems are shown in Figure 2.2. Based on the information provided, comment on the specific differences between the three systems.

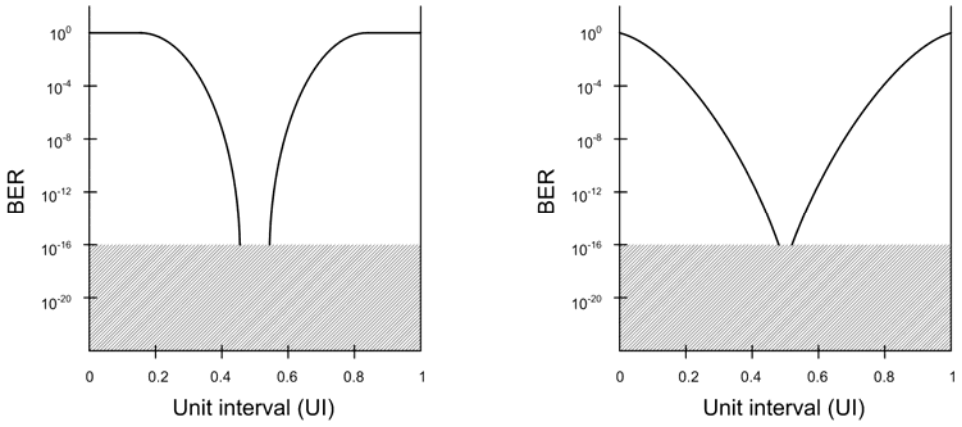


System A System B System C

Figure 2.2

(4 marks)

(d) The bathtub curves of two different high-speed systems are shown in Figure 2.3.



System X System Y

Figure 2.3

(i) For a target BER of 10^{-12}, which system will perform better? Why?

(2 marks)

(ii) From the shape of the bathtub curve, what is the specific difference between the two systems?

(2 marks)

(iii) Explain why the data in the shaded regions of the bathtub curves are not available. How is this normally obtained for high-speed systems?

(2 marks)

3. Figure 3 shows the cross section of coupled microstrip transmission lines.

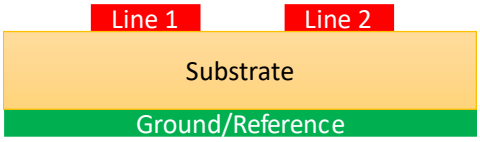


Figure 3

Given the extracted inductance and capacitance matrixes of the structure as,

$$L = \begin{bmatrix} 10.2 & 3.3 \\ 3.3 & 10.2 \end{bmatrix} nH/in \quad C = \begin{bmatrix} 4.02 & -0.35 \\ -0.35 & 4.02 \end{bmatrix} pF/in$$

(i) Draw an equivalent circuit and write the corresponding transmission line equations for a lossless system of an incremental length Δz.

(7 marks)

(ii) Determine the characteristic impedance and propagation delay for odd modes.

(2 marks)

(iii) Determine the characteristic impedance and propagation delay for even modes.

(2 marks)

(iv) Design a π termination technique for odd and even modes. Please show an odd mode and even mode equivalent circuit.

(3 marks)

(v) Define odd-mode and even-mode propagation modes.

(2 marks)

(vi) Assume there is no coupling in differential signaling, find the differential impedance and common mode impedance.

(2 marks)

(vii) List two advantages and disadvantages of differential signaling.

(2 marks)

4. Figure 4.1 is a schematic representation of complex receiver front end with an equalizer and an FEC.

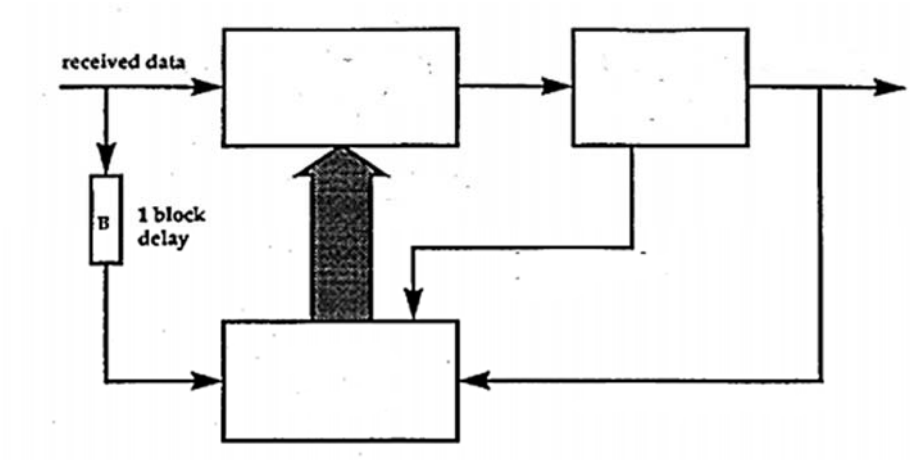


Figure 4.1

(a) From Figure 4.1, identify two blocks that the equalizer and the FEC can be placed in.

(4 marks)

(b) From Figure 4.1, identify three possible feedback loops and explain the impact of feedbacks to the receiver front end design.

(3 marks)

(c) What kind of equalizer is used here and what are its main features?

(2 marks)

(d) Figure 4.2 shows a typical operation of an equalizer in the time domain. From the figure, explain the functionality of the equalizer and what it intends to do in terms of ISI?

(3 marks)

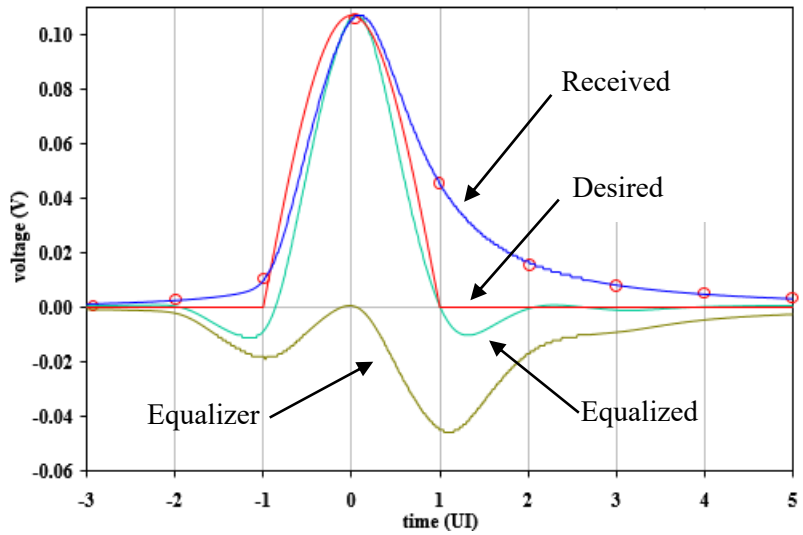


Figure 4.2

(e) How many taps can we utilize in Figure 4.2 to make an effective equalizer and how many are typically used in real life applications?

(5 marks)

(f) From the ZFS optimizing algorithm matrix in Figure 4.3, if N=5, how many tap coefficients can we expect in the design.

(3 marks)

$$\begin{bmatrix} h_0 & 0 & 0 & . & . & . & 0 \\ h_1 & h_0 & 0 & . & . & . & 0 \\ h_2 & h_1 & h_0 & 0 & . & . & 0 \\ . & . & . & . & . & . & . \\ . & . & . & . & . & . & . \\ h_{N_E-1} & h_{N_E-2} & . & . & h_1 & h_0 & 0 \\ h_{N_E} & h_{N_E-1} & . & . & . & h_1 & h_0 \\ . & . & . & . & . & . & h_1 \\ 0 & . & . & . & . & . & . \\ 0 & 0 & . & . & . & h_{N_C-1} & h_{N_C-2} \\ 0 & 0 & 0 & . & . & 0 & h_{N_C-1} \end{bmatrix} \begin{bmatrix} w_0^* \\ w_1^* \\ . \\ . \\ . \\ . \\ . \\ w_{N_E-1}^* \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ . \\ 0 \\ 1 \\ 0 \\ . \\ 0 \end{bmatrix}$$

Figure 4.3

5. (a) For a typical 4-layer desktop motherboard in Figure 5.1

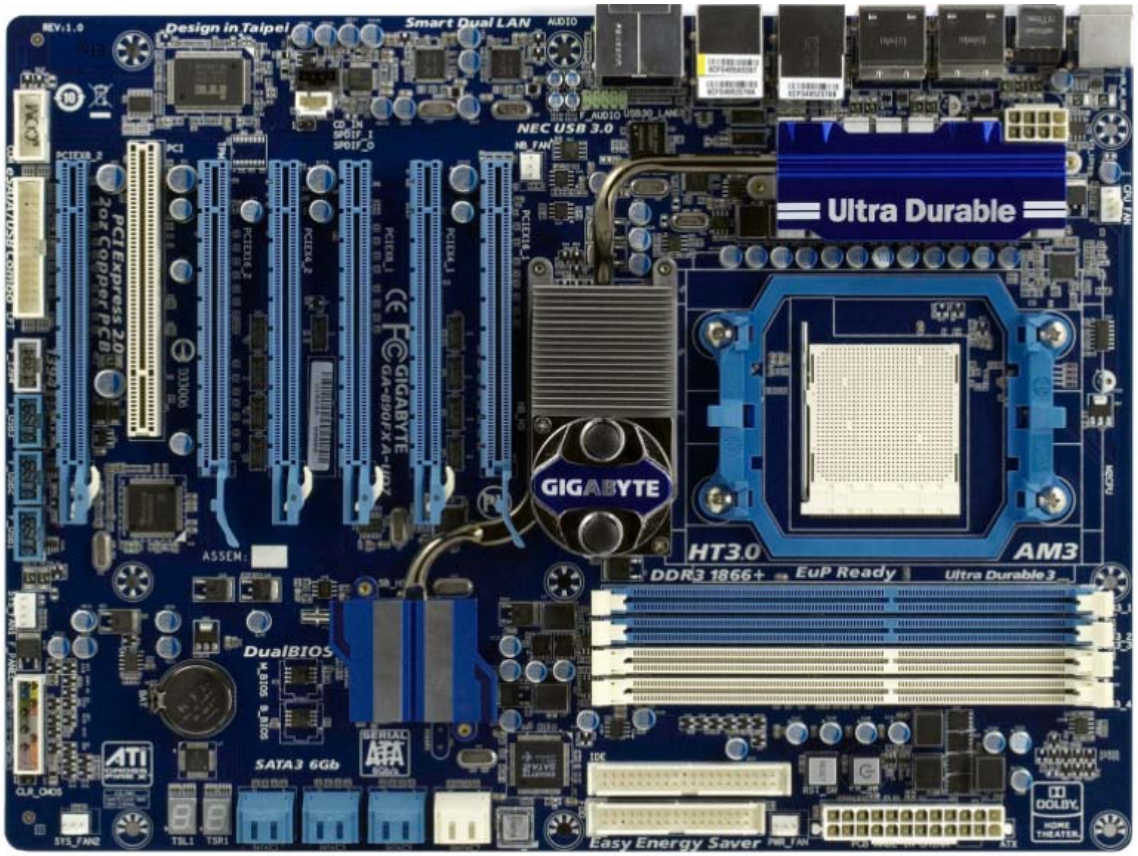


Figure 5.1

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(i) Storage I/Os begin from the Gigabyte chipset and ends at the SATA connectors. It undergoes two transitions from the top layer to L4 and then back to the top layer where it is connected through an AC coupling capacitor before being connected to the connector.

(i.i) Assume a proper ground reference in L2 and L3, draw a complete channel parasitic drawing to include the via models and capacitor models, and show the layer transition.

(3 marks)

(i.ii) Assume that for a second scenario, L2 is a ground plane. There is no ground reference on L3 but instead we have a power reference. Draw the channel parasitic drawing with the layer transition in this case.

(3 marks)

(ii) What type of packages are typically used for the chipset in the motherboard in Figure 5.1?

(3 marks)

(b) Identify components that we typically use for Power Integrity (PI) functions?

(3 marks)

(c) From Figure 5.2, identify two flipped die and one normally placed die. In what area is this kind of package normally applied?

(5 marks)

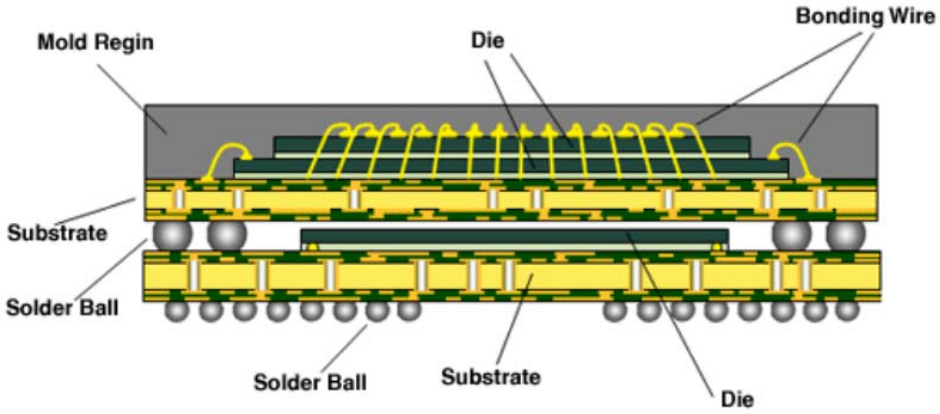

Figure 5.2

(d) During a design phase, the model for the USB3 I/O of the motherboard TL (transmission lines) are found to be inaccurate. Propose some steps that can be done to improve the model.

(3 marks)

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