Second Semester Examination
2017/2018 Academic Session

May/June 2018

EEE520 – EMBEDDED MICROPROCESSOR SYSTEMS

Duration : 3 hours

Please check that this examination paper consists of NINE (9) pages printed material before you begin the examination.

Instructions: This question paper consists **FIVE (5)** questions. Answer **FIVE (5)** questions. All questions carry the same marks.

1. (a) One of the United Nations Millennium Development Goals is to improve access to safe water, which is an engine for socio-economic growth. It is essential that effective water-monitoring programs to improve access to safe water, together with sound data and information management, are operational globally. Unfortunately, in many places in the world, such systems are not in place.

Propose an embedded system that can solve the problem. Your proposal must include the following:

(i) Product definition
(ii) Engineering Specification
(iii) Hardware Specification

(50 marks)

(b) The purpose of this Finite State Machine (FSM) is to control access by three devices to a shared resources in a given system. Only one device can use the resource at a time. Assume that all signals in the system can change values only on the positive edge of the clock signal. Each device provides one output to the FSM, called a request and the FSM produces a separate output for each device called a grant. A device indicates its need to use the resource by asserting its request signal. Whenever the shared resource is not already in use, the FSM considers all requests that are active. Based on a priority scheme it selects one of the requesting devices and asserts its grant signal. When the device is finished using the resource, it deasserts its request signal.

Draw a state diagram for the FSM.

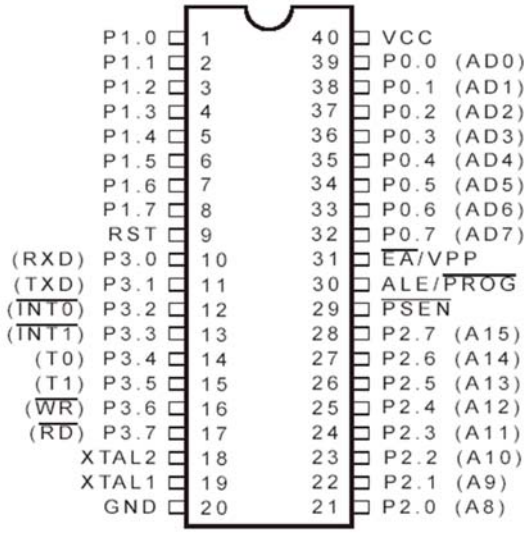
(30 marks)

(c) Minimize the number of the following states.

(20 marks)

Present State	Next State		Output
	w = 0	w = 1	~~z~~
A	B	C	1
B	D	F	1
C	F	E	0
D	B	G	1
E	F	C	0
F	E	D	0
G	F	G	0

2. (a)



Microcontroller

Figure 1

(i) You are required to interface the microcontroller as shown in Figure 1 to 4K ROM and 4K RAM. By using multichip design concept shows the interfacing between the microcontroller and the memories.

(20marks)

(ii) What is the maximum number of I/O devices that can be interfaced to the system? Specify the address of the ROM, RAM and I/O devices.

(20 marks)

(iii) If the I/O device in Figure 2 is used, state three possible addresses that can be used to communicate with the devices. In your opinion, which one is the most appropriate and justify your answer.

(10 marks)

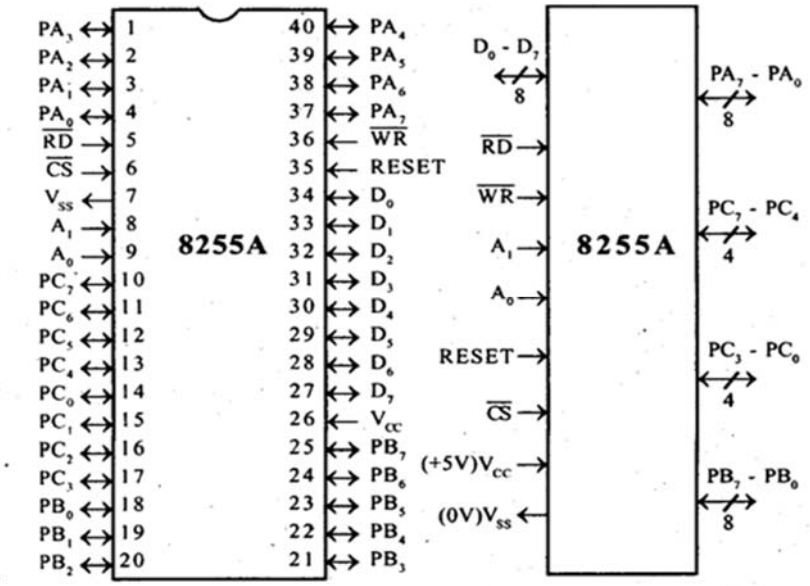


Figure 2

(b)

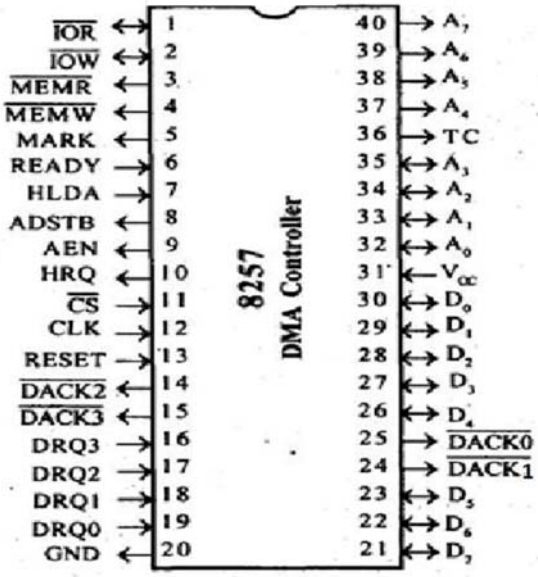


Figure 3

Figure 3 shows DMA controller with the following pin description:

- DRQ: the channel for DMA request, which are used by the peripheral devices for using DMA services.
- DACK: DMA acknowledge line
- HRQ: the signal is used to receive the hold request signal from the output device
- HLDA: It is the Hold acknowledgement signal which indicates the DMA controller that the bus has been granted to the requesting peripheral by the CPU

Answer the following questions:

(i) Explain how the DMA operations are performed.
(20 marks)

(ii) Explain the application of the HRQ and HLDA pins.
(20 marks)

(iii) State one application of the DMA controller
(10 marks)

3. (a) There are some guidelines for interfacing to the interrupt hardware for embedded system. Two types of signal used to the interrupt hardware

(i) List and describe two of signal used to the interrupt hardware
(20 marks)

(ii) Suppose, we want to measure the time elapsed between any two successive events. Let's assume that when the first event occurs, 25 milliseconds later the second event occurs. What is the best signal used to interrupt hardware CPU and explain it briefly.

(30 marks)

(b) A software monitor is a program that usually resides in PROM and allows user to examine memory, registers and I/O ports. Many software engineers write their own monitor programs, although this is less common than it used to be.

(i) List down basic capabilities in common for most monitor programs.

(20 marks)

(ii) Construct a situation where monitor program is used to solve problem of a situation.

(30 marks)

4. (a) Define the terms priority inversion, priority inheritance and priority ceiling inheritance.

(20 marks)

(b) Consider the task set shown in Table 1

Table 1 - Task characteristics (milliseconds)

Task	Computation Time	Period	Deadline
T1	7	40	18
T2	6	80	68
T3	6	90	72
T4	7	50	42
T5	8	25	11

There are three resources: A, B and C. The time required to access each resource is A: 2 ms; B: 3 ms; and C: 1 ms. The tasks access the resources once on each release according to Table 2. You may assume that there are no nested resource accesses (that is, each task can only access one resource at a time)

Table 2 - Resource requirements

Task	A	B	C
T1	X	X	
T2		X	
T3		X	X
T4	X	X	
T5	X	X	X

(i) Using Deadline Monotonic Priority Assignment, assign priorities to T1, T2, T3, T4 and T5. Use larger numbers to represent higher priorities.

(20 marks)

(ii) Assuming simple priority inheritance, determine the blocking time of each task and compute its worst-case response time using response time analysis. Do any of the tasks missed their deadlines?

(30 marks)

(iii) Assuming priority ceiling inheritance, determine the blocking time of each task and compute its worst-case response time using response time analysis. Do any of the tasks miss their deadlines?

(30marks)

5. (a) What is rate monotonic scheduling? What assumptions does rate monotonic analysis make and how are tasks scheduled?

(20marks)

(b) Consider the task set shown in Table 3.

Table 3 - Task Characteristics (milliseconds)

Task	Computation Time	Period
A	12	90
B	9	50
C	10	25

(i) Using rate monotonic task assignment assign priorities to tasks A, B and C. Use larger numbers to represent higher priorities.

(25 marks)

(ii) Use response time analysis to find worst case response times for the tasks. Do all tasks meet their deadlines?

(25 marks)

(c) Describe the differences between fixed and dynamic scheduling policies with reference to RTOS embedded system. Provide suitable examples of such policies.

(30 marks)

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