Second Semester Examination
2017/2018 Academic Session

May/June 2018

EEE 505 – Advanced Analog Integrated Circuit Design

Duration : 3 hours

Please ensure that this examination paper consists of **SEVEN (7)** pages before you begin the examination.

Instructions: Answer **FIVE (5)** questions. Answer **TWO (2)** questions in Part A and **TWO (2)** questions from Part B and **ONE (1)** question from any section.

Use two-book answers for **Part A** and **Part B**.

All questions carry the same marks

…2/-

Part A :

1. Investigate the cascode configuration of multi-transistor M_1 (common-source) and M_2 (common-gate) as shown in Figure 1 below.

   (a) Draw the small signal model for the circuit.

   (6 marks)

   (b) Derive the expression for output resistance, R_O.

   (6 marks)

   (c) Give your opinion on the method of increasing output resistance using the cascode configuration. [Hint: You may need to find the expression for small signal voltage gain, A_V.]

   (8 marks)

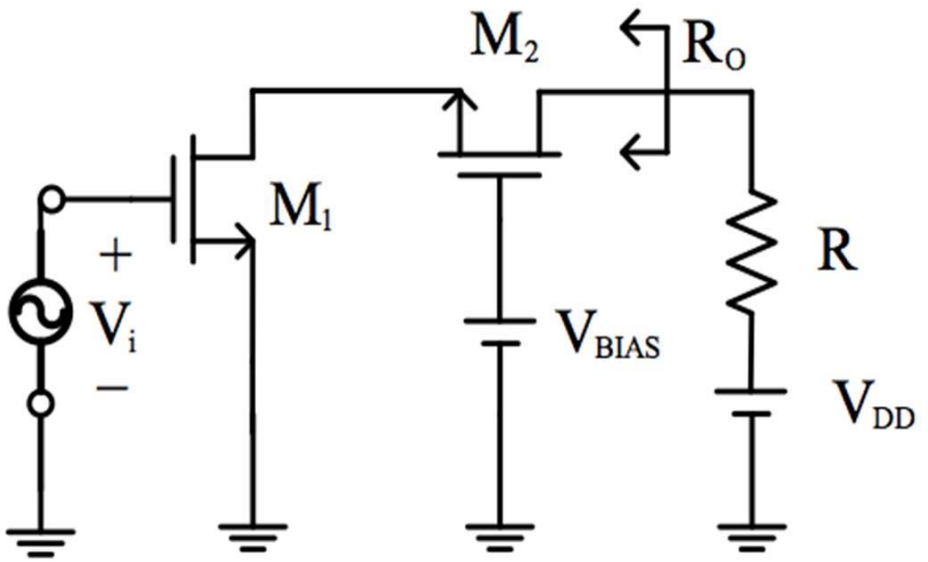

Figure 1.

2. By referring to Figure 2 below,

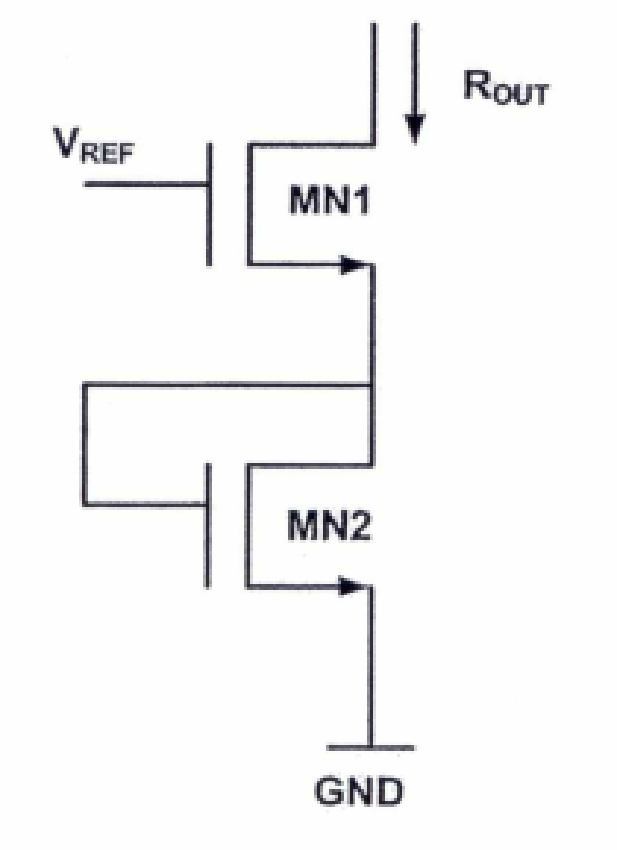

Figure 2

(a) Draw the small signal model for the circuit.

(10 marks)

(b) Derive the expression for $R_{OUT.}$

(10 marks)

3. Figure 3 refers to a differential amplifier design with common-mode and differential-mode inputs.

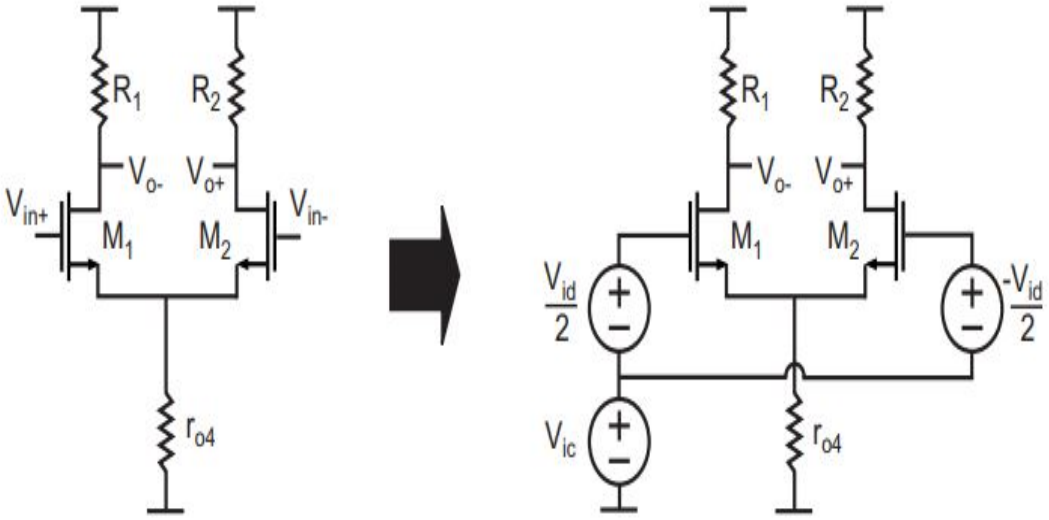

Figure 3

(a) Derive the differential-mode gain, A_{dm}.

(10 marks)

(b) Derive the common-mode gain, A_{cm}.

(10 marks)

Part B :

4.

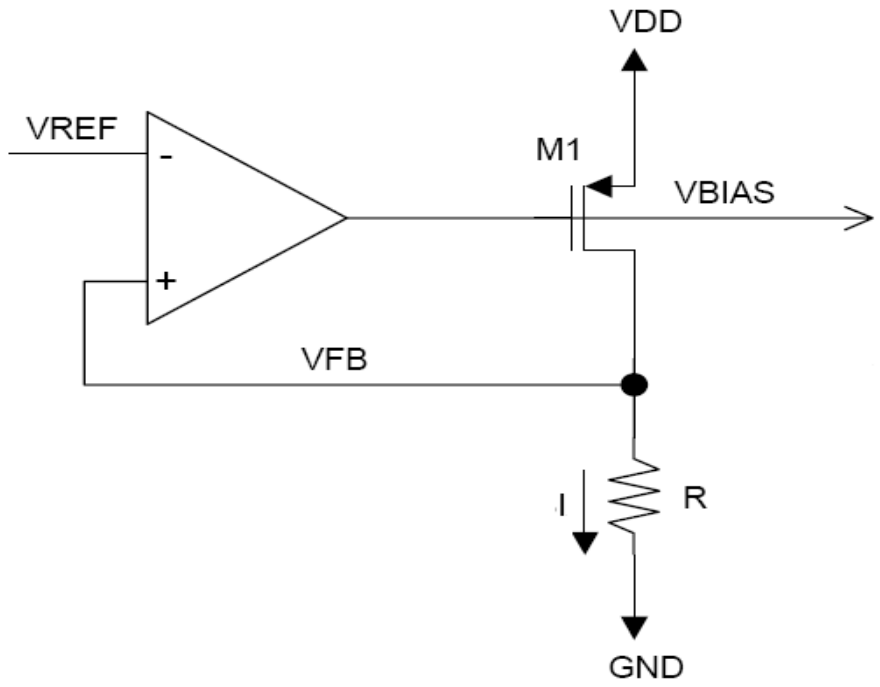

Figure 4:

(a) Figure 4 shows the biasing circuitries for a typical current steering DAC.

(i) Explain the function of the operational amplifier.

(2 marks)

(ii) What is the value of current I, if R is 1.2 kΩ and VREF = 1.2 V?

(2 marks)

(iii) Assuming VDD = 3.6 V and M1 is in saturation, W/L = 12/2, Vtp = -1V, Kp = 40 μA/V^2 , calculate the required VSG.

(6 marks)

(b) Draw the basic 6-bit DAC which must include the biasing circuitries and the DAC resistor string.

(10 marks)

5. (a) (i) State a simplified 3-bit DAC mathematical model. The model is based on current steering-resistor string approach.

(ii) Draw the schematic of the DAC.

(iii) Explain the functions of all the components in the schematic.

(12 marks)

(b) Extend the model up to 8-bit. Explain your model.

(8 marks)

6.

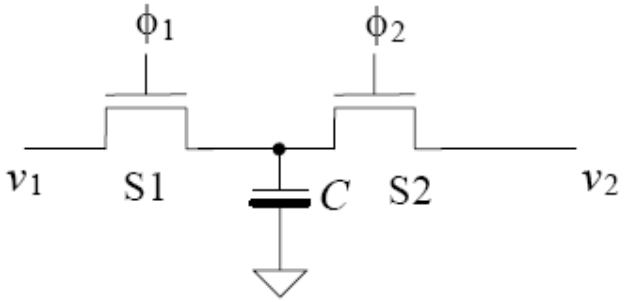

Figure 6: Switched Capacitor Resistor

(a) Figure 6 illustrates the switched capacitor resistor circuit. By referring to the figure:

(i) Explain the function of C.

(2 marks)

(ii) Derive the equivalent resistance of the circuit in Figure 6.

(6 marks)

(iii) Calculate the resistance if the clock frequency is 0.5 MHz and *C* is 1 pF.

(2 marks)

(b) What is the operation of MOSFET whereby the behaviour of V_{GS} is similar as V_{BE} of bandgap device? Together with switched capacitor resistor, design a PTAT current generator. The final equation must be included together with the design.

(10 marks)

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