A SYSTEMATICAL APPROACH FOR A ROBUST ELECTROSTATIC DISCHARGE (ESD) DESIGN

CHUAH CHEOW THENG

UNIVERSITI SAINS MALAYSIA

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A SYSTEMATICAL APPROACH FOR A ROBUST ELECTROSTATIC DISCHARGE (ESD) DESIGN

by

CHUAH CHEOW THENG

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CMOS	Complementary metal-oxide-silicon	1
ESD	Electrostatic discharge	1
MOSFET	Metal- oxide-silicon field-effect transistor	1
TLP	Transmission line pulsing	1
EOS	Electrical over stress	3
HBM	Human Body Model	4
MM	Machine Model	4
CDM	Charged Device Model	4
DOE	Design of Experiments	11
CAD	Computer Aided Design	16
ESTEEM	Extended ESD Compact Models	17
TCAD	Technology computer aided design	22
ASIC	Design specific IC architecture	32
FD-NMOS	Fully Depleted NMOS	38
SCR	Silicon Controlled Rectifier	38
ggNMOS	Grounded gate N-MOSFET	39
gCNMOS	Gate coupling NMOS	40

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LVS	Layout Versus Schematic	65
GUI	Graphic User Interface	71
BJT	Bipolar junction transistor	94

SUATU PENDEKATAN SISTEMATIK BAGI REKABENTUK

NYAHCAS ELEKTROSTATIK YANG TEGAP

ABSTRAK

Dengan peningkatan kegagalan cip disebabkan ESD, reka bentuk IC untuk membangunkan aliran reka bentuk ESD yang komprehensif menggunakan pelbagai perisian automatik yang boleh mengesan secara berkesan kelemahan reka bentuk ESD lebih awal dalam fasa reka bentuk telah menjadi semakin penting. Kita perlu mendapatkan reka bentuk (reka bentuk ESD dalam konteks ini) yang tepat pada kali pertama. Aliran pengesahan reka bentuk ESD sedia ada adalah sama ada bergantung susun atur (pemeriksa peraturan reka bentuk susun atur), bergantung litar (simulasi litar) atau terlalu lewat untuk memintas masalah reka bentuk ESD. Satu cadangan aliran reka bentuk ESD ditunjukkan dengan beberapa idea reka bentuk ESD yang betul-masa-pembinaan. Satu metodologi reka bentuk dan strategi perlindungan ESD untuk sistem digital, teguh kepada peristiwa-peristiwa ESD, dibangunkan dan disahkan untuk teknologi MOS komersial 45nm, 65 nm dan 90 nm. Aliran reka bentuk ESD pada dasarnya mengambil berat tentang model tekanan ESD HBM, MM dan CDM. Aliran reka bentuk ESD yang dihasilkan menunjukkan pelbagai jenis kesilapan reka bentuk telah dapat dikesan dan mewajarkan keperluan untuk peningkatan strategi perlindungan ESD ini. Kita mempunyai pemeriksa aturan reka bentuk bentangan, simulasi litar, alat automatik letakan pengapit dan beberapa alatan lain dalam aliran reka bentuk ESD ini. Menggunakan teknik-teknik pengukuran, pemodelan dan simulasi, metodologi reka bentuk dan strategi perlindungan ESD telah berjaya diimplementasikan ke dalam aliran reka bentuk utama komersial. Cip-cip ujian tertentu, direkabentuk menggunakan aturan-aturan ESD konvensional yang disasarkan untuk perlindungan tekanan ESD, telah digunakan sebagai bahan-bahan ujian bagi metodologi baru ini. Perubahan reka bentuk ini menghasilkan cip yang melepasi aras-aras tekanan ESD (piawaian industri HBM 2.5kV, MM 200V dan CDM 500V) dengan hampir tiada pindaan reka bentuk yang besar.

A SYSTEMATICAL APPROACH FOR A ROBUST ELECTROSTATIC DISCHARGE (ESD) DESIGN

ABSTRACT

With the increase events of ESD-induced chip failure, it has become vital for the IC design community to develop a comprehensive ESD design flow with various automated tools that can efficiently detect ESD design weakness early in the design phase. We need to get the design (ESD design in this context) right at the very first time. Existing ESD design verification flow is either layout dependent (layout design rule checker), circuit dependent (circuit simulation) or too late to intercept the ESD design problem. A proposed ESD design flow is demonstrated with some correct-by-construction ESD design idea. An ESD design methodology and protection strategy for digital systems, robust to ESD events, is developed and validated for commercial 45nm, 65 nm and 90 nm MOS technologies. The ESD design flow basically takes care of the HBM, MM and CDM ESD stress models. The ESD design flow demonstrates different type of design errors that the tools have uncovered and justify the need for this enhanced ESD protection strategy. We have layout design rule checker, circuit simulation, auto clamp placement tool and other tools_in our ESD design flow. Using these measurement, modeling and simulation techniques, the design methodology and protection strategy was successfully implemented into a commercial mainstream design flow. Specific IC test chips, designed using conventional ESD rules targeted for ESD stress protection, were used as test vehicles for the new methodology; resulting design changes resulted in chips that passed levels of ESD stress (industrial standard of HBM 2.5kV, MM 200V and CDM 500V) with virtually no major design amendments.

CHAPTER 1

INTRODUCTION

1.0) Introduction

Continuous scaling adherence to Moore's law has created high integration and low cost for mass production, integrated circuits (ICs) with high-speed input/output (I/O) operating in giga-Hz (GHz) frequency bands designed and fabricated in complementary metal-oxide-silicon (CMOS) technology. The trigger voltage and holding voltage of electrostatic discharge (ESD) protection device must be designed lower than the gate-oxide breakdown voltage of metal- oxide-silicon field-effect transistor (MOSFET) to prevent I/O circuits from being damaged during ESD stresses. Moreover, the turn-on resistance of ESD protection device should be minimized in order to reduce the joule heat generated in the ESD protection device during ESD events. The gate-oxide breakdown voltage of MOSFET is also decreased as semiconductor process technology is scaled down to nanoscale. For instance, the gate-oxide breakdown voltage under 100-ns transmission line pulsing (TLP) stress is decreased to only ~5 V in a 90-nm CMOS technology with gate- oxide thickness of ~15 Å. But, the ESD voltages in our environment could be as high as thousands of volts. Thus, ESD protection design in nanoscale becomes more challenging. To simultaneously optimize the circuit performance and ESD robustness, the I/O circuit and ESD protection circuit should be co-designed in the design phase of IC products in systematically approach in ESD design flow with construct-by-design strategy[1].

1.1) Background of ESD

ESD is little more than the shock experienced when touching a metal doorknob after walking across a carpeted room or sliding across a car seat in our daily life. However, ESD has been a serious industrial problem for centuries. As early as the 1400's, ancient forts were using static control procedures and devices to prevent electrostatic discharge ignition of black powder stores. By the 19th century, paper mills in United State of America employed basic grounding, flame ionization techniques, and steam drums to dissipate ESD from the paper through the drying process[2]. All business and industrial process has issues with electrostatic charge and discharge at one time or another. Munitions and explosives, petrochemical, pharmaceutical, agriculture, printing and graphic arts, plastics and others are just some of the industries where control of ESD has vital importance.

The age of electronics brought with it new challenge associated with ESD, as electronic devices become faster and smaller, their sensitivity to ESD increases. Today, ESD impacts productivity and product reliability in virtually every aspect of the global electronics environment.

Despite a great deal of effort during the past few decades , ESD still affects production yields, manufacturing costs, product quality, product reliability, and profitability. The cost of damaged devices themselves ranges from only a few cents for a diode to thousands of dollars for complex IC. It is unlikely that any company which ignores static control will be able to successfully manufacture and deliver undamaged electronic parts.

1.2) Problem Statement

ESD is a phenomenon of charge balancing process between two objects at different potential. Usually, static electricity can be generated due to the friction between different kind of materials, and the accumulated electrostatic charge can spontaneously be transferred to the object at lower potential. In our daily life, ESD events usually give a mild shock to human being that is a bit annoying but if the same amount of ESD stress is injected into a microelectronic component in nano scale, it could be detrimental. ESD events often involve high voltage (kV) and high current stress (1 - 10 A) on electric devices. Despite the fact of very short duration (0.2 - 200 ns), the ESD event incurs a massive current/voltage pulses can destroy ICs. These catastrophic ESD failures are none other then junction breakdown, molten via effects, the gate oxide rupture and source to drain punch-through.

In fact, a substantial number of IC failures are related to ESD/EOS (electrical over stress). ESD/EOS damage is responsible for nearly one third of the failures of IC, and approximately 10 % of customer returns are exclusively due to ESD problems. Indisputably ESD is one of the most important quality and reliability concerns in the IC industry. Therefore, to make highly reliable IC products that are insensitive to ESD threats, ESD phenomenon must be well controlled through all phases of a device's life cycle. Despite the strong need for understanding of ESD phenomena, there has been a perception that ESD engineering is a 'black art'; ESD engineers used to provide solutions based on their experience without fundamental understanding of failure mechanisms. However, during the past twenty years, numerous studies have laid the foundation for a deeper understanding of the ESD phenomena, and based on that understanding, various on-chip ESD protection techniques have been developed. ESD studies are very vast and multi-discipline studies encompass thermal, mechanical, geometrical and electrical physics.

This thesis presents simulation models that can be used to predict CDM failures in system-in-packages and Human Body Model (HBM) and Machine Model (MM)failure in chip level. Simulation of Charged Device Model (CDM) events in the IC requires modeling the plural charge storage locations and discharge paths. The CDM test is carried out on a packaged IC of a product. Finding the ESD related failures after fabricating and packaging an IC costly than finding the same issues earlier in the design cycle, and fixing them before fabrication. Thus, it is desirable to detect the ESD weaknesses in the IC design and fix them before fabricating the ICs (until packaging). In the HBM and the MM tests, peak current for a given pre-charge voltage is known beforehand. Designers can design and place the ESD protection circuits to minimize the stress on the circuits for each stress mode. However, in the CDM test, the peak current varies from design to design, depending on the size of the die and of the package. Unlike in the other tests, during the CDM test, the path of discharge cannot be easily located and identified. A charge storage model needs to be created to better understand the current discharge paths and the resulting potential drop. The rise time dictates that transient effects have to be included while analysing the circuit reliability and study the robustness of circuits. These ESD circuit simulations also allow the designers to measure voltages and currents at the internal nodes, a method which is not easy to implement while testing the packaged ICs. Circuit simulations allow the chip designers to conduct what-if analysis and make well-informed decisions during the circuit, package or ESD protection network re-design. These are very important for ESD reiteration in design stage and also allow the analysis of the root cause of any unexpected ESD failures (HBM, MM or CDM).

1.3) Motivation for Setup ESD Design Flow

Typical conventional ESD validation method is mainly in the post Si phase which leaves a very tight narrow design time window for fixing any potential ESD failures. ESD has become a major reliability of semiconductor industry. Thus, we need an early prediction of ESD performance of the ESD protection install in the design protection scheme at the early phase of design flow. Any early prediction would provide flexibility to provide proper ESD fixes (circuit, layout, technology process and others) to achieve ESD proof design.

ESD protection is essential for reliability and high yield. By focusing all ESD protection development efforts on device-level protection circuits, the chip-level paths are often neglected. ESD events are notoriously difficult to simulate and do not address power bussing issues; design rules are meant to be broken. Every new product really becomes an ESD test chip as we have encounter new ESD issue that we never experience before.

This is a difficult problem to solve. The long-term solution lies in improved technology: models, simulation, and characterization. Each engineer making decisions in the new product development cycle needs to become familiar with the standard methods of ESD testing. A device designer may understand nuances of the breakdown characteristics of an ESD protection structure, but may not understand the details of the product-level testing that the device must withstand. The system designer may follow strict rules in the application of ESD protection cells to the chip-level design, but without knowledge of how the product will be zapped, it may not have the ability to adapt to the unique requirements of their chip architecture.