METHOD FOR VALIDATING THE INTEGRITY OF CLOCK NETWORK SIGNAL IN FPGA DEVICE

By

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List of Abbreviations

Abbreviation	Meaning
ASIC	Application specific Integrated Circuit
CLK	Clock
CPLD	Complex Programmable Logic de
DCD	Duty Cycle Distortion
FF	Fast Unit
FPGA	Field Programming Gate Array
GCLK	Global Clock
I/O	Input Output
LAB	Logic Array Block
LE	Logic Element
LR	Linear Regression
LUT	Look-Up-Table
MUX	Multiplexer
PLL	Phase Lock Loop
PVT	Process Voltage Temperature
SS	Slow Unit
TT	Typical Unit
IP	Intellectual Properties

KAEDAH UNTUK MENGESAHKAN INTEGRITI ISYARAT RANGKAIAN JAM DALAM PERANTI FPGA

Abstrak

Rangkaian jam merupakan elemen utama dalam sistem digital kerana ia digunakan untuk memberi isyarat jam kepada lain-lain blok dalaman. Oleh kerana saiz litar bersepadu menjadi lebih kecil dan kompleks, lebih banyak data dan jam yang melalui dalam kawasan cip . Sebagai hasilnya, masa yang diambil untuk melalui laluan itu akan menjadi lebih lama. Projek ini akan membentangkan beberapa kaedah untuk mencirikan prestasi jam dan korelasi masa pada peranti FPGA. Pengesahan proses terbahagi kepada 4 bahagian (i) Reka bentuk litar ujian yang akan digunakan untuk meguji dengan menggunakan Quartus II (ii) disahkan fungsi Reka bentuk menggunakan alat simulasi Modelsim (iii) melaksanakan pemeriksaan dan mengumpulkan data dan akhirnya (iv) menganalisis prestasi jam berdasarkan data yang dikumpul. Keputusan prestasi jam yang di uji dijangka mencapai spesifikasi yang diterbitkan oleh kilang. Sementara itu bagi ujian liputan masa, keputusan pengukuran sebenar akan dibandingkan dengan keputusan simulasi menggunakan kaedah Linear Regression (LR) untuk memastikan kedua-dua keputusan adalah berkaitan. Berdasarkan data yang diperolehi daripada ujian prestasi, ia menumjukkan jam boleh mencapai tahap kelajuan maksimum sehingga 450MHz untuk peranti yang berkelajuan tinggi. Selain itu, ganguan pada isyarat jam juga mematuhi spesifikasi yang ditetapkan oleh kilang iaitu di antara +/-5% daripada tempoh masa jam. Untuk ujian masa, Semua keputusan simulasi dan pengukuran menunjukkan hubungan yang baik dengan pekali korelasi (R2) sehingga 0.98 dan +/-5% margin diantara keputusan simulasi dan keputusan pengukutran.

METHOD FOR VALIDATING THE INTEGRITY OF CLOCK NETWORK SIGNAL IN FPGA DEVICE

Abstract

The clock network is the main element in the digital system as it is used to provide the clock signal to others internal block. As integrated circuits become smaller and more complex, more data and clock paths are routed within a smaller chip area. As a result, the delay of the paths becomes more significant to the timing. This project presents several methods to characterize the clock performance and the timing correlation on FPGA devices. The validation process is divided into 4 parts (i) Design the test circuit that are used for testing by using Quartus II (ii) Verifying the design functionality using Modelsim simulation tools (iii) Performing tests and collecting data and finally (iv) Analysing the clock performance based on data that has been collected. The result of the clock performance check out is expected to achieve the specification imposed by the factory. For timing related coverage, the result of the actual measurements was compared with the simulation results using Linear Regression (LR) method to ensure both results correlate. The measurement results showed that clock can achieve a maximum frequency up to 450MHz for higher speed devices. In addition to that, the clock jitter also meets the design specification set by the factory which is between +/-5%. For the timing correlation patterns, all simulation and measurement results show good relationship with correlation coefficient (R^2) of up to 0.98 and with a margin within +/-5% between simulation and measurement results.

CHAPTER 1

INTRODUCTION

1.1 Introduction

This chapter focused on the introduction of the research including the objectives that need to be achieve by the end of the project. Besides that, this chapter also lists the scope of the research which covers the simulation and hardware implementation.

1.2 Field Programmable Gate Array (FPGA)

FPGA is a semiconductor device that contains the programmable logic elements or logic blocks. The logic block in the FPGA device can be programmed to perform a specific function from as a basic logic gates operation up to the complex logic function. Altera and Xilinx is dominated the FPGA markets by introducing a series of FPGA products. Xilinx uses the Vivado IDE development software to interface with the Xilinx FPGA, whereas an Altera FPGA is uses Quartus II simulation software. Both QuartusII and Vivado IDE simulation software uses Verilog and VHDL as the design language. Both company have their own customize design block that available in the tools for a user to use in the development of design to operate with the FPGA devices.

All the design will be written and verified in the simulation tools before it's being transfer to the hardware. This process is to make sure that the design can operate as per requirement and reducing the time that taken for a debugging stage as well as the design cost.

FPGA device is widely used in industrial automation because it ability to work at wide range of temperature and voltage setting. Each FPGA device will go

through the retention test before it been ship out to the end user to check the quality of the device.

The FPGA are designed to have the multiple input output and several IP blocks such as DSP, Memory, Latch and PLL. Each of the block can be internally configured by user without need an external devices. Other than that, it is also immune to electrical noise and resistance to vibration and impact. Besides an FPGA, ASIC is also another popular microcontroller device that is available in the market. The major different between FPGA and ASIC is ASIC is an integrated circuit that is designed for a specific application and rather than for general-purpose used. The ASIC device cannot be re-configured. Table 1.1 below shows the main comparison between FPGA and ASIC devices.

Field Programmable Gate Array (FPGA)	**Application Specific Integrated Circuit(ASIC)**
Reconfigurable device.	Application specific – One time programming device
FPGA tends to be slower and consumes more power than ASICs	Low power consumption
Mix of programmable and hard function	Build in the specific IP block for the specific design.
The re-configurability can benefit platform longevity by the design change or upgrade	Unable to re-configure the device once the design is completed.

Table 1.1: Comparison between FPGA and ASIC

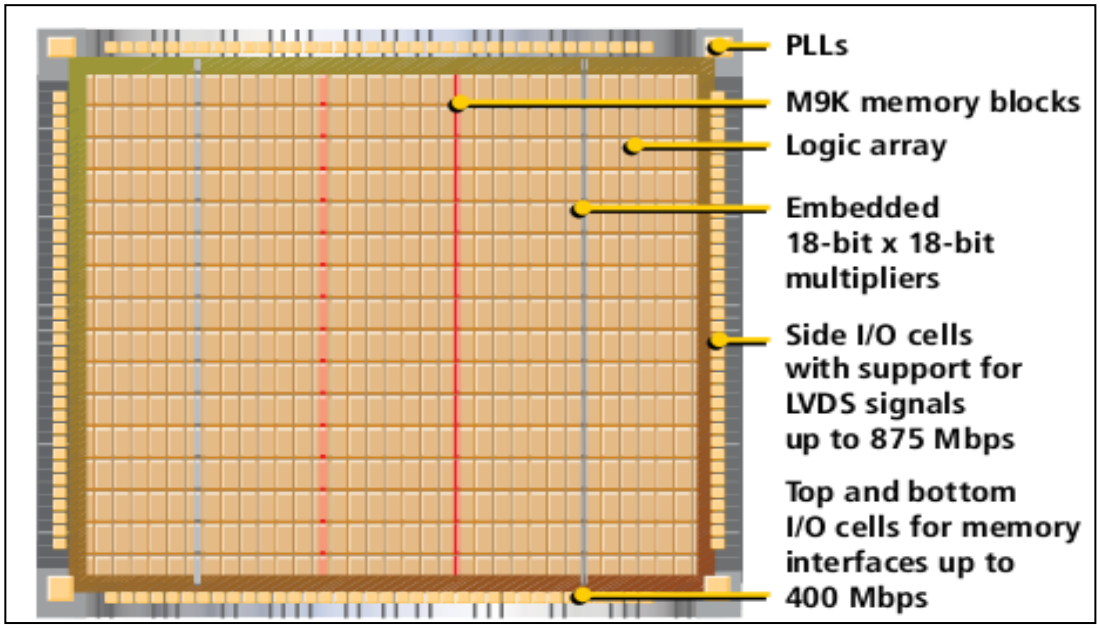

Figure 1.1: Example of Altera FPGA floor plan

The demands for FPGA are increasing from time to time because the device promises the good performance as the change of the process node. Besides that, the latest FPGA devices also offer great features such as the built-in DSP (Digital Signalling Processor) block and system-on-chips (SoC) which allow the user to use it without the need of any external interfacing device. Figure 1.1 is the example of Altera FPGA device which have been design with a multiple build in IP blocks.

1.3 Problem Statement

The clock signal is the fastest and the most active block in the digital integrated circuit. It spans the entire chip and is the most critical control signal in the design (Saleh, Hussain, Rochel & Overhauser, 2000). In the FPGA devices, the clock network is the main block that distributes the clock signal to the entire internal IP blocks that are integrated in the device. Nowadays FPGA, have a mixture of programmable and hard function blocks which are integrated in the devices such as the Digital Signaling Protocol (DSP), Memory and SOC. With the increasing number of blocks and features that they provide, the single clock source is insufficient to provide the clock signal for each block in the chip; therefore the latest FPGA device normally will have at least 5-10 clock sources. As the number of clock source in the FPGA devices increase, the synchronization becomes the significant issue in the real-time application. The clock synchronization is important to ensure that each clock source will reach the required block within the boundary of the timing.

Most of system-on-chip (SoC) design requires multiple independent clock sources and multiple interfaces. Some are using different clock frequencies. There is also a trend toward designing major sub-blocks of SoCs to run on independent clocks to ease the problem of clock skew across large chips. In order to overcome the synchronization problem in the design, the global clock needs to have abilities to handle multiple independent clocks at the same time.

The clock network is the main element in the FPGA timing, it need to verified correctly in order to avoid the performance degradation and timing failure in the entire chip. As the frequency increase, the timing becomes more complex and critical. Each interconnects will significantly impact the timing. The interconnect delay will directly impact the timing correlation on other blocks.

Besides that, the hold and setup time violation will cause the IP block to operate improperly and consequently resulting in the timing failure. With all this issue in mind, this project presents the method to validate the clock network to minimize the issue of clock synchronization and meta stability. Besides that this research also analyses the change of the clock performance with a different Process, Voltage and Temperature (PVT). Each different corner unit will have a different clock performance; this project is conducted to characterize the silicon performance with the change of voltage, temperature and units (PVT). The performance of the clock network will directly impact the performance of the other built- in block in the FPGA.

1.4 Objectives

The main objective of this project is to perform clock network validation on FPGA device, in order to verify the clock functionality and minimize the clock synchronization and meta stability issue. This project uses Quartus II and Modelsim simulation software to achieve the objectives.

The other objectives of this project are:

1. To analyze the timing correlation of the clock network in term of the setup and hold time violation.
2. To investigate the effect of the process variation PVT (Process, Voltage and Temperature) to the clock performance and timing.

1.5 Research Contribution

Process technology was decrease from time to time, process variation such as temperature and voltage give a significant impact to the timing and the clock performance .The research will present the method of validating the clock network in the Cyclone III FPGA. The test circuit generation, actual silicon implementation and the measurement method are presented. Besides that, the data analysis for using Linear Regression method has been discussed in the research. Furthermore this project will also present the effect of the change of process, voltage and temperature (PVT) to the clock performance. The important of this project is to make sure that the Cyclone III device performance meets the specification and the model has been designed in the Quartus II simulation software is correlated with the actual measurement results.

1.6 Research Scope

The research scope is divided into three parts: -

1. Designing the test circuits
    i. Design the test circuit by using Quartus II simulation software.
    ii. Compile patterns and make sure the logic circuit passing the synthesis test.
2. Simulation and testing
    i. Test bench to verify the design functionality
    ii. Assigning each input and output to the I/O pins.
3. Hardware and testing on bench
    i. Setup bench to perform the measurement. Connecting all the components to the design board and troubleshooting the setup using 1 in and 1 out patterns.
    iii. Collect the data for analysis.
    iv. Perform data analysis using Linear Regression method

1.7 Thesis Organization

This thesis is organized into five chapters. Each chapter discusses details of the particular topic in order to provide good understanding on this project.

Chapter 1 describes the background of the project including the problem statements and also the objective that need to achieve at the end of the research.

Chapter 2 delineates the theoretical concept of the FPGA as main device in the research. In addition to that this chapter is reviewing the Cyclone III clock architecture and the features that available. The primary concept of this research is to understand the significant of the test coverage for the clock signal. In addition, the technical theory of the test coverage is also described in this chapter such as maximum clock frequency, jitter and the clock timing.

Chapter 3 represents the research methodology and the overall flow of the research. The research covers the performance and timing validation of the Cyclone III FPGA. This chapter describes the details of the validation technique and also the test procedure

Chapter 4 publishes the result that obtained from the measurement. The clock performance is analyses and make sure that the output is meets the performance target that listed in the Chapter3. For the timing correlation, the linear regression method is use to compare the simulation and the actual measurement results.

Chapter 5 interpret the outcome of the research and conclude whether the research is meets it objective or not. Besides that, in this chapter there is a list recommendation to on enhance the research results.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

This chapter focused on the theoretical review and description on the Field Programmable Logic Array (FPGA), Clock Network and the clock validation method. This chapter will also include all the variable or terms that are used in this project.

2.2 Field Programmable Gate Array (FPGA)

There are three main categories of Programmable Logic devices which are available in the market which is Complex Programmable Logic Devices (CPLD), ASIC and FPGA. Each type of programmable logic has different features compare to another, but the main function of these device is to be program to perform a specific task. The complex programmable logic devices (CPLD) is the Altera low-cost, non-volatile CPLDs feature over two decades of innovations and are used broadly throughout the electronic industry. These highly integrated, single-chip programmable devices are ideally suited to manage multiple system functions in control plane or data path application

Compare with CPLD and ASIC, FPGA is comprises with thousands of logic blocks, and interconnect resources. FPGA is configures through programming by the end user and a re-programmable device. Figure 2.1 depicted the FPGA internal core structure by using an array of logic elements. Besides that, the FPGA core block is resides by a multiple I/O pins.

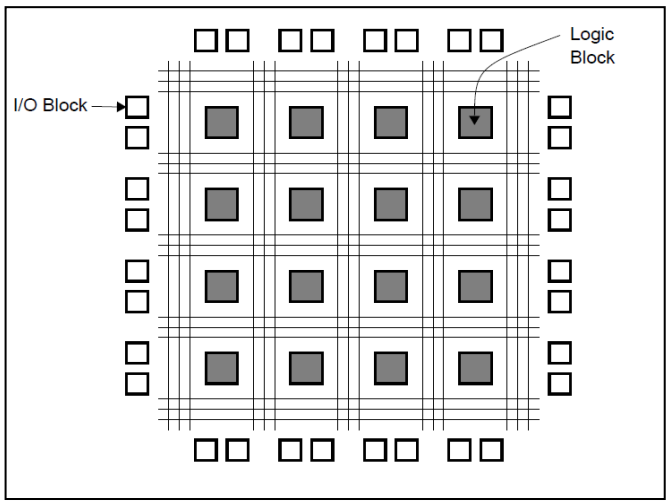

Figure 2.1: FPGA internal core structure

Figure 2.2 is the conventional way of system designs which having a multiple external block such as Flash, SDRAM and DSP. The latest FPGA provide major advantage to the user by replacing the entire internal block with a single FPGA. This will help to reduce the cost, area and power consumption. Besides that, it's much easier to interface because the entire block is sharing the same platform. The market trend of FPGA device was increase from time to time because it offers a high performance programmable device with multiple built-in blocks, which help to reduce the development cost. FPGA devices can be found in most of the application such as consumer automotive, communication broadcast, military, computer and storage

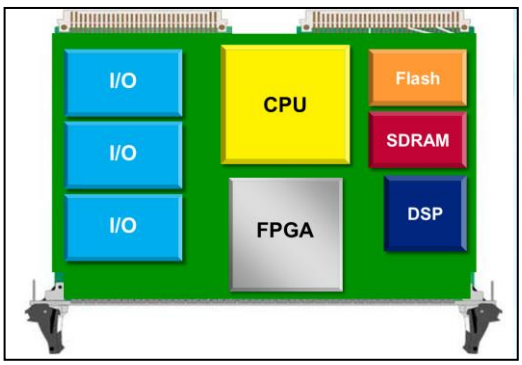

Figure 2.2 : Conventional system design interface

2.3 Cyclone III FPGA Architecture

Cyclone III FPGA is the third generation of Altera Cyclone series that offer an unprecedented combination of low power, high functionality, and low cost. Figure 2.3 is the available features in the Cyclone III FPGA. Cyclone III FPGAs are built on TSMC 65-nm low-power (LP) process technology with additional silicon optimizations and software features to minimize power consumption.

Cyclone III FPGAs include a customer-defined feature set optimized for cost-sensitive applications, and offer a wide range of density, memory, embedded multiplier, I/O, and packaging options. Cyclone III FPGAs support numerous external memory interfaces and I/O protocols common in high-volume application.

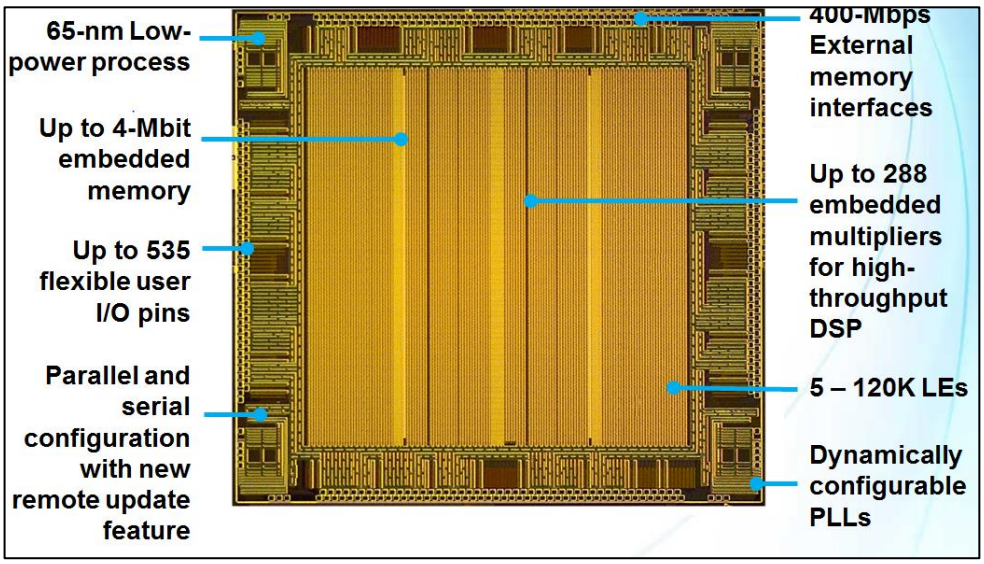

Figure 2.3 : Cyclone III Architecture Features (2015)

Altera Cyclone III FPGA consists of two categories of device family which are Cyclone III and Cyclone III LS (2015). Each different type of device has a different performance and features as shown in Figure 2.4. User can choose any type of the device based on the application and the design requirement.

The highest density of logic element is suitable for a complex application that required a complex logic design. The M9K block is the internal memory block, the highest number of block provide the large memory space in the FPGA. PLL is also one of the important blocks in digital design to generate the clock signal instead of using global clock source. The different between PLL and the global clock source is it can change the clock frequency during execution where it is fixing in the global clock network.

Compare with Cyclone III, Cyclone III LS is the first low power FPGA that include high assurance design support and enabling system level requirements to be implemented at the device level. Along with that, it also has the highest logic, memory and multiplier densities of any low power device. In addition to that, the Cyclone III FPGA is optimal for advanced signal processing on a portable or handheld platform.

Family	Device	Logic Elements	Number of M9K Blocks	Total RAM Bits	18 x 18 Multipliers	PLLs	Global Clock Networks	Maximum User I/Os
Cyclone III	EP3C5	5,136	46	423,936	23	2	10	182
	EP3C10	10,320	46	423,936	23	2	10	182
	EP3C16	15,408	56	516,096	56	4	20	346
	EP3C25	24,624	66	608,256	66	4	20	215
	EP3C40	39,600	126	1,161,216	126	4	20	535
	EP3C55	55,856	260	2,396,160	156	4	20	377
	EP3C80	81,264	305	2,810,880	244	4	20	429
	EP3C120	119,088	432	3,981,312	288	4	20	531
Cyclone III LS	EP3CLS70	70,208	333	3,068,928	200	4	20	429
	EP3CLS100	100,448	483	4,451,328	276	4	20	429
	EP3CLS150	150,848	666	6,137,856	320	4	20	429
	EP3CLS200	198,464	891	8,211,456	396	4	20	429

Figure 2.4 : Cyclone III Type and features

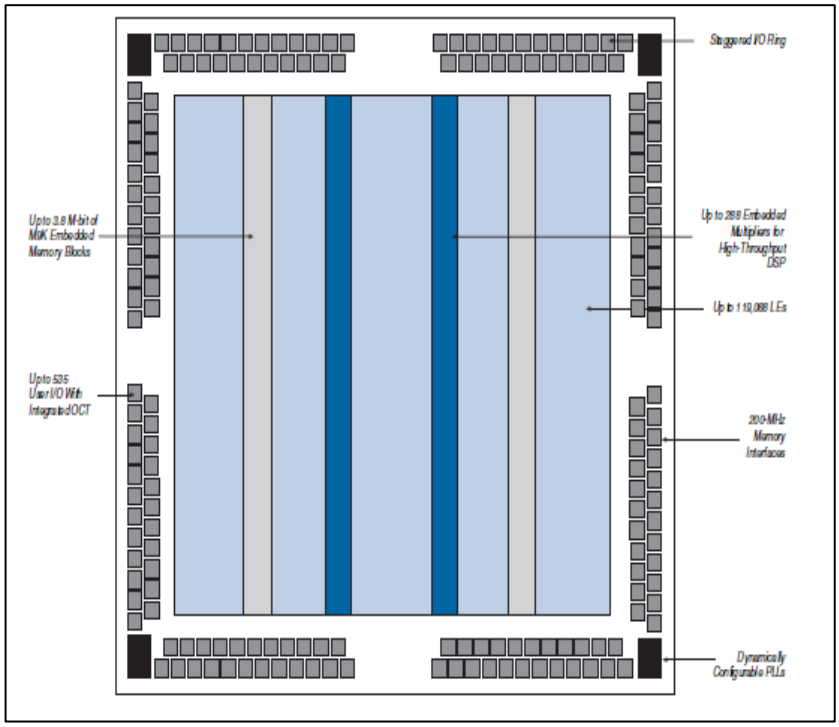

Figure 2.5 : Cyclone III Device Architecture

Figure 2.5 is the Cyclone III architecture consists of up to 120K vertically arranged logic elements (LE), 4 Mbits of embedded memory arranged as 9-Kbit (M9K) blocks, embedded multipliers, and phase-locked loops (PLLs) that are surrounded by I/O elements (IOE).The core block is dominated by the Logic Element (LE). Each logic array consists of 16 Logic elements with 4 inputs, register and output driver. The Logic Array Block (LAB) consists of 16 Logic Elements (LE) and a LAB-wide Control Block (LCB). Each LE has 4 inputs with a 4-input Look-Up-Table (LUT), a register and output logic. The LAB-wide Control Block is physically located in the mid-section of the LAB with 8 LEs above and 8 LEs below it. Included in the LAB-wide Control Block are the circuits required for Register Cascade to span multiple LAB columns for REGSCAN purposes.

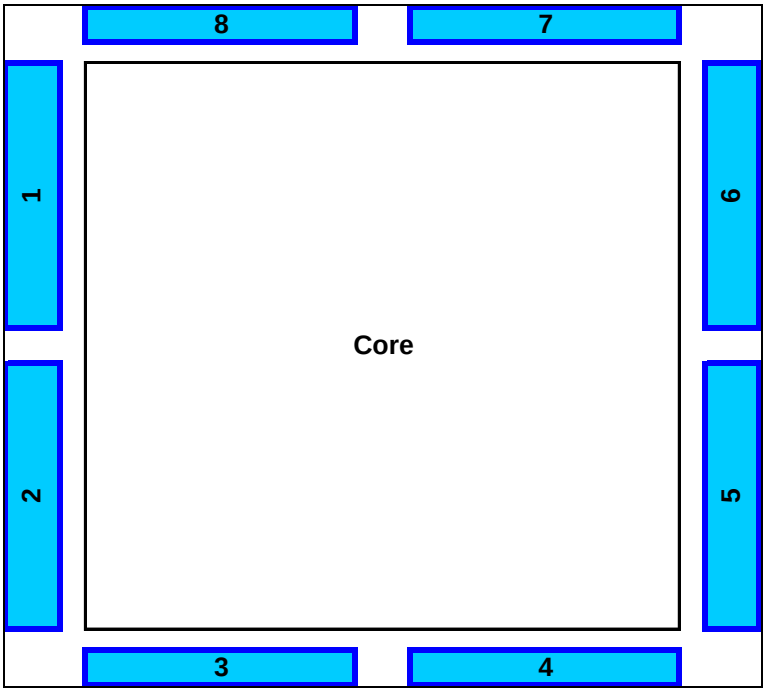

Figure 2.6 : Cyclone III I/O Bank

Cyclone III I/O pins are grouped into eight sets. Each set connected to one of eight power banks, Bank1 to Bank8. There are two power banks per side as shown in the Figure 2.6. A package pin is routed to the associated I/O or dedicated pad from the same power bank regardless any type of device is packaged in. A given VCCN pin is always routed to the same power bank specified for all devices in a given package. In general, for a given package, a power pin remains that same type of power no matter what device is packaged in it (2015).

2.4 Clock Network in Cyclone III FPGA

With the rapidly growing chip sizes and constant rate of decrease in the minimum features size, design of the fast clock trees is becoming the most important design challenge (Sauter, Schmitt-Landsiedel, Thewes & Weber, 2000). The availability of the synchronous clock signals to internal logic elements is the paramount importance in the design of digital integrated circuit (Keezer, 1990).

The higher clock rates in the digital electronic design have resulted to the complexity in the clock distribution network. Cyclone III clock networks provide clock sources for the core, HIO and VIO decoder blocks in the device. In addition, GCLK network can be used as high fan-out or global signal networks, such as reset, clear and etc. based on user application. The Cyclone III clock networking is constructed using H-tree architecture with 2 different architectures: a) 1-Spine architecture, and b) 2-Spine architecture. Cyclone III devices provide 10 (1-Spine) or 20 (2-Spine) GCLK network. The increases in number of GCLK networks in 2-Spine architecture members is to provide more clock network resources for high fan-out and clock network intensive applications.

The Cyclone III clock network performance is targeted for 450 MHz except for the biggest member (3C120), which has a target of 437.5 MHz

Cyclone III global clock signals can be drive from dedicated clock pins, dual-purpose clock pins, user logic, and PLL block. Cyclone III device family includes up to four PLLs with five outputs per PLL to provide robust clock management and synthesis. Instead of directly used the global clock source the use of PLL block is more efficient to device clock management, external system clock management, and I/O interfaces. Besides that the PLL is isolated from the chip supply and further bypassed to reduce the jitter (Harris & Naffziger, 2001).The Cyclone III is enables