20-GBPS HIGH-SPEED CONVERGED I/O LOOP BACK TEST DESIGN METHODOLOGY FOR SIGNAL INTEGRITY ENHANCEMENT

By

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LIST OF ABBREVIATIONS AND NOMENCLATURE

Abbreviation	Meaning
ATE	Automated Tester
ATH	Automated Test Handler
BER	Bit Error Rate
BGA	Ball Grid Array
CIO	Converged Input / Output
dB	Decibels
EHM	Eye Height Monitoring
EWM	Eye Width Monitoring
FC	Flip Chip
FEXT	Far End Crosstalk
Gbps	Giga Bit Per Seconds
GHz	Giga Hertz
HVM	High Volume Manufacturing
IL	Insertion Loss
mil	a unit length equal to 0.001 inch
mV	millivolt
NEXT	Near End Crosstalk
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express

RL	Return Loss
rms	Root Mean Square
Rx	Receive
SMA	Sub Miniature version A
SI	Signal Integrity
Tx	Transmit
VNA	Vector Network Analyzer

KAEDAH REKABENTUK TERTUMPU UJIAN I/O GELUNG BALIKAN 20-GBPS KELAJUAN TINGGI UNTUK PENINGKATAN INTEGRITI ISYARAT

ABSTRAK

Dalam pengeluaran jumlah yang tinggi (HVM), degradasi isyarat pada kelajuan tinggi dan frekuensi tinggi akan mempengaruhi keputusan ujian. Dalam bidang semikonduktor, ketidaktepatan hasil ujian persediaan akan meningkatkan kos operasi ujian dan melambatkan masa pengeluaran produk. Dengan permintaan untuk peningkatan pesat dalam ujian kelajuan tinggi, isyarat integriti menjadi sangat penting. Dalam tesis ini, kaedah rekabentuk tertumpu ujian I/O gelung balikan 20-Gbps kelajuan tinggi untuk peningkatan integriti isyarat telah dijalankan untuk peningkatan isyarat integriti di dalam papan litar bercetak (PCB) dengan dua puluh enam lapisan. Kesan isyarat integriti daripada rekabentuk PCB yang sebelum yang beroperasi pada 5-Gbps pada frekuensi operasi maksimum 2.5 GHz telah dikaji dan rekabentuk PCB yang dicadangkan dinilai dari 20-Gbps pada frekuensi operasi maksimum 10 GHz. Beberapa parameter utama rekabentuk seperti surih panjang yang berlainan dikaji dan komponen yang digunakan dalam ujian kelajuan tinggi daripada rekabentuk PCB terdahulu diselidik dengan lebih mendalam. Penyelidikan ini dijalankan untuk mengenalpasti faktor yang mendominasi integriti isyarat di dalam sistem ujian kelajuan tinggi. Tambahan pula, penyelidikan ini termasuk fabrikasi kupon ujian untuk memahami kesan parameter rekabentuk semasa penyelesaian langkah simulasi dan sebelum langkah fabrikasi PCB yang sebenar. Di dalam tesis ini, PCB yang dicadangkan telah diuji pada 20-Gbps dan didapati ia mampu beroperasi dengan kehilangaan sisipan sebanyak -4 dB.

20-GBPS HIGH-SPEED CONVERGED I/O LOOP BACK TEST DESIGN METHODOLOGY FOR SIGNAL INTEGRITY ENHANCEMENT

ABSTRACT

In high-volume manufacturing (HVM), the degradations of signals at high speed and high frequencies will affect test results. In the semiconductor field, inaccuracies of test setup impact a product yield, increase test operating cost and delay products release time. With the demand for rapid improvements in high-speed tests, signal integrity becomes very important. This thesis presents a 20-Gbps high-speed Converged I/O (CIO) and Peripherals Components Interference Express (PCIe) external loop back test design for signal integrity enhancement in a twenty six layer printed circuit board (PCB). The signal integrity effects were studied from the previous PCB design which operates at 5-Gbps at 2.5 GHz maximum operating frequency and the proposed PCB design were evaluated at 20-Gbps at 10 GHz maximum operating frequency. Several key design parameters such as different trace lengths were studied and components that were used in high-speed tests were further investigated from the previous PCB design. These efforts were performed to identify the dominating factors of signal integrity in high-speed test systems. In addition, research studies included the fabrication and measurement of test coupons to understand the impact of design parameters upon the completion of simulation prior to the actual PCB fabrication. In this thesis, the proposed PCB was tested at 20-Gbps and it was capable to operate with an insertion loss (IL) of -4 dB.

CHAPTER 1

INTRODUCTION

1.1 Overview

In high-speed test systems, Signal Integrity (SI) is becoming a major concern in the world of semiconductors. Signal integrity in high-speed digital design is critical to ensure that the transmitted signal is received correctly at the output of the receiver end. The most common cause of signal integrity problems is transmitted signal getting distorted and not producing expected output at the receiver end. Signal integrity is important in major integrated circuits between flip chip packages and in multi-layer printed circuit boards (PCB) consisting of signal traces, power/ground planes, vias and specific components meant for a particular design. Signal integrity is observed and evaluated in the time domain and the frequency domain. In the time domain, signals can be distorted by factors such as attenuation, crosstalk, delay, jitter, reflections, dispersion, electromagnetic interference, frequency dependent losses and signal imbalance.

Another method to measure signals is using the frequency domain. This makes it simpler to measure and view patterns of signals and trends compared to the time domain. The frequency domain also handles sinusoids better and is able to perform simpler calculations by transforming differential equations into algebraic equations. The effects of signal integrity in a high speed converged I/O loop back test design environment are listed below:

- **Attenuation and loss** caused by non-zero resistivity, and also the finite conductivity of the dielectric. It is a function of the type of material used during the design stage of manufacturing.
- **Crosstalk** between adjacent lines, resulting in one line inducing voltage on another line. This phenomenon is caused by the effect of mutual inductance and mutual capacitance. Crosstalk can cause signal delays, which results in false switching.
- **Delay** in signal, which propagates along traces at a finite speed and takes a finite amount of time (also known as flight time) to reach its destination. Delays skew the results, with the signal observed to be received at different times for different components.
- **Jitter**, or differences in the time the signal was projected to occur and the time it actually occurred. There are two types of jitter, namely deterministic jitter and random jitter, where jitter is often analyzed statistically.
- **Reflections**: a signal propagating along traces will be reflected when it encounters a discontinuity.

- **Dispersion:** signals at different frequencies propagate at different velocities.
- **EMI**: Electromagnetic interference, in which radiation interferences interfere with the signal.

In today's technology era, electronics and computing devices are moving in the direction of hand held, mobility, small size, minimum power consumption, greater reliability, and cost-effectiveness. The best strategy for achieving these goals is to be the best semiconductor manufacturer, who can quickly produce new products to win over the semiconductor market.

This research starts with a detailed discussion of the increasing product requirements and signal integrity issues that were faced in a class test high-volume manufacturing (HVM) environment for a flip chip (FC) package product. The root cause of signal integrity problem was the printed circuit board (PCB) design not being fully optimized. Main reason of signal integrity issue back in the previous product's PCB was because the PCB was built to include a number of package attributes that can be tested in a single PCB. The overall main target was to implement a cost effective PCB designed for multiple products that uses a single PCB hardware for high-speed testing for a group of flip chip products with similar attributes. The PCB was designed to test at a speed range of up to 10-Gbps at the maximum operating frequency of 5 GHz (Gigahertz).

At present, a new generation of flip chip package products is targeted to operate at a data rate of 20-Gbps external loop back test at the maximum operating frequency of 10 GHz. These new flip chip products have doubled up the overall high-speed test requirements.

In the view point of [1-4], the author summarized that current test systems must double up their test capabilities in accordance with the Moore's Law theory. PCBs which were used in high-volume manufacturing (HVM) to perform tests on millions of new products are required to be investigated in terms of its signal integrity performance. In addition, these products must also support high-speed protocols, such as the Converged I/O (CIO) and the Peripherals Components Interference Express (PCIe) which is sensitive to noise.

CIO and PCIe protocols are sensitive in high-speed test because these tests are designed to be wrapped in a single packet and transmit a signal via one protocol which is the converged I/O. Converged I/O design operates at 20-Gbps to measure transmitted signal with reference data for EWM (eye width monitoring) and EHM (eye height monitoring). The design were based on flip chip device perspective that has a capability of supporting up to four lanes transmitting and receiving signal in at the same time, as shown in Figure 1.1.

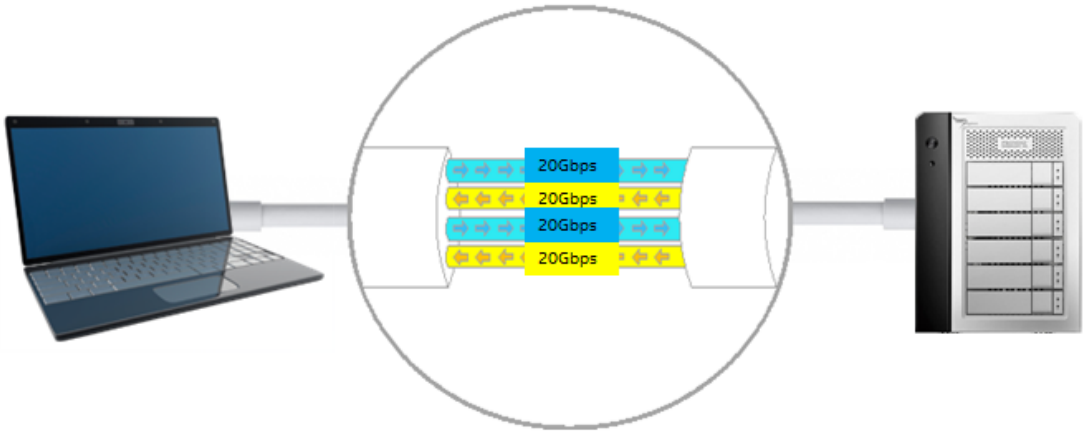

Figure 1.1 Converged I/O interface capable up to 4 lanes between the host and the user.

The high-speed test in flip chip product package is divided into two segments. They are the internal loop back test and the external loop back test. The issues covered in this research focus on the external high-speed loop back test, which requires that the signal be transmitted and received through a PCB design which includes both the CIO and the PCIe tests. For the external loop back test, it is necessary to test the Bit Error Rate (BER) which requires an external loop back signal routing that goes through a PCB before it is returned back to the product from the Tx to the Rx. Eye Width Monitoring (EWM), and Eye Height Monitoring (EHM) were also tested during the high-speed test. These high-speed specifications, of the flip chip product requirement are embedded into a test program that is attached to an automated tester where these products will be tested. During these high speed-test, signal that are generated from the test program to test the flip chip product will be required to pass through a PCB that is a designed with an external board and return the signal to the product. These external loop back tests were designed to pass through a stress board (i.e. the external test board) for a multi-layer PCB that consists of twenty six layers. This main PCB is designed to test different types of products with the same attributes. External boards on the PCB will be utilized to perform the high-speed test based on the individual product type and its test requirements.

In the previous PCB, the loop back test path was designed as an active path using high speed relays, inductors and external boards. This is shown in Figure 1.2. With this setup, it allows the device under test (DUT) to be tested through an exterior path. The test module in this research uses a coded test program that is embedded in the automated tester (ATE) based on target specifications of a flip chip product. Then, while the device is under test, the test program will sample Rx data from the external loop back test and verify it against the reference that is stored. Then Tx signal passes through a high-speed relay and an inductor in an external stress board where it completes the loopback path back to the Rx of the device. In such a complicated setup, signal degradation from transmitter to receiver is expected. If the hardware used for this high-speed test is not performing as expected, errors and losses will occur. This is expected especially when the signal is required to pass through components and the long traces of the previous designed PCB.

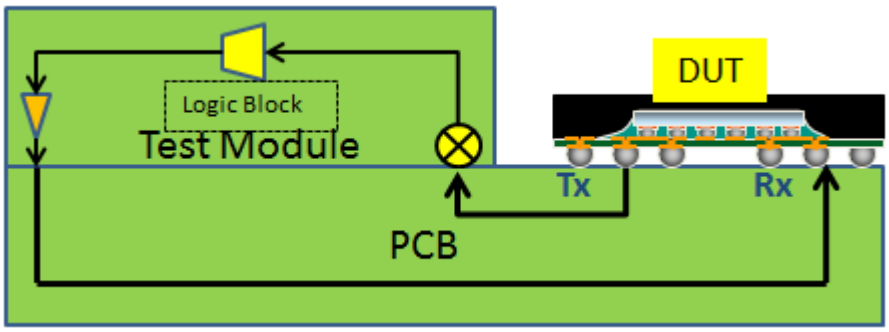

Figure 1.2 Typical loop back paths for external loop back test.

In the previous designed PCB, this is the best solution to create a low-cost PCB that allows the use of a single PCB for many flip chip products [1]. This helps to reduce the overall operating cost of a flip chip product. A high-speed test is configured to check the basic function of its products prior to starting its test flow. The CIO BER configures the Tx with a specified bit error count for a specified time period and compare it to the Rx. If there is any failure specific to the CIO lane, it is considered broken or not stable at high speeds. CIO EWM captures data from the BER test and then proceeds to calculate the eye width. This eye width results per lane will be compared against the pre-data references that were set in the test flow based on product requirements in the test program embedded in the automated tester. CIO EHM will continue the work of the EWM test, which runs and analyze the heights of the positive part of the eye and the negative part of the eye of the captured signal against the reference data, similar to the EWM concept. A typical PCB design consists of four to six layers of stacked boards but in this high-speed flip chip product, it is a requirement by product specification to have at least twenty six layers of boards. With almost twenty different test blocks that are required to be tested for a flip chip product, it is important that the CIO traces are designed to be on the top layer of the PCB closer to the DUT to avoid signal integrity issues. With that, the geometry of the high-speed test traces will not be straightforward due to PCB design rules and component placements that need to be in that region. High-speed test traces follows the Manhattan design rule in completing its signal traces.

The PCIe flow configuration is straightforward; the Tx is to send data to the Rx at the signal data rate from the external loop back through a typical multi-layer PCB. If any of these protocols fails to receive its data from the external loop back through the PCB, then it will fail its test. The high-speed test will be measured from low frequency to high frequency based on the flip chip product requirement. This described flow will be in the continuous mode for every individual product tested on a single PCB in the test environment. Figure 1.3 uses a block diagram flow to demonstrate how a converged I/O loop back test structure for an individual product (flip chip package functions) within the previous designed PCB.

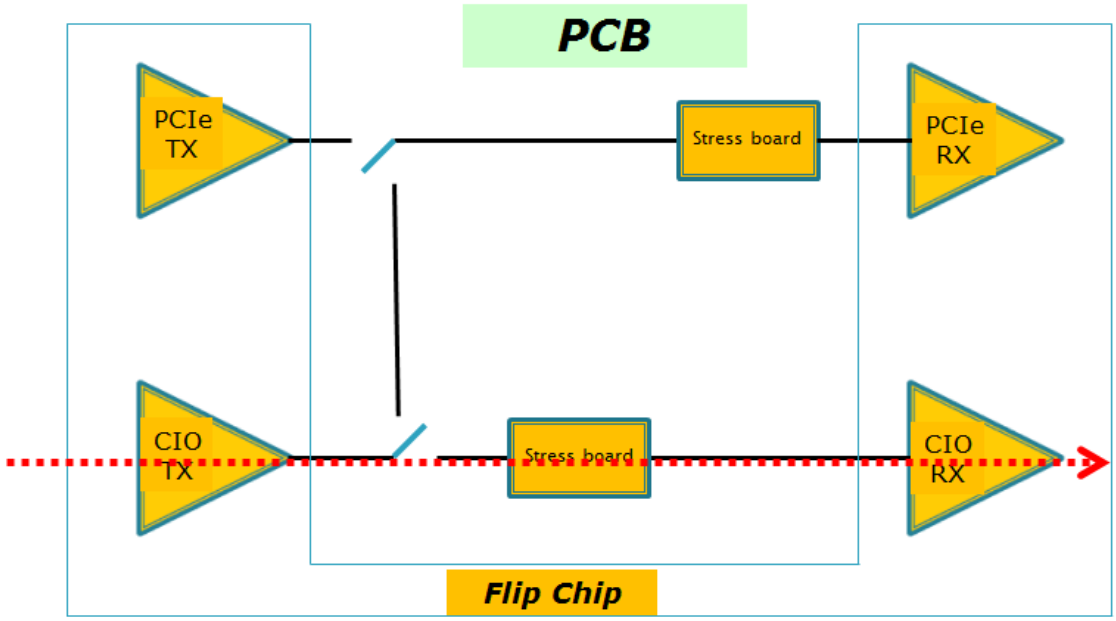

Figure 1.3 Loop back test methodology of a flip chip product in the previous PCB design.

1.2 Problem Statement

In this research, the problem statement focuses on unwanted yield losses due to known good products (flip chip devices) tested in marginally-performing PCB, failing CIO and PCIe tests. Further analysis shows that the Tx data could not be received at the Rx due to the use of the stress boards in the PCB which degraded the connection and eventually the device did not pass EWM and EHM tests. These tests are complex with four CIO test lanes to accommodate, which requires going through components, long traces, vias and stubs in the stress board, which are meant for multiple products [3-5]. CIO and PCIe protocols of known good devices do not fail by a large margin, but they fail marginally close to the test limits based on the required specifications, which makes it difficult to analyze. Flip chips failing on the CIO high-speed tests, show instability performance results where known good devices sometimes fail. Test results were analyzed based on the data log that was captured during the test. Symptoms of these failures clearly indicate that the overall design were not up to expectation to meet the 10-Gbps requirement. Analysis is carried out over a large number of package devices tested in a single PCB. The failing PCBs were replaced with new PCBs, but the problem still remained once these PCBs were used in a HVM test environment. When the failing flip chip product earlier was retested again in a different test cycle, it passes. This is a waste in resources where it is required to retest known good flip chip products where else it is supposed to be passing at the initial test.

Thus, troubleshooting efforts are performed. Model-based problem solving, with a structured high speed test analysis are done focuses on these failing PCBs to understand what exactly went wrong from the previous designed PCB. The PCB was designed for products manufactured with low cost, without considering high-speed test signal integrity sensitivity. Previous PCB design work did not include simulations to test the PCB at high-speed prior to the real PCB fabrication. In addition, they included external boards that were designed to cater for multiple products with the same package attributes. This is the main reason that causes the PCB to fail at high-speed. As a result, delays in delivering products to markets due to instability issues seen in the HVM class test environment, impacts the overall productivity costs [2-6]. In addition to the challenges that came up during the testing, new product requirements were set. CIO and PCIe are required to work at higher speeds given the current state. In previous flip chip requirements, products were tested at lower bit rates, but now the speed has to increase to 20-Gbps. The design of such product package is proportional to the increase in the operating frequency, which is now more than 10 GHz. It is difficult to meet the overall target if the conventional test system setup method is not revised. It is important to look into opportunities to reduce the traces lengths and improve the design rule of the previous designed PCB for high-speed loop back test [4-6].

1.3 Objectives

The objectives of this research are:

- ✓ To design a multi-layer PCB which will enable the integrated overall test system to operate at minimum noise level (less than 10 dB insertion loss) that is measured in the frequency domain.
- ✓ To further analyze the performance of the designed PCB in the time domain by ANSOFT HFSS simulation of eye diagrams that are able to operate at a data rate speed of 20-Gbps.

1.4 Scope of the work

This thesis covers a comprehensive test system setup that consists of a twenty six multi-layer PCB, where each layer has its own design rule complexity. As a result, the overall test system setup has a profound effect on signal integrity [4]. This thesis features in-depth analysis of key innovations in the correlation and the research of optimization on signal integrity for the 20-Gbps high-speed converged I/O (CIO and PCIe). Having identified issues with previous PCB design and doubled up high-speed test operating speed, the main focus of the research now is to eliminate potential errors that could result in high yield loss of a high volume manufacturing flip chip product.

First, high risk factors were identified. Then risk factors were sorted by priority. Finally, the risk with highest priority was selected, based on previous PCB knowledge, issues, and the data obtained. Eliminating the needs for long traces in a PCB for a direct external loop back from the Tx to the Rx without any boards or components in the middle of the traces, is a top priority [4]. This simplifies the high-speed loop back design, by making it direct without the need of external boards in a PCB. Previous designed PCB with external boards in a conventional way was removed and only applied components that are really needed for new generation products are retained. This helps to eliminate the need of vias that are found in multi-layer PCBs, as well as the need for connectors and switches. By heading in this direction, the overall design target is to make the Tx and the Rx loop back test signal design closer to the device under test (DUT). The geometry of trace placements in the PCB board is considered carefully in terms of the selection of the components, such as the relay, and the need for other components for the new design. This idea was considered at each of the design steps, aiming to achieve the best design for a 20-Gbps data rate in a high volume manufacturing environment.

1.5 Organization of the thesis

The thesis is organized into five chapters. In Chapter 1, the overview and the importance of the research are described.

In Chapter 2, literature review is presented with the background and the research study of signal integrity in high-speed tests of multi-layer printed circuit board test systems, pertaining to 20-Gbps data rate tests.

Chapter 3 explains the detailed aspect of the overall design methodology of 20-Gbps high-speed converged I/O loop back test design, including how the design topology was focusing on the high-speed loop back test with respect to the PCB design, and how validation steps meet the overall target with simulation tool ANSOFT HFSS. Measurements of the s-parameter, the insertion loss and the eye diagram of high-speed test were performed. Finally, this chapter highlights the comparison studies on simulation versus actual measurement from the test coupon building and the actual new PCB.

In Chapter 4, the results obtained from the validated ANSOFT HFSS simulation data, test coupons measurements, the previous PCB board simulation and measurement, the new PCB board simulation and measurement and analysis of eye diagrams, are discussed.

Finally, the conclusion of this research and the contributions of the findings, are presented in Chapter 5. Furthermore, the possible future works for the continuation of this study are proposed.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Signal integrity is one of the key issues in the design stage, especially when the required package becomes more complex. Converged I/O (CIO) is the current leading technology trend for multiple data rates during high-speed test interface. Complexity of converged I/O becomes a challenge when high-speed tests are performed in an external test environment setup that requires optimum conditions without any losses. In order to perform a successful high-speed test with a good yield on a device in a test manufacturing environment, every single segment that functions in the test system should be set up in optimized conditions.

The chapter starts with an overview of the test system setup for a high-speed test. Then, the signal integrity effects of a 20-Gbps high-speed converged I/O loop back test structure and a multi-layer printed circuit board (PCB) for a high-speed I/O test were reviewed. This is followed by the high-speed test transmission line design in a printed

circuit board and high-speed test signal integrity enhancement methodology for test setup. Finally, a literature review summary is presented.

2.2 Overview

In a test system setup for a high-speed test, it is critical that the contact between the device and the test pogo pin is precise, in order to ensure proper contact resistance is achieved, so that a high-speed test can be performed without any breaks in the signal [1]. Test pogo pin is being used widely in semiconductor test environment as an interface between a ball grid array package and a test socket. This pogo pin is designed to be in the range of the flip chip product diameter to ensure that it works to connect the ball grid array of the flip chip product and the PCB. This flip chip product is controlled by an automated test handler (ATH) to handle products to be tested in precise setup alignment, so that they have a perfect contact with the pogo pins while under test. The automated test handler has been set up with pre-defined specifications of the force (F) that is required to be applied on the flip chip product that needs to be tested. The overall structure of a typical test environment is explained in Figure 2.1.

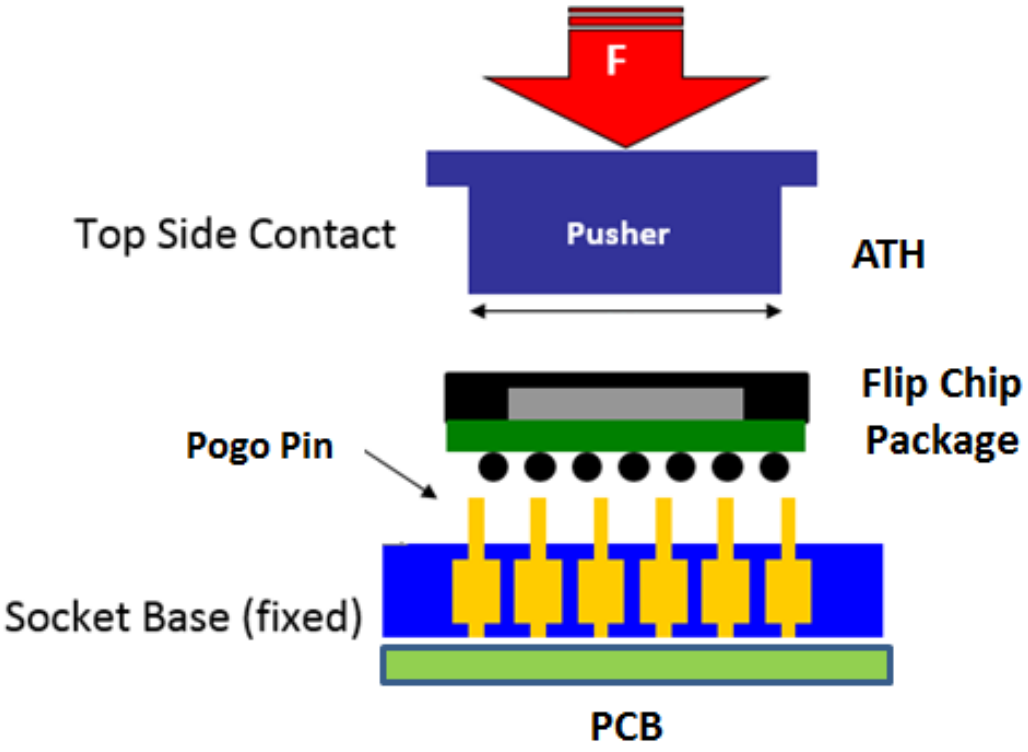

Figure 2.1 Overview of test system setup for a high-speed test.

In this research, an assumption is made that a perfect contact resistance is achieved while the device was under test, without any losses. Further analysis was carried out to look into the optimization of the printed circuit board design to cater to high-speed CIO and PCIe in a test system environment.

The high-speed tests are required to transmit signals, which are initiated through a device positioned between the silicon and the ball grid array (BGA) of the package through a PCB. This device will be plugged by the test handler into a test socket through the test pogo pin tip. When the device is in contact and aligned by the automated test hander to the pogo pin, the device will be tested using a printed circuit board connected

to an automated tester with an embedded test program based on the required product specifications. The CIO and PCIe protocols will require the signal to be transmitted from the PCB's external board to the pogo pin through the Rx pins of the package itself. If there is a break in the transmitted signal, loss or noise occurring, while the device is undergoing test, it will result in a test failure for the device. Test instability is seen as a systematic failure, where it can be reproduced and is caused by the current PCB design itself. The problem statement and the intention of this research are to understand and enhance the PCB design methodology for high-speed I/O. The flip chip package of the new generation test board, which was used as the test vehicle in this research, is required to operate at a 20-Gbps high-speed data rate within the package to transmit and to receive signals successfully through a multi-layer PCB and its components. The goal is to ensure that only devices known to be good are being shipped to the intended customer [7-9].

2.3 20-Gbps high-speed converged I/O loop back test structures

This study reviews existing research on improving the signal integrity for 20-Gbps high-speed data rate loop back test. A research on 20-Gbps high-speed test focusing on signal integrity characterization using on-chip interconnects embedded test structures is presented in [2]. The author designed and modelled a test vehicle that, proved through simulation, demonstrated how to characterize signal integrity in an on-chip flip chip package. In general, a converged input and output (CIO) high-speed test is electrically fixed in the device. It is designed for a single-ended bus to attain a higher bandwidth and data rate at the die level [3]. This is a necessary step, in order to trim down the device's power consumption [3-4]. With the current technology trend, high-speed test that can be manufactured at low operating costs, eliminates the waste of redundancy and can be marketed quickly [5]. With the complexity increasing and requirements becoming more stringent, the majority of high-speed test featured in the reviewed literature operated in the range of up to 10-Gbps – 16-Gbps. In [3], the author has also suggested a new method, proposed an ideal working model, and validated the accuracy of a multi-port differential I/O on a chip that works perfectly with a 20-Gbps high-speed test as shown in Figure 2.2.

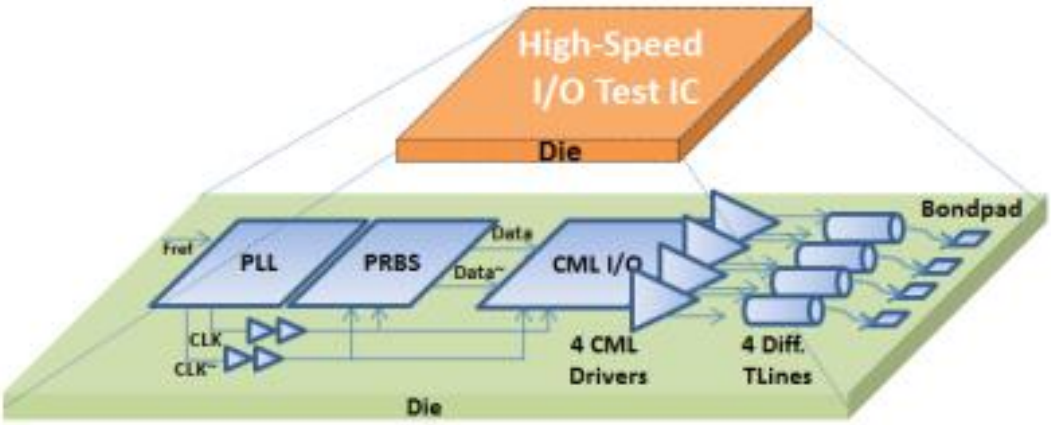

Figure 2.2 Concept block diagram for an on-chip high-speed I/O test product [3].

Most of the literature did not cover future proposed work on signal integrity when it comes to an external loop back test. An external loop back test path is required to test the DUT in a high-volume environment. The author has looked into a 20-Gbps data rate test of a new device trend but the research covered only internal loop back test on the die of the device under test [3]. A reliable high-speed loop back test structure is important, as that would lower the overall manufacturing cost [5-10].

2.4 Printed circuit board for high-speed converged I/O loop back test

In general, with a high-speed test, which involves CIO and PCIe loop back tests, signal integrity is very important, in order to ensure that the test system is set up without additional losses. Understanding the need for product requirements, knowing the test hardware collaterals, plus conducting tests to ensure high-speed data tests are achievable, all are important necessary steps. In this research, the focus is on the PCB design that is used for a high-speed loop back test of a flip chip package, operating at 20-Gbps at 10 GHz maximum operating frequency.

Printed circuit board design analysis is a key methodology, and it needs to be considered carefully for any design cycle. This design step also goes in parallel when the components involved are highly complex by design and is expected to be tested at high speed and high frequency [1-5]. As the testing procedure increases in complexity, the product design also trends towards smaller form factors [11-14].

With these challenges, the PCB must be tested using a high-speed test. Environment setup is vital in order to perform rigorous tests. This helps to ensure the consistency, accuracy and design robustness. Such test system setups, often have multi-layer boards set-up, with each layer serving a specific purpose, such as the generation, the acquisition, or the analysis of test data. Hence, designing such a system requires

foresight, as well as the ability to analyze, and address signal integrity issues. These signal integrity factors must be taken into consideration for both CIO and PCIe loop back tests at the 20-Gbps data rate.

Investigating signal integrity effects of the I/O, as well as validating the accuracy of the package electrical model becomes increasingly important when dealing with a high-speed I/O loop back test [3-5]. PCBs are required to perform extra layout checks after completing the final design, using simulations to ensure that required specifications are met for good signal integrity before proceeding with PCB manufacturing process. This avoids unnecessary cost spending during the PCB design stage [6-11].

Moreover, the PCB design is only good when the overall product specifications are met, where this PCB can be manufactured with a good yield [5]. Researcher from [1-3] has reported that the selection of the components in a PCB for high-speed test can cause problems at operating frequencies above 1 GHz. As explained before in Figure 2.1, a test system setup involves a PCB in contact with external supporting tools, which are required to be integrated while the device is being tested. Each device in the test mode has to be tested while experiencing extremely high-speed movements by the automated test handler, with required force in contact with test pogo pins implanted into the PCB. Any broken signal from the PCB to the device under test will have an impact on the overall signal integrity of the DUT, and lead to failures [4-8]. A high failure rate is wasteful from the cost and the productivity perspective.

Every small discontinuity in a PCB has to be considered carefully, especially the vias used in the PCB for a multi-layer test board. Study from [4], clearly demonstrates that as the frequency increases, via causes impedance loss, which results in signal reflections, therefore deteriorating the signal integrity of the overall PCB. Packages that operate at higher clock speeds (more than 200 MHz) with shorter rise times (less than 1 ns) and faster data rates (more than 1-Gbps) present a tremendous challenge in PCB manufacturing. Signal problems seen will affect high-speed circuit functionality if the physical designs of the vias are not considered. Studies concluded that signal propagation delay due to via design and its placement resulted in a significant problem that cannot be ignored [14-17].

This section summarizes how important is it to collaborate and innovate on high-speed test design in a PCB even if there is an established design rule available [5]. Improper PCB design leads to various signal integrity issues, resulting in transmitted signal distortion [6-7]. Moreover, common causes of signal integrity in a PCB are due to crosstalk and reflections [6-8]. Designing with extra precaution that identifies risk factors involved is essential to ensure product requirements are met at all times and ensuring that design profitability [4-6] is achieved in today's leading edge high-speed data rate test in semiconductors.