A STUDY AND DEVELOPMENT OF DIGITAL CONTROL TECHNIQUE FOR POWER FACTOR CORRECTION USING PRE-CALCULATED ALGORITHM WITH A LOW COST 8-BIT MICROCONTROLLER

by

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LIST OF ABBREVIATIONS

SMPS	Switch Mode Power Supply
AC	Alternating Current
DC	Direct Current
PF	Power Factor
PFC	Power Factor Correction
FPGA	Field Programmable Gate Arrays
DSP	Digital Signal Processor
ASIC	Application Specific Integrated Circuits
IC	Integrated Circuits
THD	Total Harmonic Distortion
F_{DF}	Current Distortion Factor
F_{DA}	Displacement Angle
ACMC	Average Current Mode Control
PWM	Pulse Width Modulation
PI	Proportional Integral
ADC	Analog to Digital Converter
SDR	Stored Duty Ratio
RMS	Root Mean Square
EPROM	Erasable Programmable Read Only Memory
OPA	Operational Amplifier
MIPS	Million Instructions Per Second
SAR	Successive Approximation Register
SA	Settling Accuracy

LSB	Least Significant Bit
AMUX	Analog Multiplexer
RMS	Root Mean Square
V_p	Peak Voltage
CCM	Continuous Conduction Mode
VEC	Voltage equilibrium Component
CFC	Current Forcing Component
PWM	Pulse Width Modulation
CPU	Central Processing Unit
IDE	Integrated Development Environment
DCM	Discontinuous Conduction Mode
CCM	Continuous Conduction Mode
OTP	One Time Programmable
LQFP	Low Profile Quad Flat Package
RMS	Root Mean Square
EMI	Electromagnetic Interference

PEMBANGUNAN TEKNIK KAWALAN DIGITAL UNTUK PEMBETULAN FAKTOR KUASA MENGGUNAKAN ALGORITMA SEDIA-KIRA DENGAN MIKROPENGAWAL 8-BIT KOS RENDAH

ABSTRAK

Kualiti tenaga elektrik yang diedarkan telah menjadi satu keprihatinan yang tertumpu pada tahun-tahun kebelakangan ini. Dalam usaha untuk memenuhi piawaian antarabangsa dalam pengurangan pembebasan harmonik daripada kebanyakan bekalan kuasa mod suis AC-DC, pembetulan faktor kuasa adalah diperlukan. Tradisional pembetulan faktor kuasa dalam mod suis bekalan kuasa kebanyakan dilaksanakan dengan pengawal analog. Teknologi yang matang dalam pembuatan peranti digital telah membawa kepada proliferasi pengawal digital yang bukan sahaja canggih malah kos lebih rendah. Ini membolehkan kemungkinan pelaksanaan teknik pembetulan faktor kuasa digital dalam cara yang lebih berdaya saing. Teknik kawalan digital untuk pembetulan faktor kuasa menggunakan algoritma pra-kiraan dengan 8-bit mikropengawal kos rendah telah dibentangkan dalam penyelidikan ini. Dalam aplikasi teknik ini, kitaran tugas bagi tempoh separuh kitaran talian AC yang sudah dikira luar talian akan disimpan ke dalam memori peranti. Faktor kuasa hampir kesatuan boleh dicapai dengan pemadanan nilai talian voltan AC kepada nilai paparan jadual di dalam memori untuk masa operasi tertentu. Kelebihan utama strategi ini bukan sahaja tidak memerlukan pengukuran arus elektrik malah tidak memerlukan peranti digital yang canggih lagi mahal. Satu prototaip pembetulan faktor kuasa yang dikawal oleh mikropengawal 8-bit dengan kit pembangunan telah disediakan untuk melaksanakan teknik yang dicadangkan bersama dengan keputusan yang didapati dalam simulasi. Kedua-dua keputusan simulasi dan eksperimen telah menunjukkan

trend positif bahawa strategi yang dicadangkan untuk pembetulan faktor kuasa hampir mencapai kesatuan faktor kuasa yang disasarkan.

A STUDY AND DEVELOPMENT OF DIGITAL CONTROL TECHNIQUE FOR POWER FACTOR CORRECTION USING PRE-CALCULATED ALGORITHM WITH A LOW COST 8-BIT MICROCONTROLLER

ABSTRACT

The quality of distributed electrical power has become an acute concern in recent years. In order to comply with the requirements of international standards of harmonics emission in most of the AC-DC switched mode power supply, power factor correction is essential. Power factor correction in switched mode power supply has been implemented with analog controller conventionally. The mature manufacturing technologies in digital devices has led to the proliferation of powerful yet low cost digital controllers and enable the possibility of digital power factor correction implementation in a more competitive way. A digital control technique for power factor correction using pre-calculated algorithm with a low cost 8-bit microcontroller is studied and presented in this paper. Based on this technique, the duty cycles for half a line period are computed offline and stored into the device memory. A nearly unity power factor can be achieved based on the AC voltage line synchronization with the look up table in the memory at specific operating point. The primary advantages of this strategy are neither current measurement nor powerful yet expensive digital device are required. A prototype of boost power factor correction controlled by an 8-bit microcontroller development board was set up to implement the proposed technique. Both simulation and experimental results are showing positive trend that the proposed strategy for power factor correction achieves near unity power factor.

Chapter I

INTRODUCTION

1.1 Overview

Long before the creation of switch mode power supply (SMPS), linear power supply was the only power supply available in the market. In order to increase the efficiency and at the same time to reduce the weight and size associated with AC power to DC power conversion in linear power supply, SMPS was introduced. A SMPS make use of the methodology of switching a transistor to convert electrical power efficiently in order to fulfill different power requirement. However, due to the high nonlinearity of this kind of power electronic systems, it introduces low power factor (PF) and high total harmonic distortion (THD) to the electrical grid which is normally unfavorable by the utility company. These unwanted harmonics usually can be corrected by incorporating power factor correction (PFC) technique into the SMPS.

The increased severity of power quality in power utility has attracted the attention of power engineers around the world to develop dynamic and adjustable solutions to minimize the power quality problems. Yet, the requirement to meet the compliance of European standards for the regulation of low frequency current harmonics such as the publication of IEC-1000-3-2 and later adopted to regional standards as EN-61000-3-2 has become one aspect of most important issue to arrange for harmonic pollutions (Reid, 1996; Agilent Standard Application Note, 2000; Limits for Harmonic Current Emissions, 2000; Grady, 2001). Great efforts have been put

forward by the researchers to develop more efficient power electronic systems in order to comply with these standards.

Thus, high PF operation as well as the reduction of input current harmonics is an important requirement for modern power supplies. Due to the stringent standards and regulations as well as the dynamic power range of the load, active PFC technique is more preferable over the conventional passive PFC technique. Although passive PFC technique may be simpler to implement and cost lower, the superiority of the instantaneous response of the active PFC over the wider and more dynamic range of control yield better performance than passive PFC.

As known, nowadays most of the control of SMPS has traditionally been a purely analog domain and there was no exception for the PFC implementation. The advent of low cost, high-performance digital controllers has opened a room for improvement for PFC control, and providing us the chances of heading toward digital revolution for digital PFC implementation. In comparison with their analog-controlled counterpart, with the similar small form factor of their analog counterpart, the digital controller can provide feature-packed peripherals, competitive size and cost yet more flexibility as well as faster design turn-cycle. Most importantly, digital controller offer performance advantages such as better immunity to environmental variations, less susceptible to input voltage distortion, adaptability, etc. that would be impossible to be achieved through analog techniques.

In this research, a pre-calculated duty cycle optimization technique is proposed as a digital implementation of PFC controller. Algorithm of the optimization technique is studied and developed in C programming language then

integrated into a low cost 8-bit microcontroller with minimal component count and without extra analog components.

1.2 Power Factor

Power factor is the percentage of electricity that is used to carry out useful work. Given in equation 1-1, power factor can be defined as the ratio of True Power in watt over the Apparent Power in volt-amperes.

$$power\ factor = \frac{P}{S} = \cos\theta \qquad (1\text{-}1)$$

Where P is the True Power, S is the Apparent Power and θ is the phase angle.

The Apparent Power also referred as total power delivered by utility company and consists of two components as illustrated in Figure 1.1.

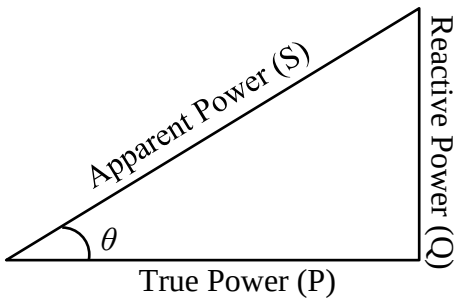

Figure 1.1 Power triangle relating apparent power to true power and reactive power.

The True Power is the actual amount of power that powers the load and carries out the useful work while the Reactive Power is the energy that is stored temporarily in inductive and capacitive elements in the form of magnetic or electric fields and then returned to source.

If both the current and voltage are sinusoidal and in phase, a power factor of unity can be achieved. However, when both the current and voltage are sinusoidal but not in phase, the power factor is the cosine of the phase angle, θ as illustrated in Figure 1.1. This definition only applies in special case where both the current and voltage are purely sine waves and when the load is composed of linear resistive, capacitive and inductive elements (On Semiconductor Corporation Standard Application Note, 2011).

Due to the nature of the input circuitry, SMPS tends to present nonlinear impedance to the mains. The input circuit usually comprises of a half-wave or full-wave rectifier followed by a bulk storage capacitor capable of maintaining a voltage of around the peak voltage of the input sine wave until the subsequent recharge of the capacitor from the next peak voltage. In this case, current is drawn from the input only at the peaks of the input waveform, and this pulse of current must contain sufficient energy to sustain the load until the next peak. This is done by transferring a large charge into the capacitor within a short duration, after which the capacitor slowly discharges the energy into the load until the cycle repeats. It is common for the current pulse to be 10% to 20% of the cycle, meaning that the current during the pulse must be 5 to 10 times the average current as illustrated in Figure 1.2 (On Semiconductor Corporation Standard Application Note, 2011). Shown in Figure 1.2, the current and voltage are perfectly in phase despite of the acute current waveform distortion. In this case applying the “cosine of the phase angle” definition as mentioned above would cause erroneous conclusion that this power supply has a power factor of unity. In lieu of that, Figure 1.2 should be analyzed using the definition of total harmonic distortion which closely ties with power factor as discussed in the following section.

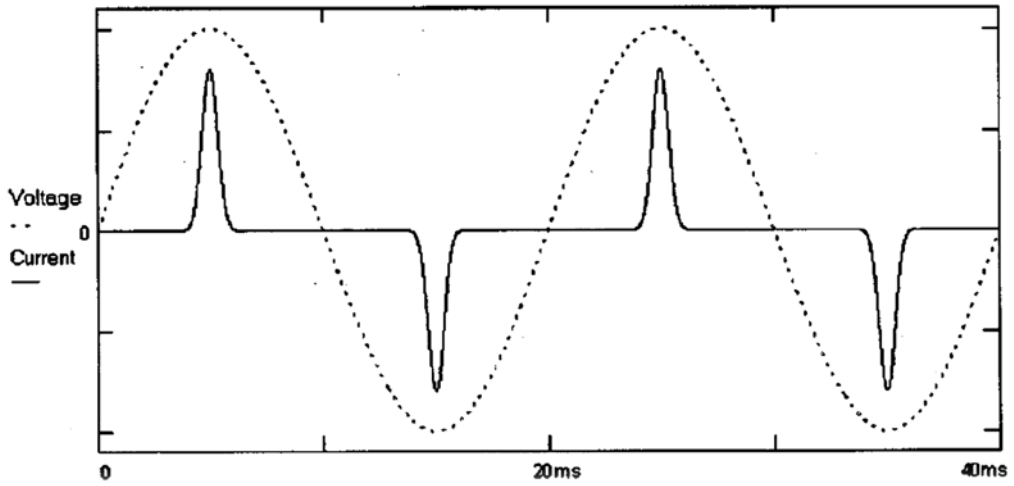

Figure 1.2 Input Characteristics of a typical SMPS without PFC (Agilent Standard Application Note, 2000).

1.3 Total Harmonic Distortion

Total harmonic distortion (THD) is defined as the quadratic sum of the undesirable harmonic components over the fundamental component that gives the relative weight of the harmonic content with respect to the fundamental component (On Semiconductor Corporation Standard Application Note, 2011). The total harmonic distortion is given by equation 1-2 in the following.

$$THD(\%) = 100 \cdot \frac{\sqrt{\sum_{n=2}^{\infty} I^2_{n,rms}}}{I_{1,rms}} \qquad (1\text{-}2)$$

Total harmonic distortion has a direct relationship with power factor where the displacement factor relates the fundamental current phase φ_1 to the fundamental voltage phase θ_1 and is given in equation 1-3; the distortion factor relates the fundamental rms current to the total current and is given in equation 1-4. The

definition of power factor is the product of the displacement factor with the distortion factor and given in equation 1-5 and equation 1-6 with no DC current component.

$$displacement\ factor = \cos(\varphi_1 - \theta_1) \quad (1\text{-}3)$$

$$distortion\ factor = \frac{I_{1,rms}}{I_{rms}} \quad (1\text{-}4)$$

$$Power\ Factor = (distortion\ factor)(displacement\ factor) \quad (1\text{-}5)$$

$$Power\ Factor = \left(\frac{1}{\sqrt{1+(THD)^2}}\right) \cdot \cos(\varphi_1 - \theta_1) \quad (1\text{-}6)$$

Hence, equation 1-6 demonstrated that in order for power factor to be one, the THD has to be zero (On Semiconductor Corporation Standard Application Note, 2011).

1.4 The Importance of Power Factor Correction

Most of the commercial and industrial installations have large electrical loads which are inductive in nature, such as motors, air conditioners, etc. which results in a lagging of current with voltage phase and contributes to the low power factor. Interestingly enough, the very technology that allows for more efficient utilization of electric energy, switch mode power supply (SMPS) is also a culprit that can negatively impact the power quality.

Power factor as given in the equation 1-1 is the ratio of the True Power with respective to Apparent Power. Power factors of loads below unity draw more than the necessary minimum volt-amperes (VA) in order to supply the True Power in watts. This increases generation and transmission costs where part of the energy is wasted. For instance, if the load power factor was as low as 0.5, the Apparent Power would be

twice the True Power needed by the load. On the other hand, while it is at unity power factor, the Apparent Power is only equal to the True Power required by the load. This implied that the actual Apparent Power needed to carry out the work load needed by the same True Power has been doubled if the power factor is 0.5.

Utilities companies typically charge additional costs to customers who have a power factor below some limit, which is typically 0.85 to 0.90. According to the guidelines published by Tenaga Nasional Berhad, a minimum power factor of 0.85 is needed for voltage lower than 132 kV and 0.90 for voltage level 132 kV and above (Tenaga Nasional Berhad Standard Application Note, 2007). Thus, power factor of a load always be the concerns of power engineers as one of the factors that may affect the efficiency of power conversion especially in SMPS.

With the rising cost of energy and concerns over the efficient delivery of power, active power factor correction has gained popularity in most of the consumer electronics in the market nowadays (On Semiconductor Corporation Standard Application Note, 2011). In Europe, IEC 1000-3-2 and IEC 1000-3-3 require power factor correction to be incorporated into consumer products in order to regulate the amount of permissible harmonics emission to the electrical grid that would burden the power distribution system with excessive neutral current (Agilent Standard Application Note, 2000).

In low voltage supply system, power factor correction is equally important. This is especially true when equipment connected to the same branch circuit may operate improperly due to EMI (Electromagnetic Interference) issue from severe voltage distortion caused by interference of harmonic current with impedances in the distribution system. The strength of the magnetic field that is built up around a wire is

proportional to the pulse rate of the current in the wire. The instantaneous changing of the current pulses emits a stronger electrical noise signal than a normal sinusoidal current and may result in an audible hum in other equipment, flickering display on monitors or filament lamp, or interference with the operation of sensitive electronic equipment such as those are commonly found in medical devices and telecommunication facilities. The IEC 1000-3-2 standard specifies the limits for harmonic currents created by equipment connected to public low-voltage supply system while IEC 1000-3-3 standard address limits for voltage fluctuations as well as flicker produced by equipment connected to public low-voltage supply system in order to ensure that voltage disturbances in electrical distribution system do not interfere with other equipment connected to the AC mains or cause light flickering that might impose health risk to human observer (Electromagnetic Compatibility Fact Sheet, 1995; Agilent Standard Application Note, 2000; Danfoss Group Whitepaper, 2011).

1.5 Problem Statement

Due to the exhaustive algorithm calculation needed in multiplication and division, a more expensive digital control devices such as field programmable gate arrays (FPGA), digital signal processors (DSP) or application specific integrated circuits (ASIC) normally will be the primary options for digital implementation of PFC. Other than that, the complexity in inductor current sensing for the implementation of the common average current mode control technique has always been a troublesome concern. Thus, in this research the potential of a low cost 8-bit microcontroller will be explored using a more economical technique without extra analog components.

1.6 Research Objective

Objective of this research is:

1. To use a lower cost 8-bit microcontroller with lower components count as the digital processing core for development of PFC control.
2. To integrate the proposed pre-calculated duty ratio technique without the need of inductor current sensing technique.
3. To implement the sensing and control technique without the need of extra analog components such as op-amps, UC3854 analog control chip, external EPROM, etc.

1.7 Research Hypothesis

A lower cost 8-bit microcontroller is able to carry out PFC tasks using pre-calculated algorithm technique with voltage sensing. Hence, a significant of cost saving as well as the wider use of digital implemented PFC controller can be promoted.

1.8 Research Scope

In this research, the digital implementation of PFC from existing works using different techniques such as average current mode control has been studied and analyzed. It was found that most of the designs of the digital implementation were built using high performance digital control devices such as FPGA, DSP and some of them together with the assistance of their analog counterpart to reduce the complexity of the architecture. In order to enjoy the pros of digital implementation without

compromising the cost as compared to the existing analog PFC IC available in the market, pre-calculated duty cycle optimization technique is proposed to be used in this research. Pre-calculated duty cycle optimization algorithm built in C language will be integrated into a low cost 8-bit microcontroller with low component count using the current boost topology as the primary development architecture.

1.9 Important and Contribution of Research

The goal of PFC controller is to increase the power factor by reducing the total harmonic distortion pollution to the utility power system. The PFC controller will shape the input current in order to maximize the real power delivered by the utility company.

Conventional implementations of PFC were all in analog domain with its own limitations. In order to meet the stringent standards and regulations, many new techniques were being developed using the digital implementation instead of analog. Due to the nature of most of the techniques involved were resources intensive, a more advanced and higher performance of digital controller is a must. This direct incurs cost concern and constraints to the popularity of digital PFC over their analog counterpart in the market though digital implementation may bring more improvement and flexibility to the PFC field.

In this research, a pre-calculated duty cycle optimization technique is proposed as a digital implementation of PFC controller. Algorithm of the optimization technique is developed in C programming language and integrated into a low cost 8-bit microcontroller with minimal component count and without extra

analog components. As a result, a low cost 8-bit microcontroller is able to carry out PFC tasks using pre-calculated algorithm technique with only voltage sensing. Hence, a significant of cost saving as well as the wider use of digital implemented PFC controller can be promoted.

1.10 Thesis Structure

This thesis is organized into five chapters. Chapter I give an overview of the research. It covers research's background, importance of PFC, problem statement, objectives, hypothesis, scope as well as its importance and contribution in power electronics design world. Chapter II provides a detail literature review of the research. It introduces the boost PFC converter operation and discusses the existing techniques in digital PFC control as well as their limitations in implementation. Chapter III introduces an overview of the system and explains the methodology in pre-calculated duty ratio algorithm for digital PFC control in depth. The methodology proposed here eliminates the expensive current sensing technique with only voltage sensing. Other than that, the design and implementation in hardware as well as software control for the digital PFC system are presented. In Chapter IV, experimental result, analysis and discussion on the implementation of pre-calculated duty ratio algorithm in digital PFC control are presented. Chapter V is the last chapter of this thesis. It concludes the thesis and discusses on the potential future work for this research.

Chapter II

LITERATURE REVIEW

2.1 Introduction

This chapter provides a detail review of the fundamental operation and the topology used in PFC converter as well as the digital techniques available nowadays. Comparisons are made between the pros and cons of these techniques along in the discussion in this chapter. This chapter serves in establishing the theoretical frameworks along with their underlying theories from previous works and is being reviewed here.

2.2 Boost PFC Converter

Boost PFC converter has been the most popular topology used in active PFC circuitry up until now due to its self PFC capability. Although other topologies such as buck-boost and fly-back converter also having excellent performance in PFC, the greater saving and simplicity make boost topology more favorable than others (Garcia et al., 2003; Nussbaumer et al., 2009; Wei & Batarseh, 1998; Madigan et al., 1992). Boost converter can easily build with only one active switch together with an inductor and a diode. The switching frequency will control the allowable level being stepped up in this case. As illustrated in Figure 2.1 is the diagram of a basic boost PFC converter

found in SMPS, where L, D, S, C and, R_L denotes inductor, diode, switch, capacitor and resistive load respectively.

In its simplest form, PFC boost converter is built from a DC-DC step up converter led by a rectifier bridge. From the AC line, the sinusoidal input voltage v_{ac} goes through the line filter and is rectified by the full bridge rectifier generating the rectified voltage v_{rec}. A full bridge rectifier converts the whole sinusoidal input waveform to one of constant polarity which is positive polarity in this case at its output. In order for the boost converter to operate properly, the output voltage v_o need to be always higher than the maximum value of input voltage $|v_{ac}| = v_{rec}$ for steady-state operation (Kazimierczuk, 2008). The AC line sinusoidal voltage is given by,

$$v_{ac}(t) = V_m \sin(\omega t) \tag{2-1}$$

The voltage at the output of the front-end full bridge rectifier is given by,

$$v_{rec} = |v_{ac}(t)| = V_m|sin(\omega t)| \tag{2-2}$$

Thus, the duty cycle *d(t)* is given by,

$$M(t) = \frac{v_o}{v_{rec}} = \frac{v_o}{V_m|sin(\omega t)|} = \frac{1}{1-d(t)} \tag{2-3}$$

$$\therefore d(t) = 1 - \frac{v_{rec}}{v_o} = 1 - \frac{V_m|sin(\omega t)|}{v_o} = 1 - \frac{\sqrt{2}v_{ac}(t)}{v_o} \tag{2-4}$$

From (2-4), the maximum duty cycle where *d(t)*=1 will only occur at ωt =0, π,2 π while the minimum duty cycle will occur at $\omega t = \pi/2$,3 $\pi/2$. In order to achieve a high PF, the sinusoidal input current i_{ac}, need to be in-phase with the input voltage v_{ac} and THD free (Kazimierczuk, 2008). A detail operation of boost PFC converter is explained in Section 2.2.1 followed by the PFC control techniques in Section 2.3.

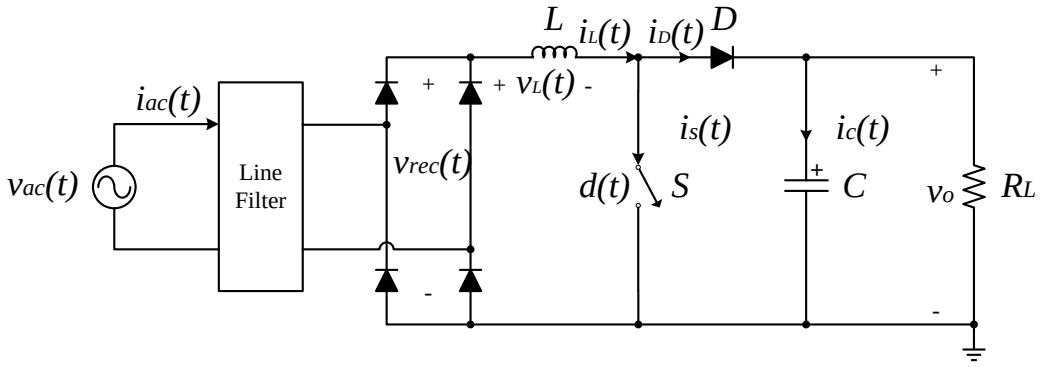

Figure 2.1 Boost PFC converter with AC-DC rectification.

2.2.1 Boost PFC Converter Operation

The principles of operation of the converter are depicted in Figure 2.2 and Figure 2.3. During the first positive half cycle of the AC line, for time interval $0 < t < DT$, switch S is closed. As a result, the voltage across the diode is $v_D = -v_o$, causing the diode in reverse biased while the voltage across the inductor is $v_L = v_{rec} = \sqrt{2} \cdot v_{ac}(t)$. Consequently, energy is stored as magnetic field in inductor L. The switch S current is equal to the inductor current.

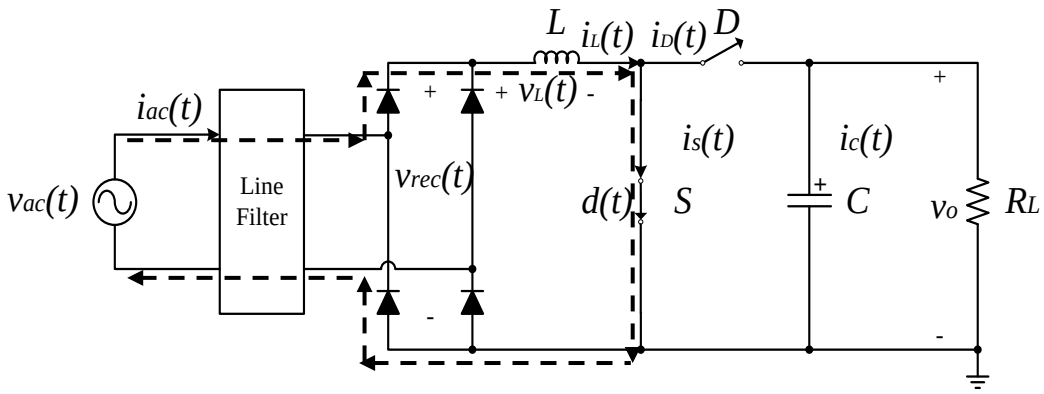

Figure 2.2 Positive AC half cycle with switch S closed in Boost PFC converter.

In the same half cycle, the switch *S* is opened corresponding to $t = DT$. The inductor now acts as a current source and turns the diode on. The voltage across the inductor become $v_L = \sqrt{2} \cdot v_{ac}(t) - v_o < 0$. The diode current equals to the inductor current. Hence, energy is transferred from the inductor *L* to the filter capacitor *C* as well as the load resistance R_L as illustrated in Figure 2.3. At time $t = T$, the switch is turned on again, terminating the cycle. These cycles continue to repeat as the AC half cycle goes to the negative half cycle as well.

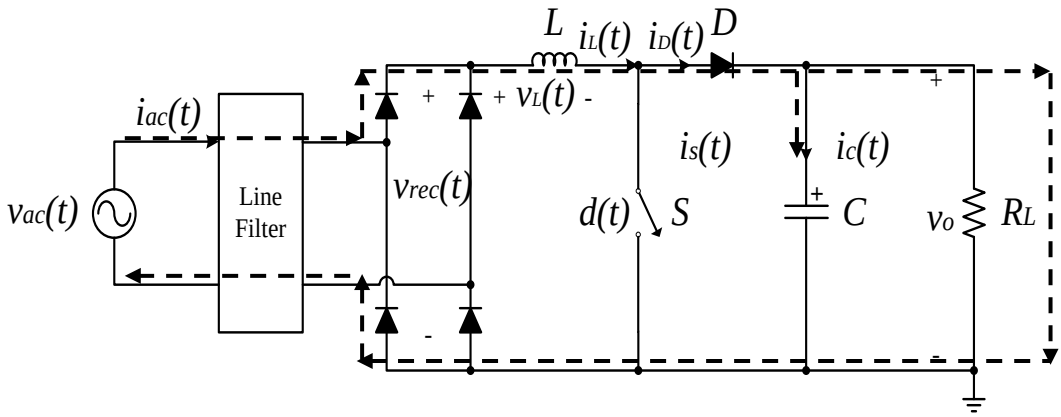

Figure 2.3 Positive AC half cycle with switch S opened in Boost PFC converter.

In order to have a better view of the operation of the boost PFC converter, detail waveforms of the operation mechanism are indicated in Figure 2.4. Shown in the plot are *d(t)*, the duty cycle of the boost converter, $v_L(t)$ and $i_L(t)$, the voltage and current across the inductor, $v_D(t)$ and $i_D(t)$, the voltage and current across the diode, $v_S(t)$ and $i_S(t)$, the voltage and current across the switch S.

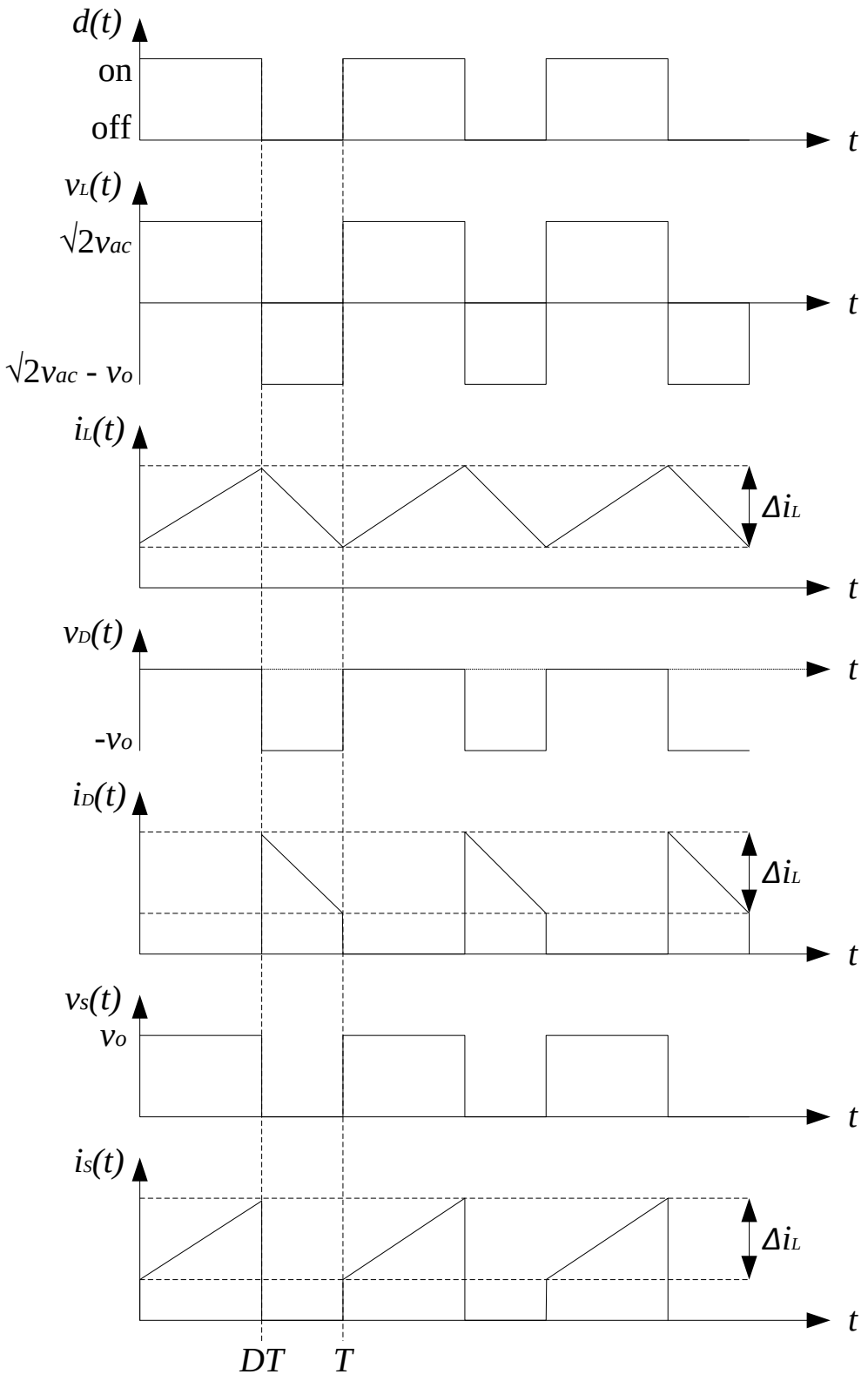

Figure 2.4 Ideal current and voltage waveforms of boost converter operation.

With the control of switch S, the boost converter can inherit the ability of PFC by making the $i_{ac}(t)$ sinusoidal and in-phase with the input voltage $v_{ac}(t)$ instead of stepping up a constant DC v_o at the output. The inductor current is shaped to have a full-wave rectified waveform given by,

$$i_L(t) = I_{Lmax}|sin\omega t| \tag{2-5}$$

where the input current of the rectifier is,

$$i_{ac} = I_{acmax}sin\omega t = I_{Lmax}sin\omega t \tag{2-6}$$

Shown in Figure 2.5 and Figure 2.6 are the visual illustrations of the phenomenon explained above.

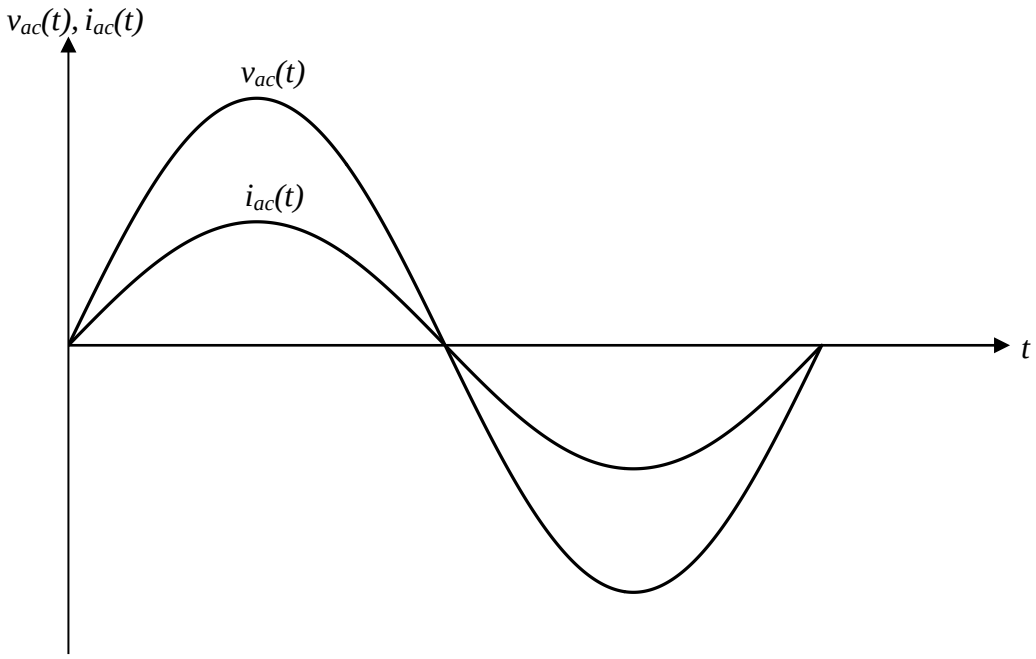

Figure 2.5 Waveforms of the line voltage v_{ac} and line current i_s.

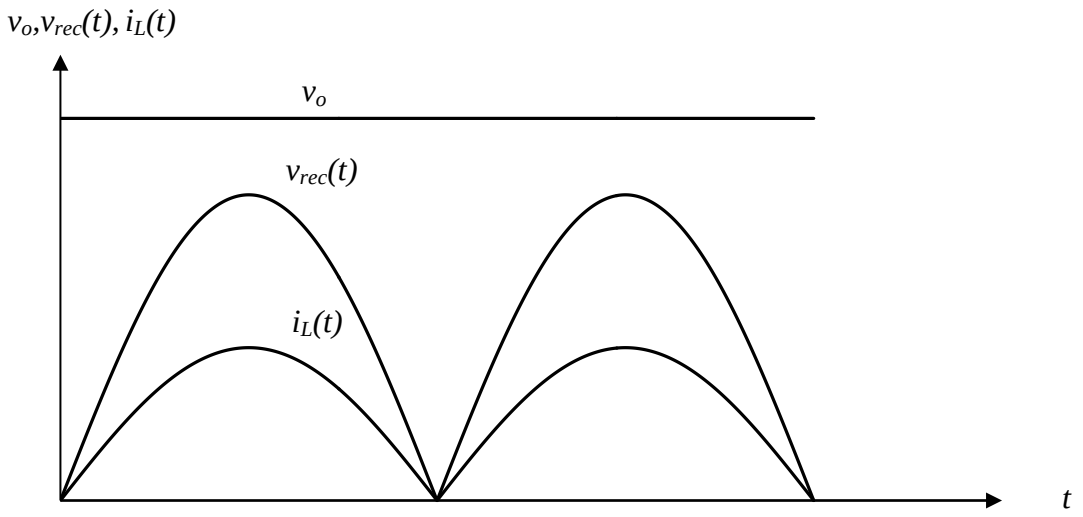

Figure 2.6 Waveforms of rectified line v_{rec}, v_o and i_L.

Hence, the input impedance of the boost converter at the utility line frequency is a linear resistance, yielding THD = 0 and current distortion factor F_{DF} = 1. The line current is in phase with the line voltage, thus yielding displacement angle F_{DA}= cos φ = 1. As a result, PF = 1. THD, F_{DF} and F_{DA} are given by the following expressions.

Displacement angle, $F_{DA} = \cos(\varphi_1 - \theta_1)$ (2-7)

Where φ_1 is the fundamental current phase and θ_1 is the fundamental voltage phase.

Current distortion factor, $F_{DF} = \frac{I_{1,rms}}{I_{rms}}$ (2-8)

Where $I_{1,rms}$ is the fundamental component of current in rms and I_{rms} is the total rms current.

$$THD = \sqrt{\frac{1}{PF^2} - 1} \quad (2\text{-}9)$$

Where THD is total harmonic distortion and PF is power factor.

2.3 Review of Boost PFC Digital Control Technique

A conventional analog PFC is achieved by sensing the line voltage and the inductor current thus deriving a feedback signal that is used to control the duty cycle of switch (Hirachi & Nakaoka, 2003; Chen & Sun, 2006; Liu et al., 2006). Following the development in digital techniques, digital control algorithms are developed and implemented using the conventional Average Current Mode Control (ACMC) technique that has been practiced in analog but replacing the original analog part with digital controller in order to benefit from the advantages of digital control (Gegner & Lee, 1996; Mitwalli et al., 1996; Zane & Maksimovic, 1998; Fu & Chen, 2001; Kim & Enjeti, 2003; Prodic et al., 2003; Jakobsen et al., 2005; Guo et al., 2006; Zhang et al., 2006; Prodic et al., 2006; Wang et al., 2008; Garcia et al., 2009; Azcondo et al., 2009; Lopez et al., 2010; Shin et al., 2010).

The only drawback of digital PFC implementation is computational resource hunger. However, with mature technology available and the introduction of faster yet affordable digital device such as DSP (Zhang et al., 2002; Zhang et al., 2004; Zhang et al., 2006; Kim & Enjeti, 2003) and FPGA (Zhang et al., 2006; Garcia et al., 2009; Chen et al., 2012) in the market, digital PFC implementation is no longer a dream. The following section provides the most common used digital control method with boost PFC converter topology.

2.3.1 Average Current Mode Control

Average current mode control (ACMC) is typically a two loop control method with inner current loop as well as outer voltage loop for power electronic converters. The inductor is covered within the inner current control loop which simplifies the design of the outer voltage control loop and improves the power supply performance. This has been the most popular technique used in achieving high PF and low THD in analog as well as digital boost PFC converter (Buso et al., 1998; Shin et al., 2010; Fu et al., 2001; He & Nelms, 2004; He & Nelms, 2005; Jakobsen et al., 2005). A simplified ACMC circuit block diagram is illustrated in Figure 2.7.

ACMC attempts to control the average value of the current to follow a reference as opposed to controlling the switch peak current. The current loop monitors and maintains the switch current or inductor current equal to a reference current. This reference current is obtained by the voltage loop, which compares a reference voltage and the output voltage of the boost PFC converter. An ACMC converter has good dynamic response for input and output disturbances (He & Nelms, 2004).

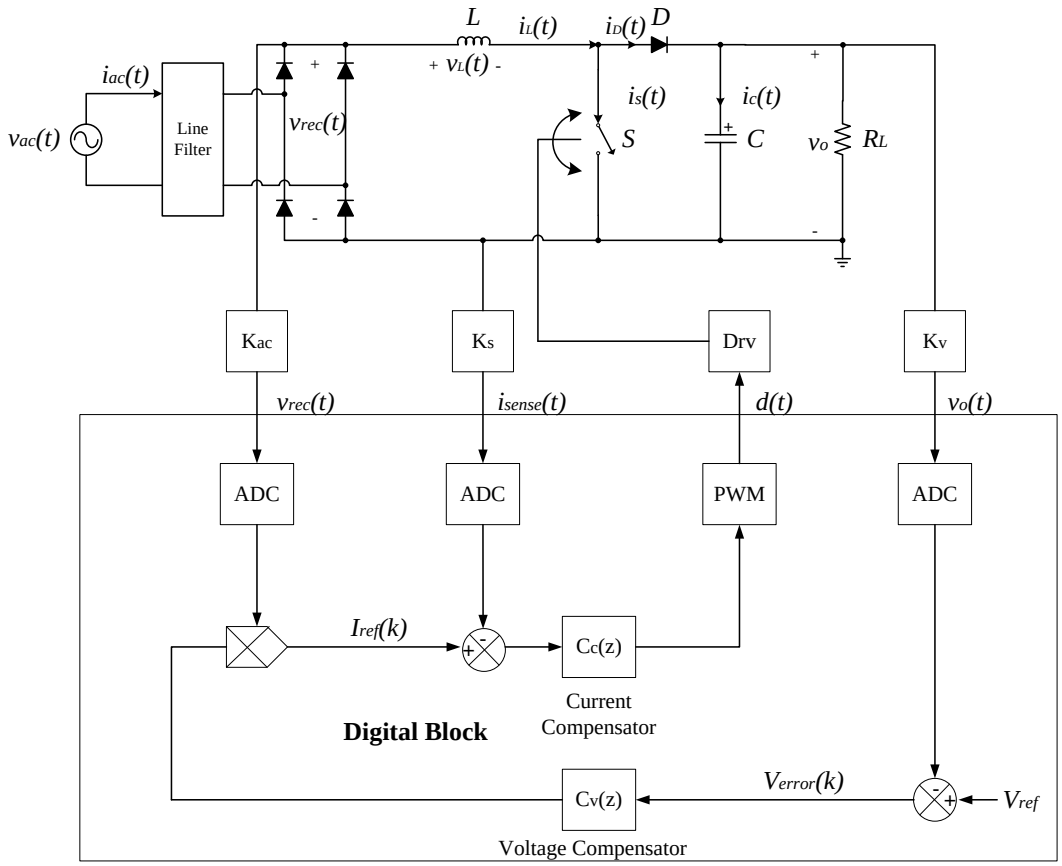

Figure 2.7 Digital ACMC for boost PFC converter.

In an ACMC system, a current amplifier is inserted into the current loop to obtain the average value of the inductor current. ACMC has several important advantages. Firstly, average current tracks the current program with a high degree of accuracy which is critical especially in high power factor pre-regulators, resulting less than 3% THD to be achievable with a small inductor. ACMC even functions well when the mode boundary is crossed into discontinuous mode at low current level with the monitoring of the outer voltage control loop.

Secondly, slope compensation is no longer required and the noise immunity is excellent. When the triggering pulse turns the power switch on, the oscillator ramp immediately go into its lowest level, avoiding corresponding current error level at the

input of the PWM comparator. Since the average current is used as a controlled quantity, ACMC is particularly suitable for PFC and applications where a constant current source is needed.

2.3.2 Conventional Digital PFC Control Limitations

The existing digital implemented PFC has several constraints. First, the switching frequency is limited in the conventional digital control PFC due to the time delay in sampling, computations and necessary processing time. In addition, even operating at a low switching frequency, the high performance digital processing device is still exclusively constraint by the PFC stage in SMPS.

Secondly, the higher the switching frequency, the faster the speed of digital processing device is needed. Thus, the popularity of digital control PFC implementation will be bottle-necked by the higher cost introduced. Thirdly, even if the fastest digital processor is used in the digital PFC implementation, the switching frequency cannot reach as the same in analog control since analog control process all the information in real time with minimal of delay.

ACMC also the primary concept used in analog control technique, and is widely been adopted into digital control PFC (Buso et al., 1998; Fu et al., 2001; He & Nelms, 2004; He & Nelms, 2005; Jakobsen et al., 2005; Chen et al., 2007; Shin et al., 2010;). As shown in Figure 2.6, the average inductor current i_L, is forced to follow the reference current I_{ref}, which is proportional to the rectified voltage v_{rec}, in order to achieve unity power factor. In digital ACMC control, the digital processing device is utilized to compute the duty cycle in every switching cycle based on the feedback

from inductor current i_L and the reference current I_{ref}. After that, the calculated duty cycle will be used to control the switch S, to maintain a unity power factor.

In article (Zhou et al., 2001), single period single sampling technique is implemented. A DSP is utilized to control the switching of gate signal in the frequency of 50 kHz. The digital ACMC was adopted in the realization of the digital PFC control. The processes implemented in digital control include voltage and current sampling, voltage and current error computation, voltage and current PI regulation, reference voltage and reference current computation, as well as PWM generation. Approximations of 11 arithmetic operations are necessary for the calculation in each switching cycle. Furthermore, extra instructions cycle is required for the execution of the computed PWM through the output I/O port within the time frame of each switching cycle. Due to the need of execution of these processes iteratively in every switching cycle, most of the resource of the processor is occupied. Hence, the switching frequency is constraint by the speed of the DSP itself as mentioned earlier above. This is a commonly known drawback to all existing digital ACMC based implementation of PFC.

In order to solve the tight computation time above, presented in articles (Zhou et al., 2001; Bibian & Jin, 2001; Guo et al., 2006) was a method of reduced duty cycle update by updating the duty cycles once in several or several tens switching cycles. Additional computation is reduced due to the infrequent update of duty cycle thus freeing the resources of the processor. However, this might induce the possibility of rising harmonic in the line current controlled by this method since no instant feedback correction in real time.

Presented in articles (Chen et al., 2003; Zhang et al., 2003; Zhang et al., 2004; Zhang et al., 2006) a predictive algorithm control was investigated and implemented in digital PFC system. In order to predict the next switching cycles, based on the sampled current, input and output voltage, the duty cycle of the next switching period is calculated in advance. More or less the same to the ACMC, control method is based on the idea of the duty cycle is calculated but in advance in every switching cycle. Therefore, its computation requirement is no less than that in ordinary digital ACMC implementation.

In order to solve the above constraints, several control strategy were exploit. The first approach is a combination of a digital processor with an analog PFC control IC such as UC3854 (Mitwalli et al., 1996). Analog control IC is used for inner loop and to determine the duty cycle directly. The DSP only process the low frequency operations for the outer voltage loop thus free up the DSP resources and no complicated calculation needed. Since this architecture involves both DSP and analog IC, the cost is increased.

The second approach is a combination of FPGA with an analog to digital converter (ADC) (Zumel et al., 2002; de Castro et al., 2003). In this approach, special design of a simple PFC control algorithm, “a digital version of charge control” is essential in order to implement in FPGA. The algorithm will control the turn on of the switch at the starting and turn off when the mean value of the input current reaches the reference value. The mean of the input current is the sum of the input current samples divided by the number of samples in one switching cycle. In order to maintain a satisfactory resolution, a fast ADC is desired in the integral task for the computation of mean input current value. Thus, this will increase the overall cost of the architecture. In addition, there is a compromise between the duty cycle resolution