DESIGN AND ANALYSIS OF A FAST TRANSIENT VOLTAGE REGULATOR WITH ALL CERAMIC OUTPUT CAPACITORS FOR MOBILE MICROPROCESSORS

By

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ABSTRAK

Keperluan untuk mereka bentuk pengatur voltan yang mempunyai tindak balas transien yang cepat didorong oleh kadar transien yang semakin meningkat daripada mikropemproses mudah alih. Oleh itu, mengoptimumkan frekuensi pensuisan pengatur voltan menjadi langkah penting untuk mencapai keseimbangan antara mengekalkan kecekapan pengatur voltan dan meningkatkan tindak balas transien. Kapasitor seramik berlapis telah menjadi lebih popular sebagai kapasitor output pengantara voltan disebabkan oleh saiznya yang kecil dan kos murah.

Walaupun topologi penukar buck kekal tidak berubah betahun-tahun, terdapat banyak inovasi dan kejayaan cemerlang dalam peringkat kuasa pengatur voltan dan teknologi kawalan. Selain itu, reka bentuk yang berorientasikan galangan keluaran dan AVP (Penempatan Voltan Automatik) telah diperkenalkan untuk menangani keperluan transien. Banyak kajian juga memberi tumpuan untuk meningkatkan kecekapan pegantara voltage terutama untuk system yang beroperasi dengan bateri.

Sebuah pengatur voltan bertindak balas laju yang mempunyai hanya kapasitor output seramik untuk mikropemproses mudah alih dicadangkan dalam kajian ini. Hasil kajian ini menunjukkan bahawa pengatur voltan yang direka adalah stabil dengan jenis dan bilangan kapasitor seramik berlapisan yang dicadangkan. Lebih penting lagi, keputusan transien juga adalah sehampir dengan keputusan simulasi di mana output pengantara voltan tidak mengalami kelanjakan dan kejatuhan voltan semasa dimuatkan dengan arus dinamik yang bermaknitud 10.5A dalam 1μs. Kesimpulannya, sebuah pengatur voltan dengan tindak balas laju yang mempunyai hanya kapasitor output seramik telah direka dan dianalisis and ia mempunyai tindak balas transien yang lebih baik berbanding dengan reka bentuk asal.

ABSTRACT

The need to have fast transient response of the voltage regulator is driven by the increasing current slew rate of the mobile microprocessor. Hence, optimizing the switching frequency of the voltage regulator becomes an important step to achieve a balance between preserving the efficiency of the voltage regulator and improving the transient response. Besides, output capacitor solution with multilayer ceramic capacitor has also become more popular due to its small size and cheap cost.

Over the years, even though the topology of the buck converter remains unchanged, there are plenty of innovations and breakthroughs in the power stage of the voltage regulator and controller technology. In addition, output impedance oriented design and adaptive voltage positioning (AVP) feature are also introduced to address the transient requirements. Apart from improving the dynamic response of the voltage regulator, many research works also focus on improving the efficiency of the voltage regulator, especially for battery-powered systems.

A fast transient voltage regulator with all ceramic output capacitors for mobile microprocessor is proposed in this study. The outcome of the study shows that the voltage regulator designed is stable with the proposed type and number of multilayer ceramic capacitors. More importantly, the actual transient results correlate well with the simulation results where minimal transient droop and overshoot are observed with a dynamic current load step with a slew rate of 10.5A per 1 μs. In conclusion, a fast transient voltage regulator with all ceramic output capacitors is designed and analyzed which proven to have better transient performance compared to the original design on the test board.

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LIST OF SYMBOLS

AC	Alternating current
A_{CS}	Gain of current sense amplifier
AVP	Adaptive voltage positioning
B_{max}	Maximum flux density
C_{boot}	Bootstrap capacitor
CCM	Continuous conduction mode
C_{droop}	Droop setting capacitor
C_{DS}	Drain-to-Source capacitance
C_{GD}	Gate-to-Drain capacitance
C_{GS}	Gate-to-Source capacitance
C_{in}	Input capacitance
C_{ISS}	Input parasitic capacitance of MOSFET
CMC	Current mode control
C_{OSS}	Output parasitic capacitance of MOSFET
C_{out}	Output capacitance
CPU	Central processing unit
C_{RSS}	Transfer parasitic capacitance
CSN	Negative current sense feedback terminal
CSP	Positive current sense feedback terminal
C_{VDD}	Input capacitance for supply voltage V_{DD}
dB	Decibel
DC	Direct current

DCM	Discontinuous conduction mode
DCR	Parasitic resistance of the inductor
DRVH	High-side MOSFET driver signal
DRVL	Low-side MOSFET driver signal
ESL	Equivalent series inductance of the capacitor
ESR	Equivalent series resistance of the capacitor
ET	Volt-second balance of the inductor
F_{CO}	Bandwidth of the voltage regulator
FET	Field effect transistor
FOM	Figure of merit
F_{SW}	Switching frequency
F_Z	Frequency of zero
GFB	Ground feedback terminal
G_L	Loop gain
G_M	Gain of error amplifier
GPU	Graphic Processing Unit
I_{DIODE}	Diode current
HS	Hide-side
I_{DRVH}	Driver signal current
I_{max}	Maximum load current
IMVP7	Intel mobile voltage positioning – 7
I_{out}	Output current
$I_{q5V\_controller}$	5V quiescent current of the controller
$I_{q3.3V\_controller}$	3.3V quiescent current of the controller
I_{q5V_driver}	5V quiescent current of the driver

$I_{q3.3V\_driver}$	3.3V quiescent current of the driver
I_{rr}	Reverse recovery current
I_{sat}	Saturation current of inductor
I_{step}	Dynamic current step of the load current
L_o	Ouput inductance
L_{out}	Output inductor
LS	Low-side
L_{VR}	Series inductor for voltage regulator model
MLCC	Multi-layer ceramic capacitor
MOSFET	Metal oxide field effect transistor
N-Ph	Number of phase
NVDC	Narrow direct current voltage
PCB	Printed circuit board
P_{core_PWM}	Core loss of inductor in PWM mode
PDN	Power delivery network
PFM	Pulse frequency modulation
PWM	Pulse width modulation
Q_G	Gate charge of MOSFET
Q_{GD}	Gate-to-Drain charge of MOSFET
Q_{GS}	Gate-to-Source charge of MOSFET
Q_{TH}	Gate charge of MOSFET at threshold point
Q_{OSS}	Output charge of MOSFET
Q_{rr}	Reverse recovery charger of MOSFET
Q_{SW}	Gate charge at switch point voltage
R_{cs}	Equivalent current sense resistance

R_{damp}	Damping resistor for MOSFET driver signal
R_{driver_sink}	Internal sinking resistance of driver
R_{driver_source}	Internal sourcing resistance of driver
R_{droop}	Droop setting resistor
$R_{ds(on)}$	Drain-to-source resistance of MOSFET
R_g	Internal gate resistance of MOSFET
R_{LL}	Load line
R_{load}	Output loading resistance
SMD	Surface mount device
SMT	Surface mount technology
SVID	Serial voltage identification
SW	Switch node
T_{DEAD}	Dead time
$T_{DLY(fall)}$	Delay time for falling edge
$T_{DLY(rise)}$	Delay time for rising edge
T_{off}	OFF time
T_{on}	ON time
T_{period}	Period
T_{rr}	Reverse recovery time
T_{slew}	Slew time
V_c	Control voltage
V_{DIODE_LS}	Forward voltage drop of body diode of low-side MOSFET
V_{DRIVE}	Driver voltage
V_{DS}	Drain-to-source voltage
VFB	Voltage feedback terminal

V_{GS}	Gate-to-Source voltage
$V_{GS(th)}$	Gate-to-Source threshold voltage
V_{in}	Input voltage
VMC	Voltage mode control
Vo	Output voltage
Vout	Output voltage
VR	Voltage regulator
V_{SP}	Switch point voltage
Z_c	Impedance of output capacitor
Z_{droop}	Impedance of droop setting RC components
Z_{out}	Output impedance
Z_{target}	Target impedance
Z_{vr}	Ouput impedance of voltage regulator

CHAPTER 1

INTRODUCTION

1.0 Chapter Overview

Chapter 1 is the introductory chapter of this study. First of all, Section 1.1 provides the background of the study and also listed down the five important criteria for a good voltage regulator in mobile segment. Section 1.2 explains the trend of switching frequency in the industry and the challenges to optimize the switching frequency to achieve a balance between good transient performance and good efficiency. Section 1.3 justifies the need to design a fast transient voltage regulator with optimized number of output capacitor in order to keep the solution size small and cheap. The problem statement and research objective are presented in Section 1.4 and Section 1.5 respectively. Last but not least, Section 1.6 provides the thesis outline.

1.1 Background

Non-isolated DC-DC voltage regulator is the key component of power delivery network in a modern computer system. It is used to step down the high DC input voltage to a well regulated lower output voltage which is consumed by platform devices. Out of all the platform devices, the design of the voltage regulator for the processor is most demanding and challenging because the quality of the power delivery network to the processor determines the overall performance of the system.

There are many key parameters which dictates the quality of a voltage regulator design. In fact, the importance of each parameters can be varied across different industry and segments. Figure 1.1 depicts the key parameters for a good voltage regulator design for mobile system such as laptop.

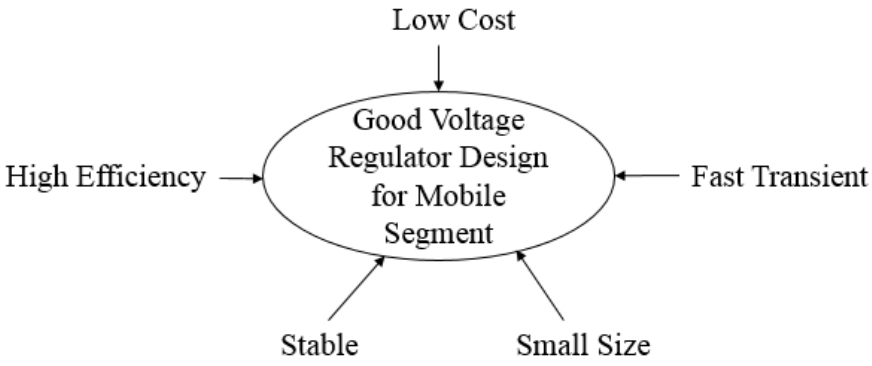

Figure 1.1: Key design requirements for power delivery circuits on mobile computer

First of all, the voltage regulator must be stable under all possible operating conditions, and this is the most important and fundamental requirement. Secondly, fast transient response of the voltage regulator has become more and more important as the mobile processor load current switches at a much higher slew rate nowadays. A fast reacting and stable voltage regulator is able to keep the output voltage under the specified regulation window even when high current transient event happens. A fast transient voltage regulator can also bring significant cost and area benefit to the voltage regulator solution. The reason is when the voltage regulator can react fast enough to high frequency transient, significant amount of output capacitors can be saved. This directly translates to less design cost and board area occupied.

Efficiency is another key metric to gauge the quality of the voltage regulator in a mobile computer system. A voltage regulator with good efficiency has low power

loss which is translated to prolonged battery life for a battery-powered system. In addition, an efficient voltage regulator requires only simple thermal solution. In a greater extent, the whole system can be designed in a chassis with no fan at all. In fact, fan-less design is very much a requirement in thin and light-weight laptop design such as Intel's Ultrabooks.

1.2 Switching Frequency of Voltage Regulator

Typical design specifications for a switching regulator includes input voltage range, output voltage, maximum output current, and worst case magnitude of the dynamic output current. Switching frequency is the key design parameter that has direct impact to the transient performance and efficiency of the voltage regulator. Figure 1.3 below shows the typical switching frequency for different power converters in the market. For the case of voltage regulator residing in a mobile computer system, the switching frequency ranges from 200 kHz to 1 MHz. In fact, the trend for switching frequency of voltage regulator has been increasing steadily over the years.

Figure 1.2: Switching frequency of different voltage regulators [1]

High switching frequency is good for transient performance and reducing size of the passive components such as inductor and capacitors of the voltage regulator. However, too high of a switching frequency will degrade the efficiency of the voltage regulator and increase the risk of control loop instability. Hence, voltage regulator designer faces a great challenge to find the suitable switching frequency in order to meet both the efficiency and transient performance targets.

1.3 The Need for Fast Transient Voltage Regulator

Moore's law propelled the semiconductor industry to double the number of transistors integrated into the processor every 18 to 24 months as shown in Figure 1.4 below. In addition, advancement of semiconductor manufacturing process also helps to reduce the supply voltage to the processor to sub-1V in the most recent processors.

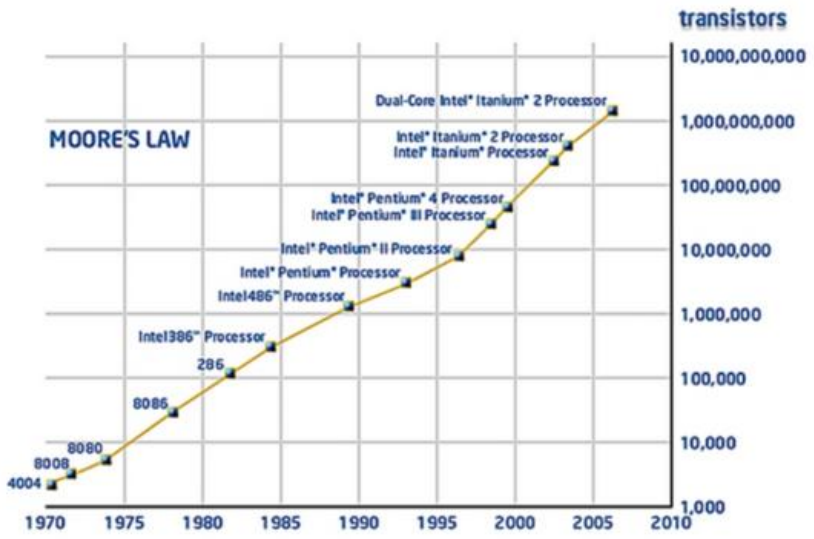

Figure 1.3: Increasing number of transistors integrated into the processor according to Moore's law [2]

However, current demand for processors is increasing year-over-year due to aggressive integration strategy and increasing complexity of circuit blocks inside the processor. Besides, computational frequency of the processor will always be pushed higher from one generation of processor to the next. Together with incremental power saving states being introduced to the processor C-states, the current profile of the processor becomes more dynamic in nature. Figure 1.5 below shows that the trend of the current slew rate of processor is increasing year-over-year when new generation of processors are released.

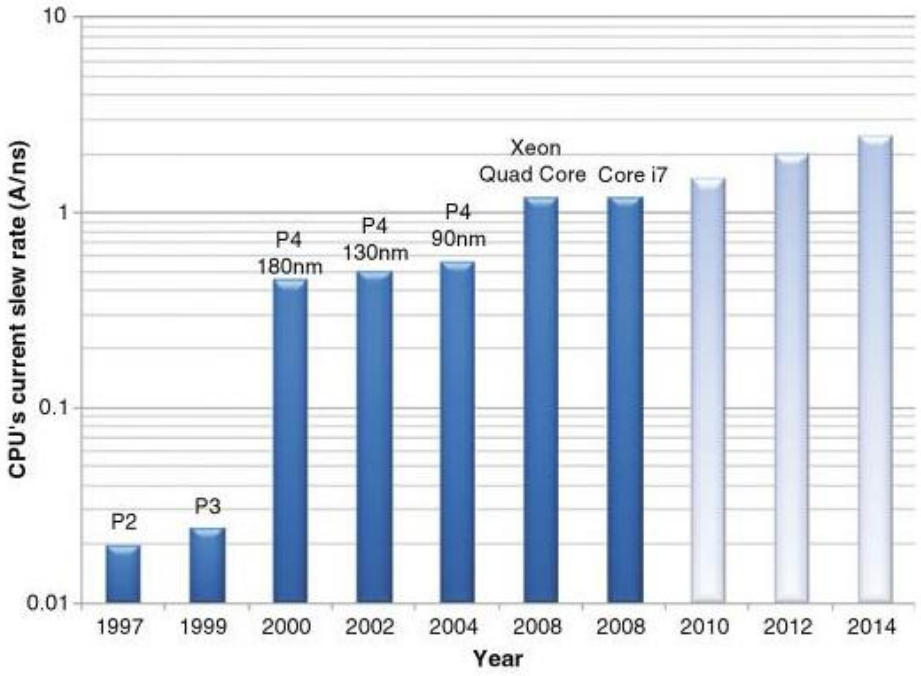

Figure 1.4: Trend of processor's current slew rate measured at the package pin [3]

The industry is trying to catch up with the high current slew rate of the processor current load by developing voltage regulator with high switching frequency. However, as mentioned in section 1.2, the switching frequency range for voltage regulator is limited in order to preserve the efficiency and stability. The other design solution to address the high current slew rate is to design with huge number of output

capacitors. Unfortunately, design with too many output capacitors will increase the product cost and consume huge amount of board area. This is not a favorable solution for mobile segment. As a result, this situation poses a great challenge to the voltage regulator designer.

1.4 Problem Statement

Fast transient voltage regulator is very much needed to address droop and overshoot caused by the high current slew rate of the processor. Increasing the switching frequency of the voltage regulator is a way to improve the transient response. However, on-board voltage regulator has limited switching frequency range. Besides, too high of a switching frequency will result in poor efficiency. Hence, this situation challenges the voltage regulator design to optimize both the switching frequency and efficiency at the same time.

Secondly, size of the voltage regulator has always been too huge driven by increasing power demand of the mobile processor. This renders the overall mobile computing product to be heavy, bulky, costly, and unattractive. With AVP feature introduced, now the voltage regulator designer has the option to design with all ceramic output capacitors in order to present an area and cost effective solution. However, design with all ceramic output capacitors requires thorough analysis and engineering judgment so that the solution presented is stable and meets the design specifications.

1.5 Research Objective

This study aims to design a fast transient voltage regulator with minimal droop and overshoot using only ceramic capacitors in order to reduce the output decoupling area and cost. At the same time, the efficiency of the voltage regulator is preserved by optimizing the switching frequency. In order to achieve this objective, a power loss calculator is developed to select the switching frequency for the voltage regulator. LTSpice and MATHCAD will be used to optimize the type and number of multilayer ceramic capacitors for the voltage regulator. The proposed design will be implemented on a test board where the actual measurement are taken to correlate with the simulated results.

1.6 Thesis Outline

Chapter 1 introduces the background of this study in the very beginning. Then, it highlights the challenge faced by the industry today in optimizing the switching frequency of the voltage regulator. Besides, the motivation to design a fast transient voltage regulator is also presented. Lastly, problem statement and research objective of this study is outlined.

Chapter 2 provides the literature review on the most recent research work related to this study. Firstly, the fundamentals of switching voltage regulator and its basic equations governing its operation is presented. Next, this chapter presents the pros and cons of different types of capacitors. The role of voltage regulator in a typical mobile computer system is briefly discussed and the concept of power delivery network is introduced thereafter. Then, the proposed single-phase on-board switching regulator is compared against different topologies such as linear voltage regulator, on-

chip voltage regulator, and multi-phase voltage regulator. Next, recent innovations and breakthroughs in the buck converter design are presented followed by reviews on output impedance based design methodology to improve the transient response of the voltage regulator. Besides, adaptive voltage positioning (AVP) concept and studies on voltage regulator efficiency are covered in the last part of this chapter.

Chapter 3 presents the methodology to design and analyze the proposed voltage regulator. Firstly, the block diagram of the proposed voltage regulator is presented with each blocks inside the voltage regulator is discussed. Next, the design flow chart is presented. A power loss calculator is developed to plot the efficiency of the voltage regulator for different switching frequency. Besides, current sensing network topology as well as detailed analysis and selection steps to arrive at the type and number of multilayer ceramic capacitors are also presented. The stability of the voltage regulator is analyzed using MATHCAD software while the exact number of MLCC used is confirmed by running SPICE simulation using LTSpice. Lastly, simulation results will be correlated to the measurement results on the test board.

Chapter 4 presents the results outlined in the methodology presented in Chapter 3. Firstly, the switching frequency selection outcome is discussed. Next, the temperature characteristic of the current sensing network is presented. Simulation outcomes using LTSpice is presented and the proposed type and number of MLCC used as the output capacitors is discussed. Lastly, the measured transient results obtained from the test board are presented to show the improvement as compared to the original design.

Chapter 5 draws the conclusion of this study and presents the future works that can be extended to further improve the scope and depth of this study.

CHAPTER 2

LITERATURE REVIEW

2.0 Chapter Overview

Chapter 2 is the presentation of the review of the most recent and relevant literature in the field of voltage regulator design in mobile segment. Section 2.1 explains the theory of operation of a switching voltage regulator. Section 2.2 introduces the common capacitors used as the output capacitor for voltage regular and the pros and cons for each and every one of them. Section 2.3 shows where does the voltage regulator fit in a typical mobile computer system while Section 2.4 introduces the concept of power delivery network (PDN) and the role of voltage regulator in the PDN. Section 2.5 draws the comparisons between switching voltage regulator and linear voltage regulator. Section 2.6 compares the pros and cons of both on-board and on-chip voltage regulators and brings the focus of this study to on-board voltage regulator. Section 2.7 explains why it makes more sense to design with single-phase voltage regulator in low power mobile computer system. Section 2.8 provides the overview on the topology of a conventional buck converter and recent breakthroughs in each of its fundamental building blocks including the power stage, controller, and feedback compensation. The relationship between output impedance of voltage regulator and its transient response is explained in Section 2.9. Section 2.10 introduces the concept to adaptive voltage positioning (AVP) in improving the transient response of the voltage regulator. Lastly, research works and studies on efficiency of voltage regulator are presented in Section 2.11.

2.1 Fundamentals of Switching Voltage Regulator

Switching voltage regulator is the most common topology used as the DC-DC converter powering the processor and all other system loads inside of mobile computer. Figure 1.2 below shows the typical design of a synchronous switching voltage regulator. V_{in} is the input voltage while V_{out} is the output voltage. C_{in} stands for input capacitor while C_{out} stands for output capacitors. L_{out} is the output inductor which forms the LC filter at the output of the switching voltage regulator. The main switch of the voltage regulator is the control MOSFET, Q_1. Synchronous voltage regulator has its freewheeling diode replaced with a synchronous MOSFET, denoted as Q_2. Lastly, the switching activity of the voltage regulator is controlled by a controller.

Switching voltage regulator uses pulse-width modulation (PWM) scheme to control the duty cycle of its switching activity to achieve the desired output voltage regulation. During the time when the control MOSFET, Q_1 is turned on and the synchronous MOSFET, Q_2 is turned off, the voltage across the inductor is given by the formula in equation 1.1 and 1.2 respectively.

$$During\ T_{on}: V_{in} - V_{out} = L_{out} \cdot \frac{\Delta I_{Lout}}{T_{on}} \tag{2.1}$$

$$During\ T_{off}: V_{out} = L_{out} \cdot \frac{\Delta I_{Lout}}{T_{off}} \tag{2.2}$$

The energy stored in the output inductor during ON time, T_{on} and energy released during OFF time, T_{off} must be equal in magnitude to achieve equilibrium in energy transfer for a lossless system. The energy of an inductor is given by the formula shown in equation 1.3.

$$E_{inductor} = \frac{1}{2} \cdot L_{out} . \Delta I_{Lout}^2 \tag{2.3}$$

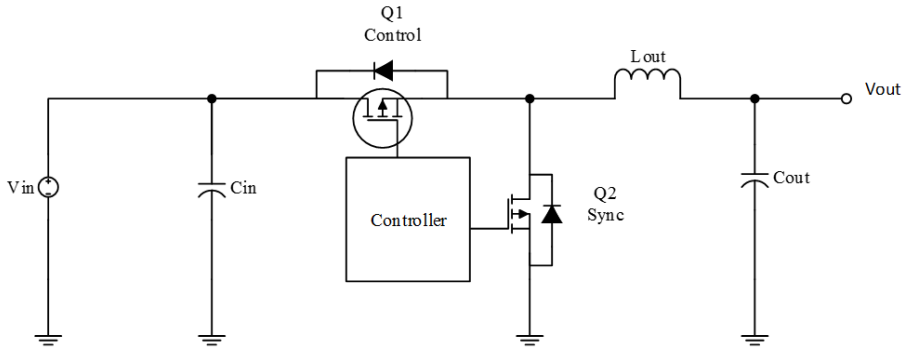

Figure 1.5: Switching voltage regulator

Based on equation 1.3, it means the inductor current ripple during T_{on} and T_{off} must be equal. Hence, combining equation 1.1 and 1.2, the relationship between the input voltage and the output voltage can be derived. Essentially, the output voltage can be regulated by controlling the duty ratio of T_{on} to the switching period, T_{period} as shown in equation 1.4. The switching period is a fixed duration of time given the fact that the switching frequency of the voltage regulator is a constant.

$$\frac{V_{out}}{L_{out}} \cdot T_{off} = \frac{V_{in} - V_{out}}{L_{out}} \cdot T_{on}$$

$$V_{out}(T_{on} + T_{off}) = V_{in}(T_{on}), T_{on} + T_{off} = T_{period} = {}^{1}/_{F_{sw}}$$

$${}^{V_{out}}/_{V_{in}} = {}^{T_{on}}/_{T_{period}} \tag{2.4}$$

2.2 Output Capacitor for Voltage Regulator

Output capacitor plays an important role to contain the droop and overshoot at the output of the voltage regulator. Besides, output capacitor is also used to stabilize

the control loop of the voltage regulator and to reduce output voltage ripple. Usually, the amount of output capacitor needed is capped by the transient requirement of the design. Table 2.1 below tabulates the list of common surface-mount (SMD) capacitors and the characteristics of each and every one of them.

Table 2.1: Common surface-mount (SMD) capacitors

Type / **Char.**	**Multilayer Ceramic**	**Aluminum Electrolytic**	**Solid Tantalum**	**Polymer / Organic**	**Hybrid**
Capacitance	Low	High	Medium	High	High
ESR	Low	High	High	Low	Medium
Size	Small	Very Huge	Huge	Huge	Very Huge
DC Bias Effect	Yes	No	No	Slight	No
Ripple Current	Medium	Low	Low	High	Medium
Temperature Characteristic	Bad	Bad	Medium	Good	Good
Acoustic Noise	Yes	No	No	No	No
Life Span	Long	Short	Medium	Medium	Medium
Leakage Current	Low	Low	Low	High	Low
Safety	Good	Good	Bad	Medium	Good

As the mobile computer market is trending towards cheaper, lighter, and thinner computing products, multilayer ceramic capacitors (MLCC) emerges as the popular choice of output capacitors for voltage regulator. The reason is because MLCC is very cheap and small in size. Apart from this, MLCC has the lowest equivalent series resistance (ESR) and equivalent series inductance (ESL) among the SMD capacitors available in the market. In other words, MLCC has the least undesired parasitic components. Besides, MLCC has a reputation for good reliability and least safety hazard. Leakage current in MLCC is also one of the lowest among the capacitors.

However, designing with MLCC has its fair share of challenges as well. First of all, it has relatively lower capacitance. A lot of MLCCs are needed to replace the original bulk capacitors with higher capacitance. A twist to this scenario is when adaptive voltage positioning (AVP) is introduced to voltage regulator design about a decade ago. AVP is a feature where output voltage drops when output current increases. This invariably helps to reduce the power consumption of the processor during high current loading. More importantly, AVP provides a larger window for overshoot, and this means less output capacitors are needed. As a result, all ceramic output capacitors design becomes an attractive solution due to the cost and area benefits offered.

Another undesired characteristics of MLCC is DC biasing effect where its effective capacitance drops more with higher DC voltage applied across its terminals. Fortunately, output voltage level reduces year-over-year due to Moore's law. For the current state-of-art processor, the voltage supply ranges from 0.5V to 1.5V only. Thus, MLCC is still suitable as the output capacitors for voltage regulator because the DC bias effect is minimal with the aforementioned output voltage range. Other secondary unwanted effects for all ceramic output capacitors design include acoustic noise effect and poor temperature characteristic. Acoustic noise is caused by piezo-electric effect inherent to ceramic materials during voltage transients. Noticeable high pitch ringing can be heard from the computer if the piezo-electric effect is very serious. Nowadays, variants of MLCC design have been developed to address this issue and acoustic noise is no longer a design concern. As for the aspect of temperature characteristics of MLCC, many different ceramic materials have been proposed which effectively allay the concerns of voltage regulator designers. In summary, voltage regulator with all ceramic output capacitors is preferred in mobile computer design.

2.3 Power Delivery Architecture in Mobile Computer System

Voltage regulator (VR) plays an important part in the power delivery architecture of a mobile computer system such as laptops, Ultrabooks, and mobile internet devices. A typical power delivery architecture of a battery-powered, narrow-V_{DC} (NVDC) mobile computer system advocated by Intel® is shown in Figure 2.1 below [4]. The NVDC buck charger converts the adaptor voltage of 19V to the system input voltage, V_{DC}. Besides, the Lithium-Ion battery also supplies to the V_{DC}. V_{DC} has a rated voltage of 8.7V to 12.6V due to the 3S2P configuration of the battery pack (3S2P means a configuration of two parallel groups of three series connected Lithium-Ion cells). Further down the power delivery path, numerous on-board voltage regulators are used to step-down the V_{DC} to a lower output voltage needed by different platform consumers such as the central processing unit (CPU), memory, chipsets, and other devices.

Out of all the voltage rails, CPU Vcccore rail of the mobile microprocessor has the most demanding electrical requirements. The quality of the power delivery of this rail dictates the peak performance of the mobile microprocessor. As a result, for the last ten decades, multiple efforts and innovations were introduced to improve the voltage regulator design of the Vcccore rail in terms of lower tolerance, faster transient response, better efficiency, and improved stability [5].

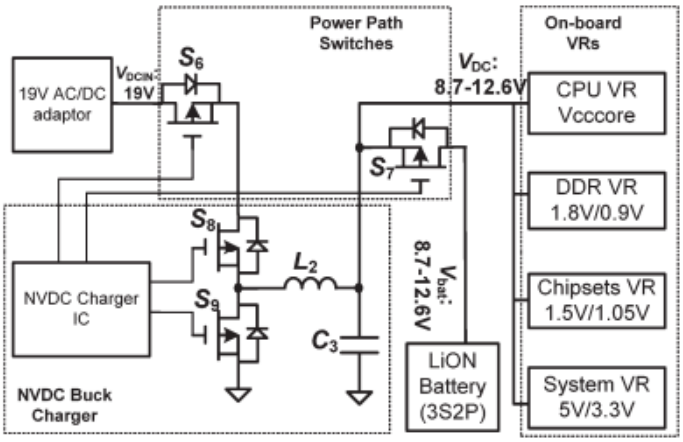

Figure 2.1: Typical power delivery architecture in mobile computer system [4]

2.4 Voltage Regulator in the Power Delivery Network

A typical power delivery (PDN) model is shown in Figure 2.2 below. VR is represented as VRM in the figure and it is the abbreviation for voltage regulator module. VR is the starting point for any power delivery network, and it has the higher capacity of charging but covers up to several kilo Hertz only because it is limited by its operational bandwidth. The full PDN seen by the microprocessor is a cascaded connection of capacitors as well as parasitic resistances and inductances in the power planes. The capacitors near the VR are larger in size and capacitance such as the bulk caps and surface-mount technology (SMT) caps. These large capacitors are used to stabilize the VR, minimize the output ripple, and react to low frequency transient events. Package capacitors on the other hand which are placed close the microprocessor have smaller size and capacitance. They are used as the first line capacitors reacting to the very high frequency transient happening at the microprocessor. Apart from transient requirement, the amount of capacitance needed

also depends on the power planes of the printed-circuit board (PCB) and the package because they are the key contributors of parasitic elements of the PDN.

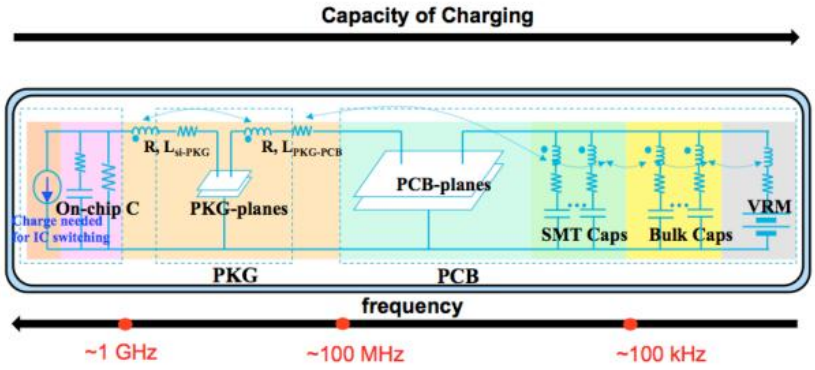

Figure 2.2: Power delivery network model [6]

2.5 Switching VR vs Linear VR

There are two main topologies of step-down voltage regulator widely used in mobile computer system as the power supply to the microprocessor, namely linear regulator and switching regulator. Linear regulator is smaller, less noisy, and simpler compared to its switching counterpart. This makes linear regulator a good topology for silicon integration for loading current in milliamps range. On the flip side, linear regulator has bad efficiency at heavy load and limited to only step down regulation [7].

In comparison, switching regulator is very efficient compared to linear regulator due to its design of using reactive components to achieve voltage regulation instead of resistive components. In spite of the complexity, noisy, and larger design of the switching regulator, it is still preferred topology to power up the microprocessor because it can handle high current with much better efficiency. This is especially true in battery-powered system where good efficiency is critical to prolonged battery life.

2.6 On-board VR vs On-Chip VR

Due to advancement in silicon manufacturing process, on-chip VR is designed so that power supply can be placed very close to the microprocessor. This means parasitic components between the on-chip VR to the microprocessor are less, and on-chip VR can respond faster to load changes. Besides, on-chip voltage VR offers the benefits of smaller passive components such as decoupling capacitors and inductors because it can switch at a higher frequency compared to on-board voltage regulators. Another important reason why on-chip regulator is studied and developed is because the increasing frequency gap between the microprocessor and the on-board voltage regulators. For instance, computer microprocessor can easily run at Giga Hertz range of frequency while an on-board voltage regulator still switches at Kilo Hertz range of frequency. In order to bridge this gap, a lot of decoupling capacitors are needed which is translated to additional design cost [8].

However, there are several issues and challenges associated with on-chip voltage regulators. Firstly, even though on-chip voltage regulator switches at higher frequency, but the trade-off is the degradation in regulation efficiency. In battery-powered system, efficiency of voltage regulators is very important and due to this reason alone, on-board voltage regulators are still preferred over on-chip voltage regulators. Next, due to limited area on the chip, size of passive components for on-chip voltage regulators is relatively smaller. This means that on-chip voltage regulators are unable to contain the voltage droop or overshoot due to high transient activity of the mobile processor, especially for central processing unit (CPU) core and graphic processing unit (GPU). Lastly, it is a technical challenge to integrate power inductor onto the silicon. In addition, inductive circuits require large real estate of chip to be fabricated, which adds cost and area overhead to the silicon design [9] .

In conclusion, for mobile microprocessor, on-board voltage regulator is still a better choice compared to on-chip voltage regulator because of its higher current capability, better efficiency, and availability of supporting passive components on the board.

2.7 Single-Phase VR vs Multi-Phase VR

Number of phase in a VR is referring the number of power stages connected in parallel to a common output. In fact, VR used to have only single-phase design as the power demand of microprocessor back then was low. When power demand of microprocessor has been increasing steadily over the years, multi-phase VR was introduced as an innovative way to support high power load without over-sizing the power stage [10]. Besides, multi-phase interleaved VR also appears to have lower output ripple and better dynamic response as passive components are now smaller [11].

However, for mobile microprocessor where maximum current is low, using a multi-phase design is more of a bane than boon to the whole system because of additional cost and component count needed to support the extra phases. In addition, multi-phase design complicates the internal control circuitry of the controller in order to implement non-overlapping control for each of the phases. The overall efficiency of the VR will take a hit also because of additional passive component count. As a result, multi-phase design is only popular for high current and high performance systems such as desktop and workstation [12], [13]. For mobile system, especially for battery-powered and low cost design, single-phase VR converter is still preferred.

2.8 Topology of Buck Converter

Step-down switching voltage regulator powering mobile microprocessor is essentially a buck converter. Basically, buck converter can be categorized into three different parts, i.e. the power stage, feedback compensation circuit, and the controller as shown in Figure 2.3.

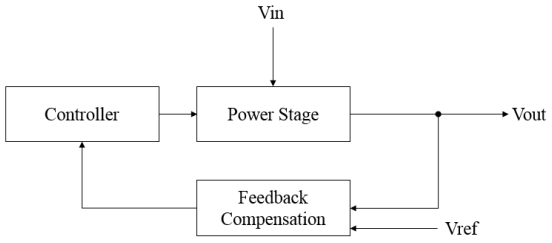

Figure 2.3: Fundamental building blocks of a buck converter

2.8.1 Power Stage of Buck Converter

The power stage of the buck converter consists of the input capacitor, high-side (HS) FET, low-side (LS) FET, driver, output inductor, and output capacitor (Figure 2.4) [14].

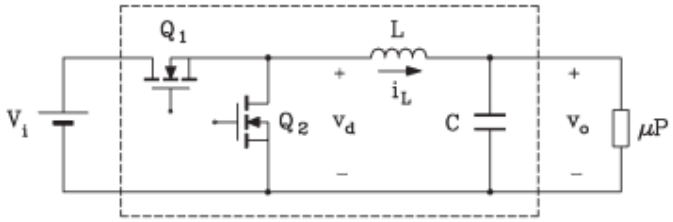

Figure 2.4: Power stage of buck converter [14]

Technological advancement in power electronics such as novel packaging technology as showcased in [15] improves the electrical performances of the power stage. Besides, various component level breakthroughs over the years help to bridge

the gap between the capability of the buck converter and the ever increasing power demand of the microprocessor. For example, [16] proposes a novel tapped inductor for buck converter to achieve a fast transient response.

Apart from improving the power capability, there are also engineering efforts spent to reduce the power components count and size for the power stage. Size and component count are getting more important when the overall mobile computer size is shrinking, especially in slim and highly portable mobile devices. As a result, integration of power stage components into silicon has become a trend in the industry as demonstrated in [17]. This is as opposed to the conventional buck converter power stage where every single power component is designed with discrete and standalone package on the motherboard.

2.8.2 Control Schemes and Techniques

Switching regulator used to employ only pulse-width modulation (PWM) control scheme to achieve voltage regulation at its output [18]. For PWM scheme, there are two main classical VR control topology, i.e. voltage mode control (VMC) or current mode control (CMC) [19]. CMC is known to have faster transient response due to its inner current loop. Besides, compensation circuit required by CMC is less complicated as compared to VMC [20]. Hysteretic control has been gaining popularity in recent years because it is faster than VMC and CMC, and in the same time requires no compensation to work [14]. In recent years, a number of variants of hysteretic controller based on different modulator design such adaptive constant-on time with constant ripple are proposed in [21], [22]

However, PWM control is not efficient during low current load. On the other hand, pulse-frequency modulation (PFM) control scheme is proven to be able to reduce power loss of the buck converter during low current load [23]. As a result, buck converter for mobile system nowadays is designed to operate in both PWM and PFM control schemes in order to achieve a good efficiency across the current load range. It is often called dual-mode buck converter. Basically, it means the controller employs PWM control during continuous conduction mode (CCM) while switches to PFM control when entering discontinuous conduction mode (DCM). Switching between PWM and PFM control scheme is achieved automatically using a zero current detection circuit resides inside the controller [24], [25].

2.8.3 Feedback Compensation

Feedback compensation circuit is used to create a negative feedback system in the buck converter to keep the output voltage within the regulation window. Besides, compensation circuit is important to maintain the stability of the VR. The compensation circuit is an intermediate circuitry between the power stage and the controller. Hence, the design of the compensation circuit depends very much on the power stage and the controller topology. There are three main types of compensation network [26]. Type I compensator is a lag compensator. It basically slow down the feedback response of the VR. Secondly, Type II compensator is a lead compensator as it provides a 90^{o} phase boost with additional zero in the feedback network. Lastly, Type III is the most sophisticated feedback compensator which able to provide a phase boost up to 180^{o}. All in all, feedback compensation network is connected in series to the loop gain path of the VR to ensure a stable negative feedback system. A stable VR

system is known to poses a phase margin of 45^{o} to 60^{o}, and a gain margin of around 10dB [27], [28].

2.9 Output Impedance and VR Transient Response

Output impedance is an important figure of merit which is linked to the transient response of a voltage regulator (VR) to its output current loading [29]. By inspecting the amplitude of the output impedance curve of the voltage regulator in frequency domain, undershoot and overshoot of the voltage regulator can be predicted in time domain. Output impedance oriented design methodology is getting more popular because the response of the voltage regulator can be easily analyzed across the full frequency spectrum of the current load. This is further evidenced by the fact that given the high repetitive and high slew rate nature of nowadays microprocessor current load, output impedance based frequency domain analysis undoubtedly eases the design challenge to meet the stringent transient specifications. In addition, output capacitors can be designed optimally as resonance peaks information is readily available in the output impedance curve. This leads to a cost effective power delivery solution.

The output impedance seen at the output of the voltage regulator are shaped by the output capacitors used and the bandwidth of the voltage regulator. The bandwidth of the voltage regulator is dependent on the compensation network and bandwidth of the error amplifier. Normally, VR bandwidth is less than one-fifth of its switching frequency [30]. Increasing the VR bandwidth and adding more output capacitor is a way to reduce the output impedance at the expense of additional design cost and lower efficiency. However, VR together with its output capacitor can only address output

impedance up to around Mega Hertz range. The full power delivery network (PDN) from voltage regulator to the silicon load contains numerous capacitors of different types and capacitance connected in parallel in order to maintain a low PDN impedance from VR all the way to the silicon.

Due to advancement of silicon process technology and increasing computational demand, the supply voltage of the silicon reduces with each introduction of smaller transistor node while the maximum current and dynamic current are increasing year-over-year [31]. Target impedance (Z_{target}) is an important design parameter introduced decades ago but still very useful even till today to evaluate the impedance of the PDN. The target impedance is calculated using the formula given in equation 2.5 below [32]:

$$Z_{target} = \frac{(Power\ Supply\ Voltage)\ \times (Allowed\ Ripple\ \%)}{Current}. \qquad (2.5)$$

Power supply voltage is the nominal voltage of the VR while allowed ripple is the tolerance of the VR output quoted in percentage. The denominator in (2.5) is the maximum load current or dynamic load step. When the current demand is increasing with power supply voltage drops from one generation of silicon products to the next, it can be implied that the target impedance will be a very challenging design target to meet year-over-year. Table 2.2 shows that for desktop workstation segment, the target impedance is dropping at a factor of five every three years [33]. It proves to be even more challenging for current state-of-art computing device because it operates mostly at sub-1V supply. On another note, frequency range needs to be supported is also increasing drastically for every product generation too. Even though the statistical data quoted in [33] is based on desktop segment, the trend of reduction in target impedance are observed in other segments as well [32].

For a voltage regulator design to address a specific target impedance of the PDN across the frequency range of interest, output impedance oriented methodology helps the designer to arrive at an optimal decoupling cost and tuning of the VR bandwidth which meet the transient specifications.

Table 2.2: Trend of target impedance in desktop workstation [33]

Year	Supply Voltage (V)	Maximum Current (A)	Power Dissipation (W)	Z_{target} (mΩ)	Frequency (MHz)
1990	5.0	1	5	250	16
1993	3.3	3	10	54	66
1996	2.5	12	30	10	200
1999	1.8	50	90	1.8	600
2002	1.2	150	180	0.4	1200

2.10 Adaptive Voltage Positioning (AVP)

Adaptive voltage positioning or AVP is a revolutionary technique introduced years ago to reduce the decoupling capacitors needed for VR transient response especially during overshoot event. The principle idea behind AVP is to generate an artificial load line using the VR controller where output voltage of the VR drops linearly as current load increases as shown in Figure 2.5 [34].

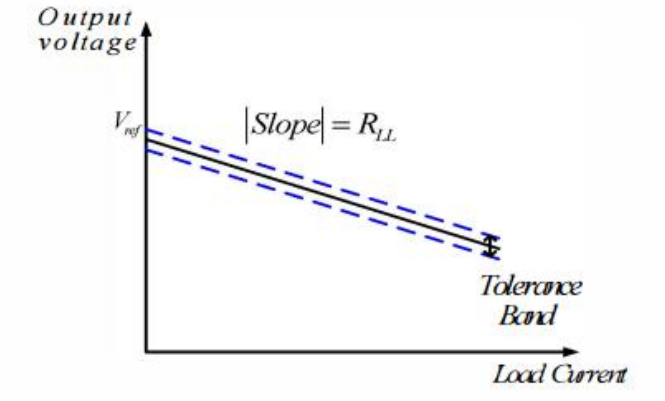

Figure 2.5: AVP load line programmable by the VR controller [34]