INVESTIGATION OF WIRE SWEEP DURING PBGA ENCAPSULATION PROCESS USING FLUID STRUCTURE INTERACTION

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INVESTIGATION OF WIRE SWEEP DURING PBGA ENCAPSULATION PROCESS USING FLUID STRUCTURE INTERACTION

by

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DECLARATION

I hereby declare that the work reported in this thesis is the result of my own investigation and that no part of the thesis has been plagiarized from external sources. Materials taken from other sources are duly acknowledged by giving explicit references.

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LIST OF SYMBOLS

A_1, A_2	Pre-exponential factors 1/s.
B	Exponential-fitted constant Pa.s.
C_1, C_2	Fitting constant.
C_P	Specific heat J/kg.K.
C_D	Drag coefficient
D	Drag force per unit length of the wire
D_N	Largent deformation normal to the wire
d	Wire diameter
E	Elastic modulus of wire
E_1, E_2	Activation energies K.
F	External body force.
f	Front advancement parameter.
f_B	Bending geometry factor for the bending moment.
f_T	Twisting geometry factor for the bending moment.
G	Shear modulus of wire
g	Gravitational acceleration.

H	Height of wire
I	Momentum of inertia of the wire
I_p	Polar moment of inertia of the wire
k	Thermal conductivity W/m.K.
k_1, k_2	Rate parameters described by an Arrhenius temperature dependency 1/s.
L	Length of the wire span
M	Linear viscous operators.
m_1, m_2	Constants for the reaction order.
N	Non-linear viscous operators.
n	Power law index.
P	Static pressure Pa.
Re	Reynolds number
S	Length of the wire
T	Absolute temperature K.
t	Time s.
T_b	Temperature-fitted constant K.
U	Undistributed upstream velocity of fluid

u	Fluid velocity component in x-direction mm/s.
$\vec{u}$	velocity of solid in *x*, *y* and *z* axis mm/s.
v	Fluid velocity component in y-direction mm/s.
w	Fluid velocity component in z-direction mm/s.
x, y, z	Cartesian coordinates.

Greek letters

α	Conversion of reaction.
α_{gel}	Degree of cure at gel.
$\dot{\alpha}$	Curing rate.
ΔH	Exothermic heat of polymerization J/kg.
η	Viscosity Pa.s.
η_0	Zero shear rate viscosity Pa.s.
ρ	Density kg/m^3.
ρ_s	Density of solid kg/m^3
τ	Shear stress Pa.
$\dot{\gamma}$	Shear rate 1/s.

τ^*	Parameter that describes the transition region between zero shear rates and the power law region of the viscosity curve Pa.
Φ	Energy source term J.

LIST OF ABBREVIATIONS

AMI	Autodesk Mould-flow Insight
CABGA	Chip Array Ball Grid Array
CAE	Computer-aided Engineering
CCD	Central Composite Design
CCD Camera	Computer Capture Digital Camera
CFD-ACE-U	Computational Fluid Dynamics - Aides Computer Engineering-Unit
CSP	Chip Scale Package
DOE	Design of Experiment
EMC	Epoxy Moulding Compound
FEA	Finite Element Algorithm
FE	Finite Element
FEM	Finite Element Method
FFT	Flow Free Thin
FSI	Fluid-Structure Interaction
FVM	Finite Volume Method
GNF	Generalized Newtonian Fluid
GUI	Graphical User Interface
IC	Integrated Circuit
I/O	Input/output
LQFP	Low Plastic Quad Flat Pack
MMAP	Matrix Molded Array Package
MpCCI	Mesh-based parallel Code Coupling Interface
MUF	Moulded Underfill

OA	Orthogonal Array
PBGA	Plastic Ball Grid Array
PDA	Personal Data Access
PGE	Power Ground Embedded
PLICE	Plastic Integrated Circuit Encapsulation
PWB	Printed Wire Bonding
RSM	Response Surface Methodology
S-CSP	Stacked-Chip Scale Package
SiP	System in Package
SOT	Small Outline Transistor
TBGA	Thin Ball Grid Array
TQFP	Tape Quad Flip Chip Package
UDF	User-Defined Function
USM	Universiti Sains Malaysia
UTM	Universal Testing Machine
VCR	Video Camera Recorder
VDCM	Vacuum Dip Compression Molding
VOF	Volume of Fluid

KAJIAN BAGI WAYAR TERSAPU SEMASA PROSES PENGKAPSULAN PBGA MENGGUNAKAN INTERAKSI STRUKTUR BENDALIR

ABSTRAK

Pengurangan berterusan saiz cip dalam industri elektronik moden mempunyai kesan yang besar ke atas reka bentuk litar dan proses pemasangan pakej IC. Pengurangan saiz cip dengan peningkatan kiraan I/O menghasilkan pembengkokan wayar yang serius semasa proses pemindahan acuan (molding). Dalam penyelidikan ini, satu teknik kajian tiga dimensi (3D) interaksi struktur cecair (FSI) dengan menggunakan mesh kod berasaskan gandingan antaramuka selari (MpCCI), untuk visualisasi pelengkungan wayar semasa pengkapsulan pakej tatasusunan grid bebola plastik (PBGA). Kesan-kesan reologi polimer, tekanan salur masuk, susunan pintu masukan, nombor cip bertingkat, diameter wayar, dan saiz lubang rongga acuan, pada kelakuan aliran bendalir, pembengkokan wayar, masa pengisian, taburan tekanan kaviti dan pengagihan tekanan, terutamanya dikaji. Satu model 3D acuan dan wayar telah dilukis menggunakan GAMBIT, dan simulasi interaksi bendalir/struktur adalah menggunakan perisian FLUENT dan ABAQUS bersepadu dengan MpCCI untuk pengiraan masa sebenar. Model Castro-Macosko dan model Kamal digunakan untuk menggabungkan polimer reologi dan kaedah keutuhan penjejakan isi padu bendalir (VOF) bagi menyelesaikan medan aliran dua fasa untuk profil pergerakkan. Fungsi Takrifan Pengguna (UDFs) manakala persamaan Kamal digunakan untuk menyelesaikan pemulihan kinetik. Saiz pakej berskala besar telah direka untuk mencontohi pengkapsulan pembungkusan PBGA untuk mengkaji kesan fenomena FSI dalam pakej PBGA. Kesan cip bertingkat, perkiraan pintu masukan dan tekanan masuk rongga acuan pada kelakuan aliran leburan dan pembengkokan wayar dikaji.

Bendalir yang berkelikatan malar telah digunakan untuk eksperimen. Keputusan berangka bagi corak aliran hadapan dan pembengkokan wayar dibanding dengan keputusan uji kaji dan didapati selaras dengan keputusan uji kaji. Tiga jenis komposisi acuan epoksi (EMC) telah digunakan untuk kajian aliran bendalir dalam rongga acuan. Profil aliran hadapan dan kelikatan melawan kadar ricihan bagi semua kes dianalisis dan dibentangkan. Keputusan berangka bagi tingkah laku aliran hadapan dan pembengkokan wayar berbanding dengan eksperimen keputusan sebelumnya dan didapati dalam perbandingan yang baik. Dalam kajian ini, penggunaan epoksi yang berkelikatan lebih rendah membolehkan udara terperangkap, taburan tekanan dan pelengkungan wayar yang lebih rendah. Reka bentuk PBGA yang optimum boleh memberi proses yang lebih baik dalam pengkapsulan PBGA dan mengurangkan pembengkokan wayar. Parameter fizikal dan proses (iaitu, tekanan salur masuk, diameter wayar, ketinggian bolong) telah dioptimumkan melalui kaedah respons permukaan menggunakan reka bentuk komposit pusat (CCD) untuk mengurangkan pelengkungan wayar, masa pengisian dan gelombong dalam pakej semasa proses pengkapsulan PBGA. Interaksi struktur bendalir (FSI) dipertimbangkan dalam pengoptimuman proses pengkapsulan PBGA. Model empirik optimum telah diuji dan disahkan dengan keputusan simulasi. Reka bentuk optimum PBGA dengan 12 wayar untuk kedua-dua parameter fizikal dan proses dicirikan dengan 5.57 MPa tekanan masukan, 0.05 mm diameter wayar, dan 0.36 mm ketinggian bolong. Oleh itu, kebolehan gandingan kod MpCCI dalam menangani masalah FSI terbukti dengan cemerlang. Kerja ini dijangka akan menjadi rujukan dan garis panduan dalam industri mikroelektronik.

INVESTIGATION OF WIRE SWEEP DURING PBGA ENCAPSULATION PROCESS USING FLUID STRUCTURE INTERACTION

ABSTRACT

The reduction of IC chip size has a significant impact to the modern electronic industry especially on the circuit design and IC assembly process. The increasing of I/O counts in a small scale IC chip result in severe wire deformation and deformation issues during transfer moulding process. In this research, visualization of wire sweep phenomenon during the encapsulation process of plastic ball grid array (PBGA) package is studied through a three-dimensional (3D) fluid structure interaction (FSI) technique; which FV- and FE-based software are connected by using mesh-based parallel code coupling interface (MpCCI). The effect of polymer rheology, inlet pressure, arrangement of inlet gate, number of stacked die, wire diameter and size of mould cavity vents, on the melt flow behaviour, wire sweep, filling time, cavity pressure and stress distributions, are mainly studied. A 3D model of mould and wires was created by using GAMBIT, and the fluid/structure interaction was simulated by using FLUENT and ABAQUS software integrated with MpCCI for the real-time calculations. The Castro-Macosko model and Kamal model are used to incorporate the polymer rheology and the Volume of Fluid (VOF) technique is applied for melt front tracking. User-defined functions (UDFs) were incorporated to allow the curing kinetics. However, in the experimental work, the effects of FSI phenomenon in the PBGA package was studied using a scaled-up package size to mimic the encapsulation process. The effects of stacked die, inlet gate arrangement, outlet vent, and inlet pressure of mould cavity on the melt flow behaviour and wire sweep were

investigated. The constant viscosity of test fluid was utilised for experiment. The numerical results of melt front patterns and wire sweep were compared with the experimental results and it was found in good conformity. Three types of Epoxy Moulding Compound (EMC) were utilized for the study of fluid flow within the mould cavity. The melt front profiles and viscosity versus shear rate for all cases were analysed and presented. The numerical results of melt front behaviour and wire sweep were compared with the previous experimental results and found in good agreement. In the present study, the lower viscosity shows the lower air trap, lower pressure distributions and lower wire deformation. Optimised design of the PBGA gives better PBGA encapsulation process and minimises the wire sweep. The physical and process parameter (i.e., pressure inlet, wire diameter, vent height) were optimised via response surface methodology (RSM) using central composite design (CCD) to minimise the deformation of wire sweep, filling time and void in package during the PBGA encapsulation process. Fluid structure interaction (FSI) was considered in the optimisation of the PBGA encapsulation process. The optimum empirical models were tested and well confirmed with the simulation results. The optimum design of the PBGA with 12 wires for both physical and process parameters ware characterised by 5.57 MPa inlet pressure, 0.05 mm wire diameter, and 0.36 mm vent height. Therefore, the strength of MpCCI code coupling in handling FSI problems is proven to be excellent. This present work is expected to be a reference and guideline for microelectronics industry.

CHAPTER 1

INTRODUCTION

The introductory background of the IC package encapsulation process is presented in this chapter. The technical challenges in wire deformation, encapsulation process simulation and Plastic Ball Grid Array (PBGA) package are also briefly discussed. In the later sub-chapters, the problem statement, the significance of the current study, research objectives and contribution, the scope of study and the thesis outline are presented.

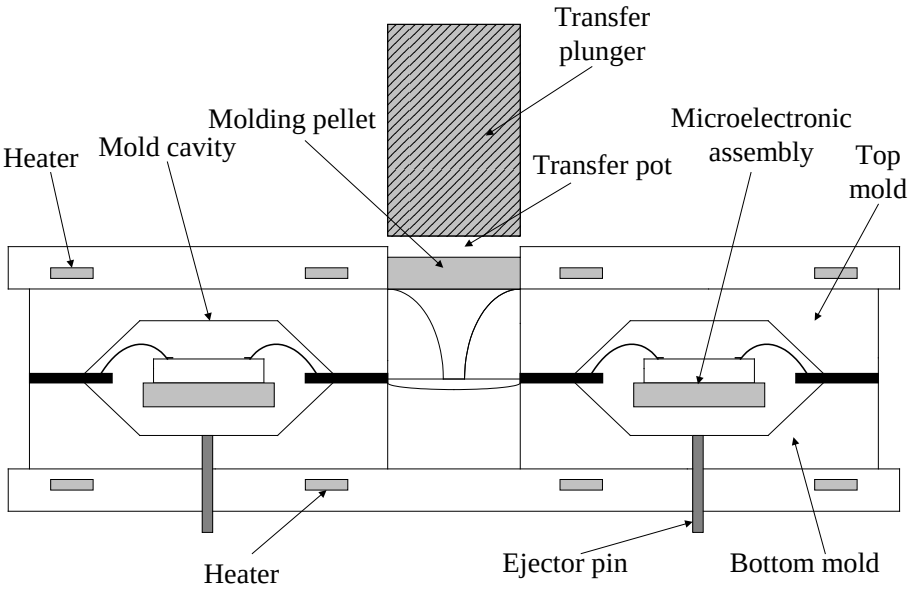
1.1 Background

Transfer moulding is an economical method for encapsulation process. During transfer moulding process, the epoxy moulding compound (EMC) is transferred from a reservoir into the cavities under the application of heat and pressure. The processes of transfer moulding are shown in Figure 1.1(a) and (b).

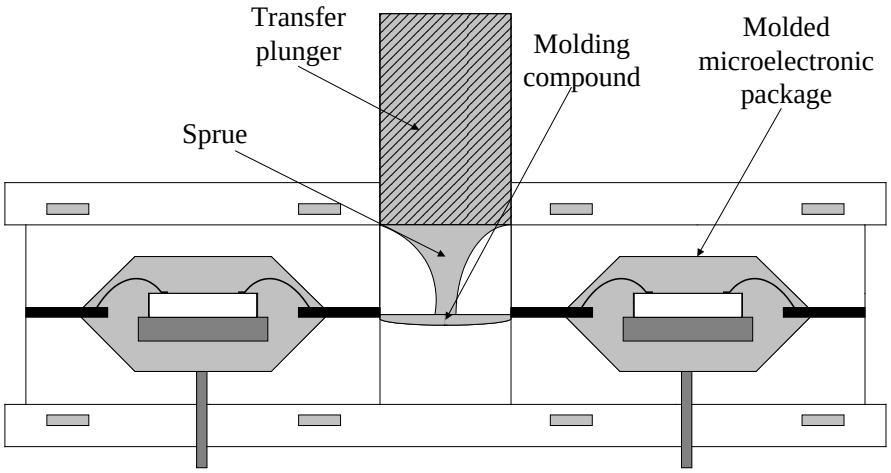
Transfer moulding is a two-step process. In the first step, the melt front of EMC flows and fills up the mould cavity. In the second step, it involves the processes of curing, packing, cooling, and solidification. After the EMC fills up the mould cavity, there is a series of chemical reactions taking place in the mould cavity. As a result, the viscosity of EMC increases before it starts to gel and solidify.

If the plunger pressure is high, it might cause defects within the IC package. In the package, wire bonding is still the dominant microelectronic packaging technology (Kung et al., 2012). The more typical examples of process defects include wire sweep, misaligned leads, paddle shift, warpage, voids, incomplete curing, non-uniform encapsulation and etc. An illustration of defect sites and types, which occur

during transfer moulding process, is shown in Figure 1.2. These defects can be eliminated by the stringent design of mould cavity and optimized parameter settings to minimize shear rate and flow stresses during transfer moulding process.



(a) Before moulding.



(b) After moulding.

Figure 1.1 Transfer moulding of encapsulation process (Ardebiri and Pecht, 2009): (a) Before moulding and (b) After moulding.

In the continuous miniaturization of IC package, there are rising technical challenges in circuit design and assembly processes of IC packages.

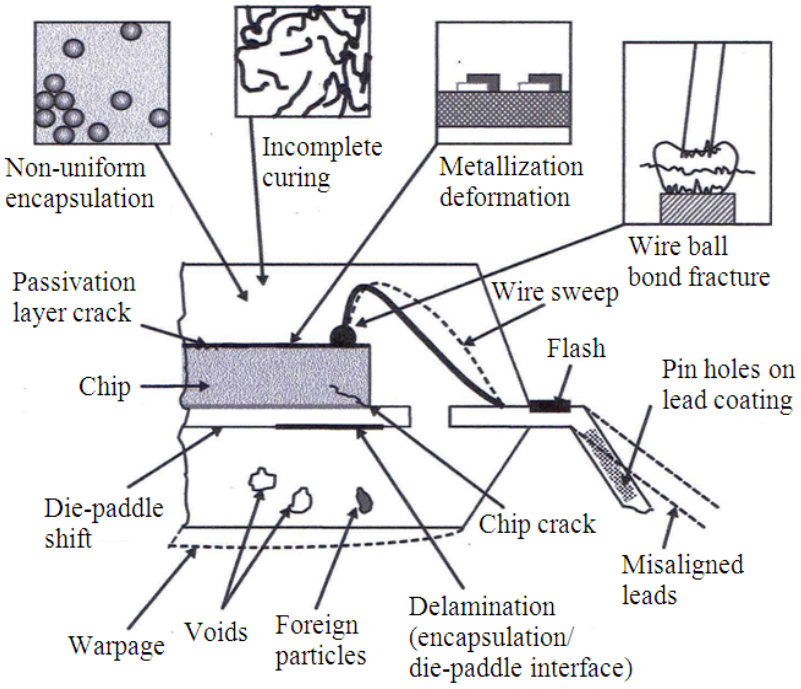


Figure 1.2 Defects produced during the encapsulation process (Ardebiri and Pecht, 2009).

However, the miniaturization of IC package with increasing number of input/output (I/O) counts has resulted in serious wire sweep during transfer moulding process. An illustration of epoxy moulding compound (EMC) behaviour during the encapsulation process is shown in Figure 1.3. Large wire deformation may initiate several problems such as open circuit and short circuit (Su et al., 2003). Therefore, wire deformation has been classified as the vital issue in the IC encapsulation process (Jong et al., 2005). Many researchers have attempted to solve this problem by using the computer-aided engineering (CAE) to predict the wire sweep problems.

Wire sweep is most often caused by the EMC that flows transversely across the bond wires during encapsulation process, which usually occurs around the mid-span of a wire.

The wire sweep in the encapsulation process involves an interactions between fluid flow and structural deformation, which making it a typical fluid-structure interaction (FSI) problem. Numerous researchers have focused on this issue using various simulation tools such as CFD and CAE techniques.

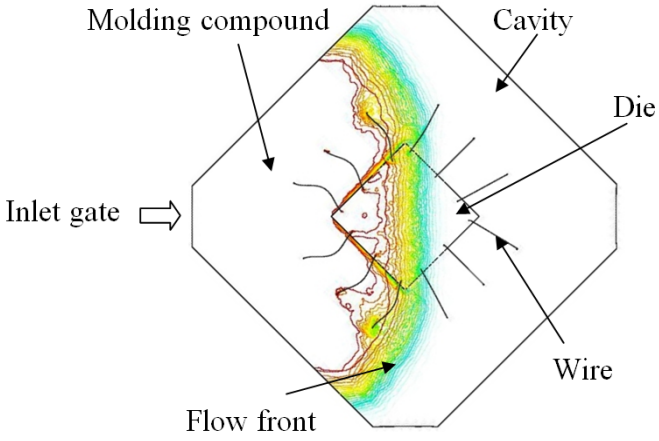


Figure 1.3 Epoxy moulding compound flows into the cavity.

Currently, EMC is widely used as the encapsulant material in plastic encapsulated IC packages (Lu et al., 2009). EMC has the advantage in terms of manufacturability, availability, and low cost. The rheological properties of EMC also play an important role that may influence the final quality in the encapsulation process. This is because the encapsulation process and final physical appearance of IC packages are much dependent on it. The most common rheokinetic model used is the Castro-Macosko model. It is especially useful in predicting the viscosity of

thermoset polymers (Abdullah et al., 2009). The EMC rheological effects on wire deformation and melt front behaviour will also be discussed in this research work.

1.2 Plastic Ball Grid Array (PBGA)

PBGA is classified as a high-density IC packaging technology that could accelerate the advancement of microelectronic industry. This is determined by a broad adoption of PBGA in convenient multimedia products. Since then, the market opportunities for PBGAs have extended more than 30% per year (Ardebiri and Pecht, 2009). This technology has enabled more dies stacking design in a single package for higher performance. Besides that, this will also provide outstanding performance and manufacturing cost reduction to the end users.

Many advantages of using PBGA over similar lead count leaded devices include (Mawer, 1996) several aspects:

a. Reduce board space due to the compact package design.
b. Provide better thermal and electrical performance.
c. Excellent surface mount yields when compared to fine pitch leaded devices.
d. Design of package with lower profile characteristics (i.e., overall thickness).
e. Handling and assembly compatibility with existing surface mount technology, test and equipment.
f. Diminish the total cost compared to leaded devices due to reduced scrap, rework and lack of need for fine-pitch assembly equipment.

Figure 1.4 and Figure 1.5 depict the schematic of cross-section and a typical plastic ball grid array (PBGA) package. In the PBGA technology, substrate and solders balls have been applied to replace the traditional lead-frame, which offers

many advantages over fine-pitch technology such as providing a high-density of interconnector. Moreover, these include other advantages on better assembly process and electrical performance.

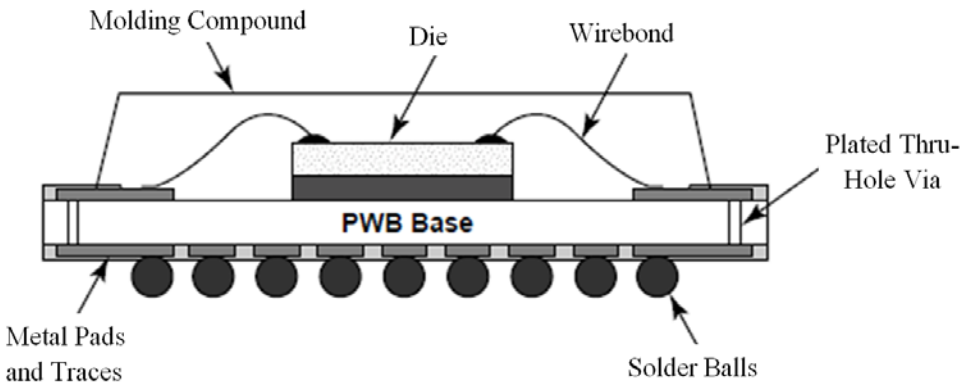


Figure 1.4 Schematic cross-section of a typical PBGA package (Zhang et al., 2000)

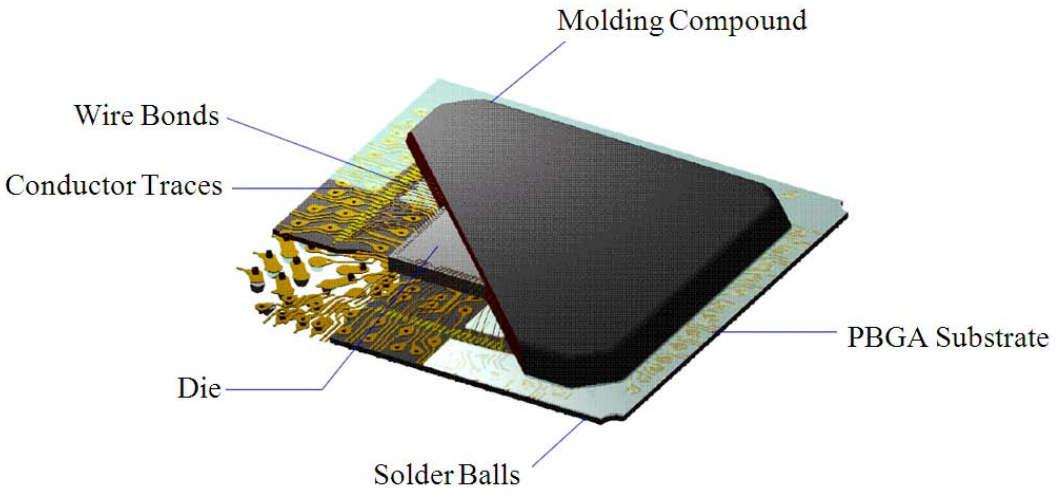
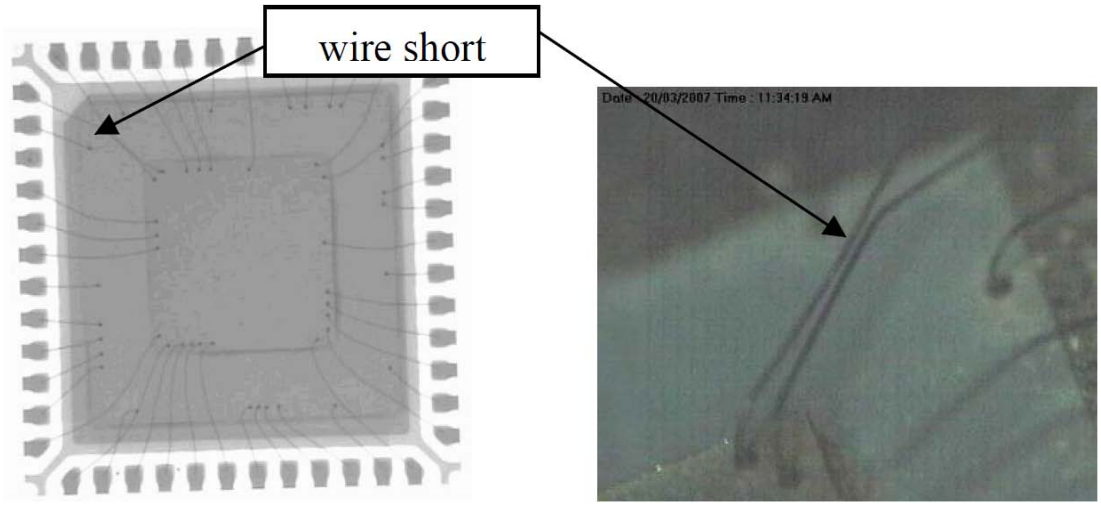


Figure 1.5 Package of Plastic Ball Grid Array (PBGA) Configuration (Texas Instrument, 2009).

1.3 Problem Statement

Recent advances in IC packaging, for example, moulded array package technology of PBGA encapsulation process by the transfer moulding process,

subjected to the flow induced stress of EMC. This flow stress can cause the lead-frame and the wire bonds to deform permanently from their original geometry. A phenomenon of wire sweep is shown in Figure 1.6. Large deformation of a bonding wire can cause package failure; either short circuit or open circuit due to the contact between adjacent wire and a broken wire. Even if the deformation is not severe, it will deteriorate electrical and mechanical performance of the device and shorten its lifetime. Therefore, it is important to minimise or avoid the wire sweep deformation during encapsulation process based on the proper control of package design and operating process.



(a) Actual image. (b) Enlarge image.

Figure 1.6 Example of wire sweep in a package (Abdullah, 2008): (a) Actual image and (b) Enlarge image.

The wire sweep during encapsulation is considered as a fluid-structure interaction (FSI) problem, which always involved the interaction of EMC flow and package structures. The resulting drag force from the EMC flow causes wire deformation, this phenomenon is known as the wire sweep. However, the report of the FSI application for the wire sweep is still lacking in the simulation of two-ways

analysis and also in the experimental work. The FSI phenomenon in encapsulation process should be addressed to solve the FSI-related defects.

In the actual PBGA encapsulation process, the visualisation of FSI phenomenon is difficult and constrained by small IC package size, limitation of visualization equipment, and the costlier experimental setup. Besides that, the non-transparent packaging mould used in the PBGA encapsulation process also causes difficulties in visualising the FSI phenomenon. Typically, the deformation of wire bonds is observed from the top view of the package using X-ray. It is the best method for observing FSI phenomenon through vertical and top views of the mould for better understanding. Moreover, investigations of the wire sweep phenomenon can also be conducted by using simulation tools.

Optimal design of PBGA provides the optimum encapsulation process and minimizes the wire sweep. The physical and process parameter (i.e., pressure inlet, wire diameter, vent height) should be optimised to minimise the deformation of wire sweep, filling time and voids in package during the PBGA encapsulation process. However, FSI should be considered in the optimisation of the PBGA encapsulation process.

1.4 Significance of the Study

By considering the problem statement, the numerical study of encapsulation process is important in improving the quality of IC package and reducing the production cost. This will further decrease the development cost needed in producing electronic gadgets such as mobile phones, PC tablets, laptops and etc.

The quality of IC package is a major concern. In the ongoing trend, most of the PBGA package is produced in a thin and wide pattern, which could possibly

trigger even more serious process defects during encapsulation process. The more common process defects such as wire sweep, warpage and voids could decrease the overall production yield. These critical defects have to be considered during the initial stage of package development (Sze and Papageorge, 1998). It is reported that the industry is attempting to produce thin IC packages with more stacking dies and high density of wire.

In the current research, both simulation and experimental results are important, which can provide useful guidelines in understanding the FSI phenomenon that occurs during encapsulation process. Moreover, the knowledge acquired from the research can be a good reference in the industry.

1.5 Objectives of the Present Research

The general objective of this research work is to investigate the fluid structure interaction during PBGA encapsulation process. The understandings of encapsulation process are significant for PBGA designers and engineers to obtain the optimal PBGA package design and process control. In order to achieve these aims, six main objectives were set out as mentioned below:

1. To validate the predictions of modelling tools, CFD and CAE in the fluid flow and structural analyses of PBGA encapsulation process.
2. To predict and comprehend the effect of inlet gate and outlet vent arrangements on the fluid melt front profile and wire deformation during the encapsulation process.
3. To investigate the effect of stacked dies and gate orientation on wire sweep during encapsulation process of scale-up PBGA.

4. To perform the effect of inlet pressure to the Von Mises stress and shear stress of wire on the mould filling process of scale-up PBGA.
5. To carry out the effect of EMC rheological properties on wire sweep by applying the Castro-Macosko viscosity model and the Kamal curing models in the encapsulation process of actual size PBGA.
6. To optimise the physical and process parameters, those are found to be having a dominant effect on wire deformation, mould filling time and voids in the actual size PBGA encapsulation process.

1.6 Contribution of the Study

This research work contributes to the knowledge development in microelectronics packaging in the following aspects:

a. Introducing a new method to solve the FSI of wire sweep in the encapsulation process by using two-ways and real time MpCCI coupling method.
b. The numerical analysis uses User-defined functions (UDFs) to account for curing kinetics. The Castro-Macosko viscosity model with curing effect was written into C language using Microsoft VISUAL Studio 2005 and compiled as UDF in FLUENT.
c. Scaled-up PBGA encapsulation process contributes the clear visualisation of the FSI phenomenon, fluid flow and wire sweep mechanism through the top view of transparent mould.
d. The parametric studies and optimisation of PBGA encapsulation process contribute better understanding, clear visualisation on fluid and structure of wire sweep phenomena for engineers in microelectronic industry.

1.7 Scope of Research Work

In this research work, 3D computer analysis is applied via MpCCI in understanding FSI phenomenon during encapsulation of PBGA package. The effect of EMC rheological properties, stacked dies, inlet gate arrangements, and size of outlet vents on the overall wire sweep, EMC melt front, and pressure and shear stress distributions is studied.

In the simulation, EMC is considered as a generalised Newtonian fluid (GNF). In the encapsulation process, the EMC flow behaviour is modelled by the Castro-Macosko viscosity and Kamal curing models. These models are written in C language and compiled by using user-defined functions into the FLUENT analysis. Volume of fluid (VOF) technique is applied for melt-front tracking. The subsequent structural deformation of wire sweep is computed in ABAQUS. The present work discusses the effect of inlet pressure on wire deformation, stacked dies and inlet gate arrangements on fluid flow during the encapsulation process on scale-up PBGA by experimentally and simulation. This research also discusses the optimisation of physical and process parameters of the PBGA package for the analysis of wire sweep, void and filling time during the encapsulation process. Besides, the flow effect due to different inlet pressure is also considered in this study. The fluid flow during encapsulation process is viewed from the top, and comparisons are made between the numerical and experimental results.

In the present study, the computational fluid dynamic code FLUENT 6.3 is used to analyse the effect of outlet vent and inlet gate arrangements on flow behaviour during encapsulation of scale-up four wires PBGA. A 3D model is developed and analyzed using the finite volume method. Three different arrangements of mould, namely, 2-vents, 4 vents and 6 vents, and 1 inlet gate, 2 inlet

gates and 3 inlet gates are applied in the analysis. Two different die height and inlet gate arrangement are studied numerically and experimentally in scale-up eight wires PBGA. The Castro–Macosko model is used to consider polymer rheology with curing effect in the viscosity behaviour of the EMC. Three different EMC properties, designated as Cases A, B and C, were studied for analyzing of fluid flow and wire sweep inside the mould cavity. Optimization of package design and process parameters is also studied. A program written in C language is employed in the User-Defined Function (UDF) to calculate the curing kinetics of EMC. The VOF technique is also applied to track the flow front of the EMC. The numerical results of the flow patterns and the filling time of the three arrangements of EMC properties are compared.

Wire sweep profiles and pressure field are analyzed and presented. The simulation results are compared with the previous experimental result that available in the literature and it is found in good agreement. In the simulation, the Castro–Macosko viscosity model with considering curing kinetics was applied to describe the EMC behaviour. However, volume of fluid (VOF) technique was applied for to track the EMC flow front. Void problems or incomplete filling around packages and the multi-inlet gate are also discussed in the present paper. The results of the simulation and previous experimental results are found to be in good agreement.

1.8 Thesis Outline

In this thesis, there are five chapters. In Chapter 1, a brief presentation on encapsulation process, background of the study, encapsulation process simulation, PBGA, problem statement, significance of the study, objectives and scope of research works are introduced. In Chapter 2, literature studies of mould flow and

wire deformation in the PBGA encapsulation process are introduced. The numerical and experimental approaches are discussed in Chapter 3. In Chapter 4, model validation as well as results and discussions are presented in details. The discussion of wire sweep defect has also been extended to several case studies, which include the effect of inlet gate arrangement, stacked dies, inlet pressure, rheological properties, physical and process parameters. The process optimization is also being presented in the chapter. In the final chapter, the conclusion and recommendations for future works are discussed.

CHAPTER 2

LITERATURE RIVIEW

2.1 Introduction

Smaller, faster and cheaper characteristics of complex microelectronic devices are the demands in current electronic trend, the modern packages such as, mobile phone, Personal Data Access (PDA), other portable and handheld electrical products are necessary to increase I/O numbers, reduce die and package sizes and manufacturing costs. Nowadays, microelectronic devices have many types of modern package, e.g. flip chip; wafer level packaging and tape automated bonding technologies (Schueller et al., 1997). In the IC packaging, wire bonding technique is still the dominant microelectronic packaging technology (Kung et al., 2012) such as PBGA and its prospectus market has been gradually increase to 2020 (Prior, 2010). Low cost of IC package trend and small form factor packaging is shown in Figure 2.1.

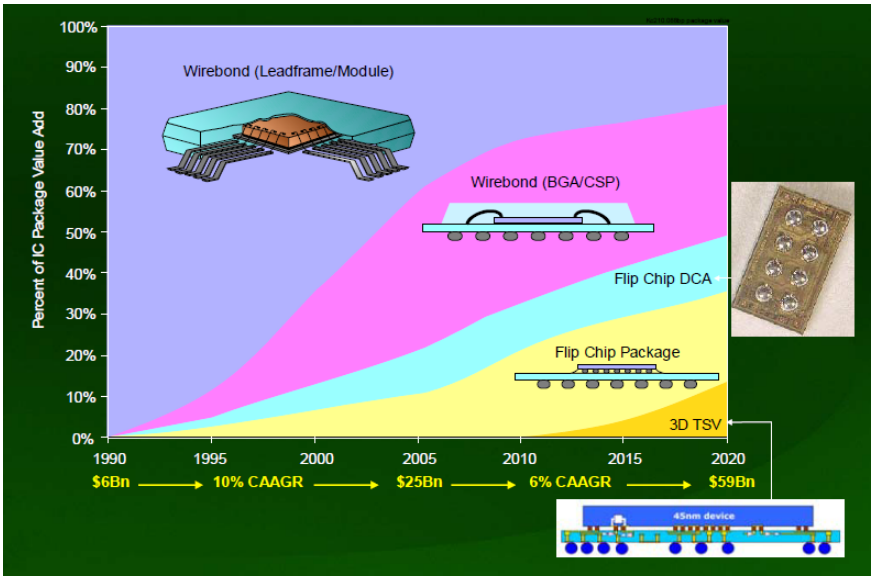


Figure 2.1 IC Package value trend of low cost and small form factor packaging (Prior, 2010).

Integrated Circuit (IC) devices have a great constraint in these products. To keep these IC devices working appropriately, it needs to protect the IC from physical break and contamination. The major objectives of IC encapsulation process are given as followed (Chen, 1990).

a. Protection of the device from mechanical and chemical hazards.

b. Thermal path for heat dissipation.

Due to the cause of cost and efficiency, modern electronic package uses plastic as the body material for packaging. Moulded plastic is then used to protect the chip and leadframe from physical damage and contamination.

In this chapter, the various issues that related to the problems arising from the encapsulation process and how to overcome these problems are solved and described base on previous papers. The paper review begins from moulding process experimentally and numerically analysis of encapsulation, the influence moulding process parameter and design packages of the wire bonding profile and fluid flow behaviour, and papers discussed optimization of the parameters.

2.2 Moulding Process

Transfer moulding is the most popular and well establish microelectronics encapsulation technique for electronics packaging. Typically, several moulding defects in this process are wire sweep, paddle shift, short shot, air trap, as well as other stress-induced problems (Abdullah et al., 2010). These defects may attribute by various factors such as improper selection of processing conditions, moulding material, lead frame layout, or mould design. Furthermore, trends to produce faster, smaller, and cheaper electronic products are driving packaging technology toward a higher packaging density with thinner and smaller profiles. This condition has made

the process of encapsulation much more complicated and unpredictable (Chang et al., 2004). The samples of some packages are shown in Figure 2.2 which is the die stacking technology that applicable for memory devices or memory-logic devices.

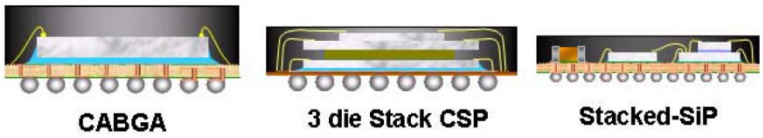


Figure 2.2 Conventional CABGA and thin multi-die stacking or stacked SiP (Lee et al., 2006)

In recent years, there has been a significant demand for stacked die technology due to it characteristics. The stacking of chips in leaded and substrate package can efficiently minimize package size and cost (Abdullah et al., 2008, 2010). Stacked-chip packages can be packed using die attach, wire bonding, and moulding methods. However, some challenges in stacked die development were thin wafer back grinding and handling, thermal issues due to the low thermal conductivity of the nonconductive die attach paste between die to die, and delamination issues due to package material mismatch, among others (Abdullah et al., 2009, Yao et al., 2003). Many researchers have studied this mould-filling process. However, only an amount of substantial works that related to the present study are reviewed in the current chapter.

The numerical analysis that considers the time-dependent behaviour of EMC and the presence of inserts in the mould cavities during encapsulation process is complicated and difficult. However, once a good quantitative model of the encapsulation process has been verified, considerable time and cost can be saved. Long and costly experimental runs are no longer needed to be carried out by trial and error to restore a mould or qualify a new compound.

3-D FEM model of PBGA package was simulated by Tay and Lee (2002) considering different gate positions. Teng and Hwang (2008) studied the behaviour of EMC melt fronts during the LQFP mould filing process, which modelled by using Castro-Macosko and Kinetic's models.

Recently, Khor et al. (2011) investigated the effect of different inlet gate arrangements in TQFP encapsulation process. GAMBIT was utilized to build a 3D model of plastic TQFP package and fluid flow analysis was solved by FLUENT software. Su et al. (2003) introduced “In-Pack” for wire sweep analysis that combined global flow analysis (C-MOULD) and structure analysis (ANSYS).

CFD code (CFD-ACE-U) and a structural dynamics code (FEM-STRESS) was used by Yang et al. (2001) through a two-way coupling technique. They used CFD and structural dynamics codes to compute the transient flow field in encapsulation process and the transient deformations and stresses in wires.

Lim and Lee (2000) performed numerical simulations of three-dimensional (3D) mould filling during resin transfer moulding. They used the finite element method to predict the flow front while the epoxy moulding compound (EMC) is injected into a mould cavity preloaded with a porous fibrous pre-form. To check the 3D EMC front location as a function of time inside the pre-form, an optical fibber is used as sensing element. The experimental data were found to agree well with the numerical results.

Sato and Yokoi (2000) had developed a transparent mould with a glass-inserted structure, which enables observation of the dynamic melt behaviour inside the cavity along the thickness direction. The melt flow profile and the behaviour of the flow front surface were recorded using a high-speed video system and the data was analyzed with an image processor. Several experiments revealed that the melt

advanced slipping on the cavity surface or lead frame. The melt flow is suggested to be affected by the melt in the opposite cavity beyond the lead frame.

Teng and Hwang (2008) studied the prediction of EMC flow front in the mould filing process of LQFP package. The EMC flow was modelled using Kinetics model and Castro-Macosko viscosity model. However, they did not include the degree of conversion of the moulding compound in their study.

Nguyen et al. (2000) studied transfer moulding numerically. They presented, discussed, and compared the results from experimental and computational studies on plastic encapsulation for a 144-lead TQFP package. The experimental results were obtained using an instrumented moulding press system. The computational predictions were carried out by using newly developed software for the modelling of transfer moulding process. Their predicted results were compared with the corresponding experimental measurements in terms of pressure, temperature, and flow front advancement in the cavities and runners. The experimental and computational results were demonstrated a good conformity, especially for the flow-front shapes and locations.

Shojaeia et al. (2002) presented numerical simulations of a 3D isothermal mould filling process based on the concept of the control volume by using finite element method. Quasi-steady state and partial saturation formulations were employed to track the flow front advancement in numerical analysis. Pre-form permeability may be a function of fluid velocity. Hence, the proposed numerical schemes accounted for the velocity dependency of permeability. The correlation between pre-form permeability and fluid velocity during mould filling had made the numerical schemes complex. The two schemes were evaluated by a comparison with analytical solutions for simple geometries and it was found in excellent agreement.

Gokce and Advani (2004) investigated the moulding process, where the resin is injected into the mould cavity containing preplaced reinforcement fabrics, through openings known as gates. During the process, the displaced air leaves the mould through openings (vents). Gate and vent locations were found significantly affect process output, such as fill time, pressure requirements, and whether or not the fabrics will be saturated entirely. In their study, a cascaded optimization algorithm was proposed for simultaneous gate and vent locations optimization in the presence of race tracking during mould filling. This algorithm is created by integrating branch and bound search with map-based exhaustive search.

Abdullah et al. (2007) numerically examined the encapsulation of the stacked-Chip Scale Package (S-CSP). They presented a study of flow visualization during encapsulation in S-CSP. The Navier–Stokes equation was solved by using the finite difference method. The prediction of numerical model was verified by the experimental results, the flow front profile was found in good agreement. The predictions also showed that the short shot problem that occurred for the die top clearance lower than 0.25 mm.

Recently, Khor et al. (2011) studied the effect of inlet gate arrangement on the filling time during TQFP encapsulation. A 3D model of plastic TQFP packages was built using GAMBIT and simulated by FLUENT software.

Ishiko et al. (2006) presented a thermoelectric simulation for optimizing the wire-bonding position in insulated gate bipolar transistor modules, using the SOLIDIS 3-D simulator. They demonstrated that wire-bonding optimization by thermoelectric simulation could contribute not only to the realization of more compact power modules but also to improvements in the module reliability.

The rheological properties of the EMC play a crucial role in the encapsulation process, where the rheology is defined as the science of flow and deformation of matter (Abdullah et al., 2009). The final physical properties of IC package and processing rely on its characteristics. The most common and excellent rheology model for EMC material is Castro–Macosko model, especially for thermoset polymer rheology (Abdullah et al., 2009). The effect of gaps between the die top and mould cap surface and between adjacent dies on EMC rheology during stacked-chip-scale packages encapsulated was reported by Abdullah et al. (2009). Rheokinetic simulation of the mould-filling behaviour, mould void, and wire sweep dependences of gate size was analyzed by Lee et al. (2006). Three dies stack CSP 294LD of 4 × 4 mould array selected in this study with four different mould gate types. The simulation performed full 3 dimensional rheokinetic of mould filling behaviour by applying Castro-Macosko model. Experimental validations used for checking melt front advancements, mould voids and wire sweeping dependencies for each gate type.

Chen et al. (2007a) had successfully integrated the mould filling simulation and structural analysis software to predict the lead-shift phenomenon in an IC package. Their simulated results were verified with experiments. In this simulation, only unbalanced flow caused pressure difference was considered as loadings for the simulation.

2.3 Experimental Apparatus of Transfer Moulding Process

To enhance the understanding on the effects of the process parameter and design of IC package on the filling process, wire sweep or wire displacements. There is a need of experimental apparatus for the visualization during the transfer moulding process. The experimental set up had been introduced by Yang et al. (2000), Reddy et

al. (1998), Yoshihara et al. (1999b), Chai and Zohar (1999), and Han and Wang, (1995a, 1995b).

Yang et al. (2000) introduced PBGA encapsulation process numerically and experimentally. In this study, the encapsulation mould was covered with a transparent top plate and the cavity filling process during transfer moulding was recorded by using a CCD camera. The wire sweep in the filling of cavities using original plane package and ribbed packages were evaluated and compared. Experiment facilities for flow visualization in the encapsulation process are schematically shown in Figure 2.3, and the detailed construction of mould is shown in Figure 2.4.

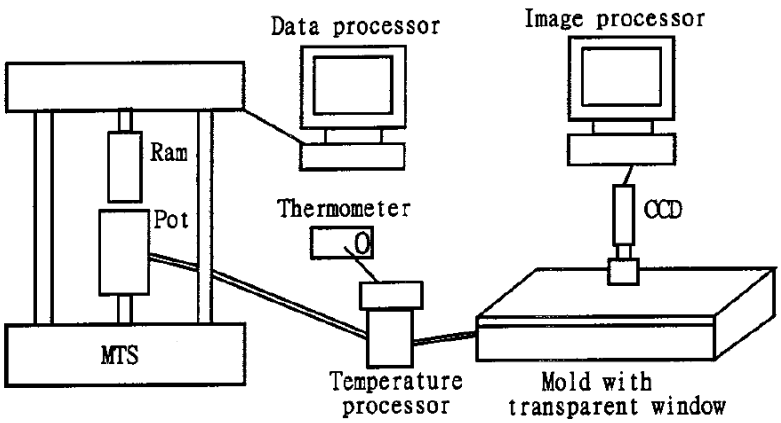


Figure 2.3 Schematic of facilities for flow visualization experiment (Yang et al., 2000).

The geometry of the cavity and typical wire bond geometry used in the experiment are shown in Figure 2.5. The effects of ribbed geometry on the thermal warpage and wire sweep of PBGA encapsulation were investigated in their study. Three rib geometries namely border, diagonal, and cross with a variation of rib widths and thicknesses were compared with the original plane geometry. Finite element analyses of thermal warpage during the reflow process of PBGA moulding with and without ribbed geometry were also carried out. They concluded that the cavities with ribs were significantly reduced the wire sweep compared with non-ribbed cavities.

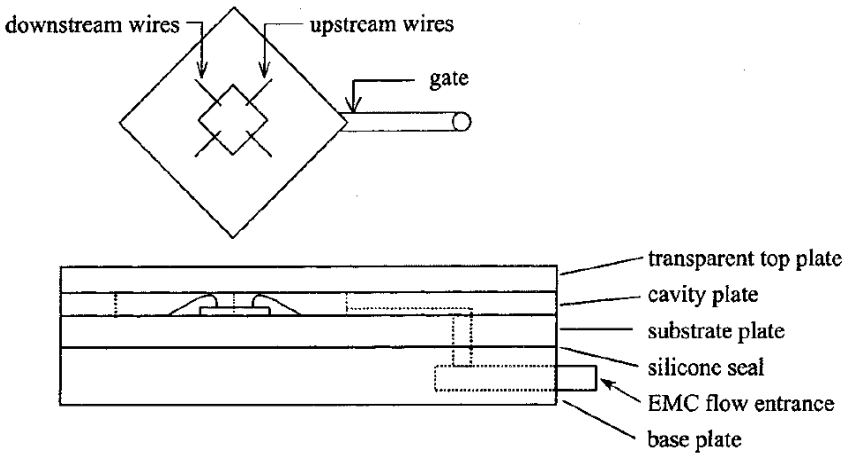
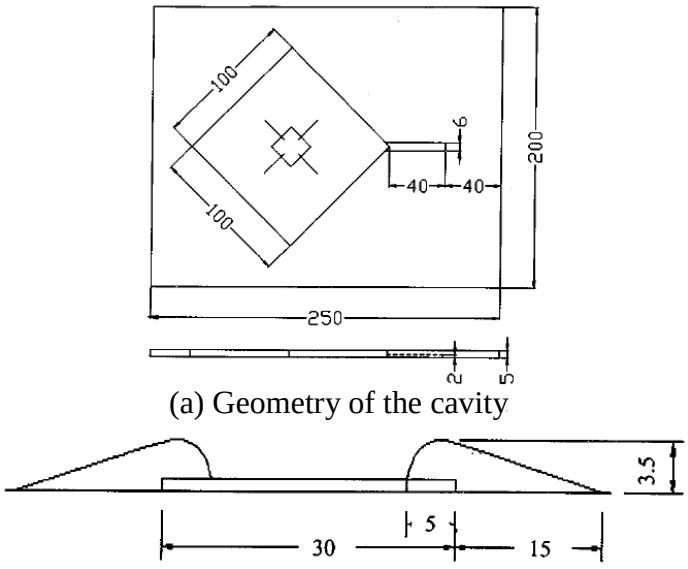


Figure 2.4 Sketch showing the detailed construction of mould (Yang et al., 2000).



(a) Geometry of the cavity

(b) Typical wirebond geometry

Figure 2.5 Sketch showing (a) geometry of the cavity and (b) typical wirebond geometry (Yang et al., 2000).

Reddy et al. (1998) verified the numerical predictions of the fluid-front advancement and pressure variation within the cavity by conducting experiments with mould cavities in the microchip encapsulation process. The experimental setup as illustrated in Figure 2.6, which consists of an Instron Universal Testing Machine (UTM) that was utilized to obtain a constant velocity of the piston in a hydraulic piston-cylinder. A steel pipe was connected from the cylinder to the mould.

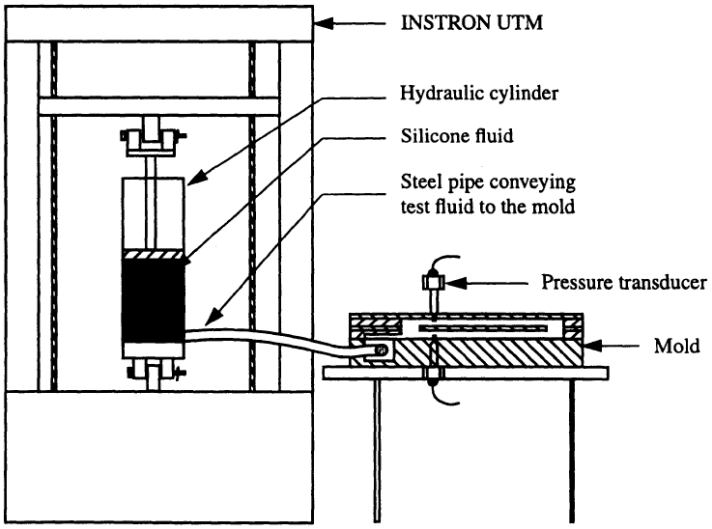


Figure 2.6 Schematic of experimental set up (Reddy et al., 1998)

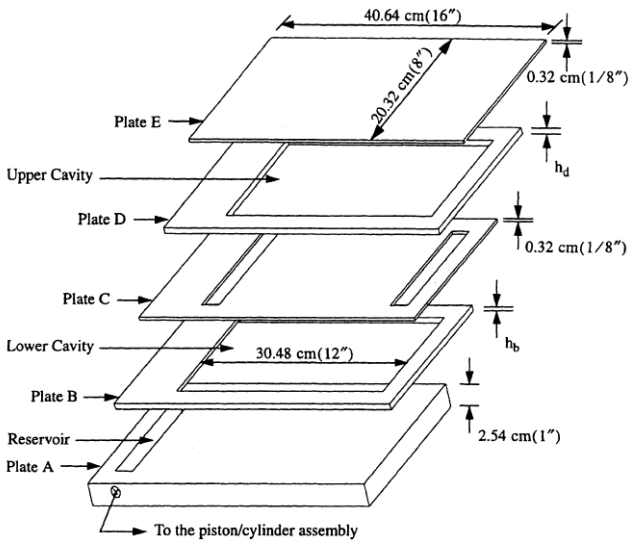


Figure 2.7 Geometry and dimension of the experimental mould plates (Reddy et al., 1998)

The experimental mould plates used by Reddy et al. (1998) are shown in Figure 2.7. The mould consists of five rectangular plates of various thicknesses, which were held together by eighteen screws that positioned along the outer edge. To enable a video recording of the fluid-front advancement during mould filling, the transparent Plexiglas was used as one of the mould plates.

Yoshihara et al. (1999a) investigated wire sweep by carried out an experiment considering the loop shape of the wire during the plastic IC packages encapsulation through the transfer moulding technique. The experimental investigation of the wire sweep was performed and its governing factors were studied. The wire bonding conditions of the bonder were varied, producing various loop shapes as shown in Figure 2.8. The specimen was a wire loop on the island of the lead frame (Figure 2. 9). Their experimental setup is shown in Figure 2.10. The specimen was positioned in the cavity, in which the wire loop was perpendicular to the direction of liquid flow (Figure 2. 11).

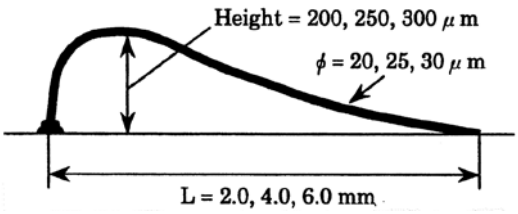


Figure 2.8 Wirebond geometry used in the experiments by Yoshihara et al. (1999a).

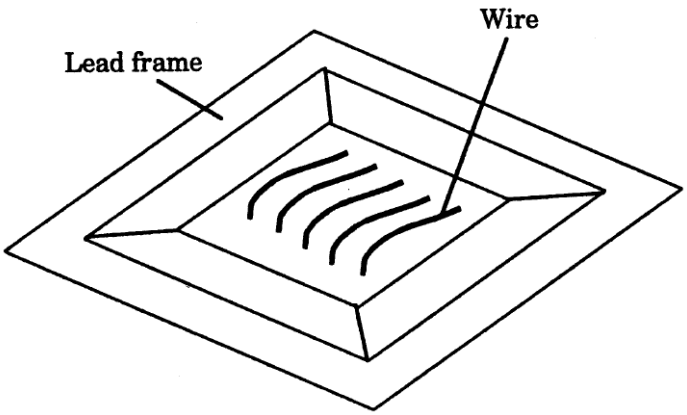


Figure 2.9 Specimen that fabricated by Yoshihara et al. (1999a).