DESIGN OF MULTIPLY-BY-TWO AMPLIFIER FOR 1.5 BIT PIPELINED ANALOGUE-TO-DIGITAL CONVERTER APPLICATION

TENG JIN CHUNG

UNIVERSITI SAINS MALAYSIA

2014

DESIGN OF MULTIPLY-BY-TWO AMPLIFIER FOR ANALOGUE-TO-DIGITAL CONVERTER APPLICATION

By

Teng Jin Chung

Thesis submitted in fulfilment of the requirements for the Master of Science (Electric & Electronic Engineering)

July 2014

ACKNOWLEDGEMENT

I would like to give my deepest appreciation to some of the parties who had help and guide me during my dissertation project implementation.

First of all, I would like to thank School of Electrical and Electronic of Engineering, Universiti Sains Malaysia for this Master of Science in Microelectronic Engineering Course.

Secondly, I would like to thank Talent Corp for giving me the chance to sign up for this Fast Track Master program.

Then I would like to express my thankfulness to my supervisor, Mr. Zulfiqar Ali Abdul Aziz for providing me guidance and help during this research. Besides that, I would like to thank CEDEC for giving me software support to complete this research.

Next I would like to thank my manager, Ho Nee Shen, who giving me full support and being understanding and considerate.

Last but not least, I would like to thank my friends and family for giving me the support during this whole year of my master study.

Table of Content

List of Tables

List of Figures

List of Solutions

List of Abbreviation

ADC	Analogue-to-Digital converter
CMFB	Common-mode Feedback
CMOS	Complementary Metal Oxide Semiconductor
CMRR	Common- mode Rejection Ratio
DC	Direct Current
NMOS	n-channel MOSFET
op-amp	Operational Amplifier
PMOS	p-channel MOSFET
PSRR	Power Supply Rejection Ratio
DRC	Design Rules Check
LVS	Layout Versus Schematic
PEX	Parasitic Extraction

DESIGN OF MULTIPLY-BY-TWO AMPLIFIER FOR ANALOGUE-TO-DIGITAL CONVERTER APPLICATION

ABSTRACT

This report explain about the design of multiply-by-two amplifier for Analogue-To-Digital Converter. The specification of the operational amplifier is 40dB of gain, and 1MHz cut-off frequency. Silterra 0.13um process technology is used in this work. The amplifier topology used in this research is Folded cascode which gives larger output swing. Differential pairs Common-mode feedback is used to overcome the mismatch of source current and to fix the folded cascode output voltage level at 350mV. The proposed design was able to achieve DC gain of 44.77dB and 1.06MHz cut-off frequency. The designed amplifier power consumption is very low, which is 9.598mW. Figure of merit of this design are $FOM_1 = 447.11\,MHzpF/mA$ and $FOM_2 = 164.44 MHzpF/mA$. The designed operational amplifier is implemented into the multiply-by-two circuit and was able to achieve 98.75% of accuracy for multiplying the difference in inputs voltage level. A layout design is done for the proposed multiply-by-two amplifier. The layout is tested with parasitic effect considered, the accuracy of output drop to 97.5%.

REKABENTUK MULTIPLY-BY-TWO AMPLIFIER UNTUK KEGUNNAAN ANALOG-TO DIGITAL CONVERTER

ABSTRACK

Laporan ini menjelaskan reka bentuk Multiply-by-two amplifier. Spesifikasi bagi amplifier adalah 40dB gain, dan 1MHz cut-off frekuensi. Silterra 0.13um proses teknologi telah dipakai untuk kerja ini. Topologi amplifier yang digunakan dalam kajian ini adalah Folded cascode yang memberikan ayunan output yang lebih besar. Common-mode feedback differential pair diguna untuk mengatasi masalah mismatch bagi punca arus dan memastikan voltage pada output kekal pada 350mV. Reka bentuk yang dicadangkan dapat mencapai gandaan DC sebanyak 44.77dB dan mempunyai 1.06MHz Frekuensi potongan. Amplifier yang direka menggunakan kuasa yang sangat rendah, yang 9.598mW. Figure of Merit reka bentuk ini adalah $FOM_1 = 447.11\,MHzpF/mA$ and $FOM_2 = 164.44 MHzpF/mA$. Folded cascode amplifier yang direka telah diguna untuk Multiply-by-two amplifier dan ketepatan 98.75% telah dicapai. Reka bentuk susun atur bagi Multiply-by-two amplifier telah dilakukan. Susun atur yang direka telah diuji dengan kesan parasitik, ketepatan output jatuh kepada 97.5%.

CHAPTER 1

INTRODUCTION

1.1 Overview

Analogue-to-Digital Converter (ADC) is a device that used to convert analogue signals (continuous signals) to digital signals (discontinue signals), usually voltage signals is being converted. As most of the sensors have analogue output that needed to be process by the microprocessor which only process digital signal, ADC act as the link between the sensors and the microprocessor. With the increase needs of portable devices, such as the smartphone (with camera) and tablet pc, high speed and high accuracy ADC is playing a very important role in converting analogue audio, image and video signal into digital processing(Lee & Geiger 1999). The resolution and speed of the ADC will affect the performance of the system. Lower power consumption and longer battery life is also an essence for the portable devices. This also led to lower power consumption Analogue-to-Digital (ADC) circuit design. The important aspects to evaluate an ADC is the accuracy, power consumption, speed and area (Sun et al. 2008; Nabavi & Lotfi 2006).

There is a few ADC architectures that were used to satisfy different requirements, such as Flash ADC, Pipelined ADC, Successive Approximation Register (SAR) ADC and Sigma-Delta ADC. The most popular ADC architecture is the Pipelined ADC for sampling rates up to 100 MSPS and resolutions from 8 bits to 14 bits. Pipelined ADC usually have multiple stages structure in which each stage only

work on a few bits. Each stage of the Pipelined ADC performs an operation on the signal, provides the output for the following sampler, and begins the same operation on the next signal. Different stages process different samplers concurrently and throughput rate is depends on the speed of each stage (Leclare et al. 2003).

1.2 Problem Statement

In designing an Analogue-to-Digital converter, the few important parameters for an ADC are accuracy, speed, gain, and power consumption. With each parameter is need to be set based on the requirement to achieve most of the specification is the crucial part of this project. Multiply-by-two amplifier, which is part of an ADC, is also very important to have a better accuracy, speed and power consumption. This research will need to achieve 40dB gain and 1MHz of cut-off frequency. Power consumption is set to be as low as possible, less than 10mW will be the target of this research.

1.3 Objectives

1) To design multiply-by-two amplifier for 12-bit Pipelined ADC for sensor application.
2) To characterise the current consumption and speed of the multiply-by-two amplifier.

1.4 Scopes

This research include the design of multiply-by-two circuit for 1.5-bit pipelined ADC using Cadence. The technology used for this research is Silterra 0.13um process technology. This research cover the simulation part, including schematic and layout, but no chip will be fabricated due to the time constraint. DRC and LVS rules check will

be used to check the layout design and to compare the schematic and the layout design. PEX is run to extract the parasitic effect resulted from the interconnection of layout design.

1.5 Thesis Organization

This thesis is organized into five chapters. The following chapter is the literature review which will explain more about the important topics that is used in this research. It include the topics like Analogue-to-Digital Converter, amplifier topology, common-mode feedback circuit, 1.5 bit pipelined ADC, multiply-by-two circuit and parasitic capacitance. This chapter provide the brief elaboration to understand every circuit and how they are integrated into one schematic.

Chapter 3 describe the methods used to complete this research. Different sub-topic is used to show the details on all the aspect while completing this research. The sub-topics are operational amplifier design, folded cascade op-amp, gain and phase margin of the amplifier, common-mode feedback circuit, characteristic of the op-amp, multiply-by-two circuit, and designing the layout.

Chapter 4 highlights the result of the research. Analysis and discussion is done in this chapter. From the operational amplifier, common-mode feedback cir cuit, to multiply-by-two circuit, all of the result is presented and analysed.

Finally, Chapter 5, the conclusions of the research are presented as well as the findings and contributions of the research are highlighted clearly. In addition, the chapter highlights the possible future works as a continuation of this work.

CHAPTER 2

Literature Review

2.1 Overview

In this chapter, it will cover the studies of some of the important elements for this project, including Analogue-to-Digital Converter (ADC), Amplifier Topology, Common-mode Feedback circuit, 1.5-bit Pipelined ADC, and parasitic capacitance.

2.2 Analogue-to-Digital Converter (ADC)

Analogue-to-Digital Converter (ADC) is a device that used to convert analogue signals (continuous signals) to digital signals (discontinue signals), usually voltage signals is being converted. As most of the sensors have analogue output that needed to be process by the microprocessor which only process digital signal, ADC act as the link between the sensors and the microprocessor.

With the increase needs of portable devices and wireless communication, such as the smartphone (with camera) and tablet PC, ADC is playing a very important role in converting analogue audio, image and video signal into digital processing(Kargaran et al. 2012)(Wenxiao et al. 2009). The resolution and speed of the ADC will affect the performance of the system. Lower power consumption and longer battery life is also an essence for the portable devices. This also led to lower power consumption Analogue-

to-Digital (ADC) circuit design(Cabebe et al. 2013). The important aspects to evaluate an ADC is the accuracy, power consumption, speed and area(Sun et al. 2008)(Nabavi & Lotfi 2006).

There is a few ADC architectures that were used to satisfy different requirements, such as Flash ADC, Pipelined ADC, Successive Approximation Register (SAR) ADC and Sigma-Delta ADC. The most popular ADC architecture is the Pipelined ADC for sampling rates up to 100 MSPS and resolutions from 8 bits to 14 bits. Pipelined ADC usually have multiple stages structure in which each stage only work on a few bits. Each stage of the Pipelined ADC performs an operation on the signal, provides the output for the following sampler, and begins the same operation on the next signal. Different stages process different samplers concurrently and throughput rate is depends on the speed of each stage(Leclare et al. 2003).

2.3 Amplifier Topology

Operational amplifier is one of the basic and must have circuits in analogue circuits. The increase of demand for high speed and high resolution applications such as ADC, result in an increasing demand for high speed and high gain amplifier(Mahmoudi & Dadashi 2012).

Folded cascode Op-Amp topology is combined of Cascode topology and Folded topology. Cascode topology is used to increase the gain of the input differential pair. Folded topology is used to improve the ICRM (Input Common-Mode Range) and also to reduce the require voltage supply. Folded cascode op-amp is considered as a single stage amplifier. Folded cascode circuit is shown in Figure 2.1 and Figure 2.2 below.

Folded cascode amplifier are also common choice for use in switch capacitor circuits in analogue to digital converter application(Scanlan 2006).

Folded cascode amplifier has gained popularity over telescopic because of it low voltage nature and future CMOS technologies, with the drawback of higher power budget(Assaad 2007)(Daoud et al. 2006). Furthermore, PMOS driven folded cascode amplifier has become the better choice for it low input common-mode level, higher non-dominant poles and lower flicker noise.

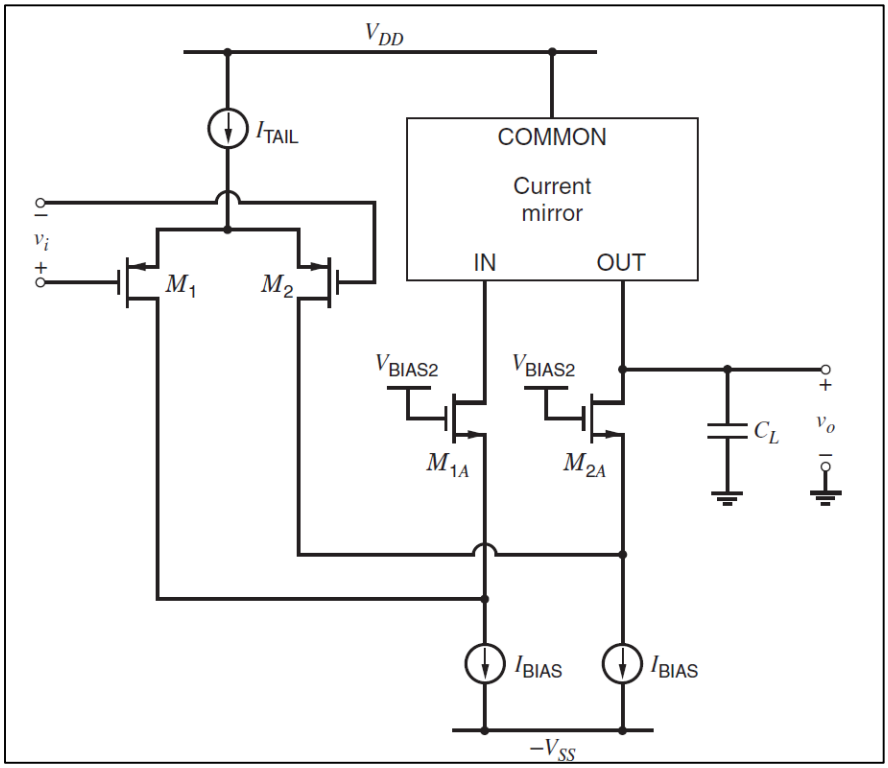

Figure 2.1: Simplified schematic of a folded cascode op-amp.

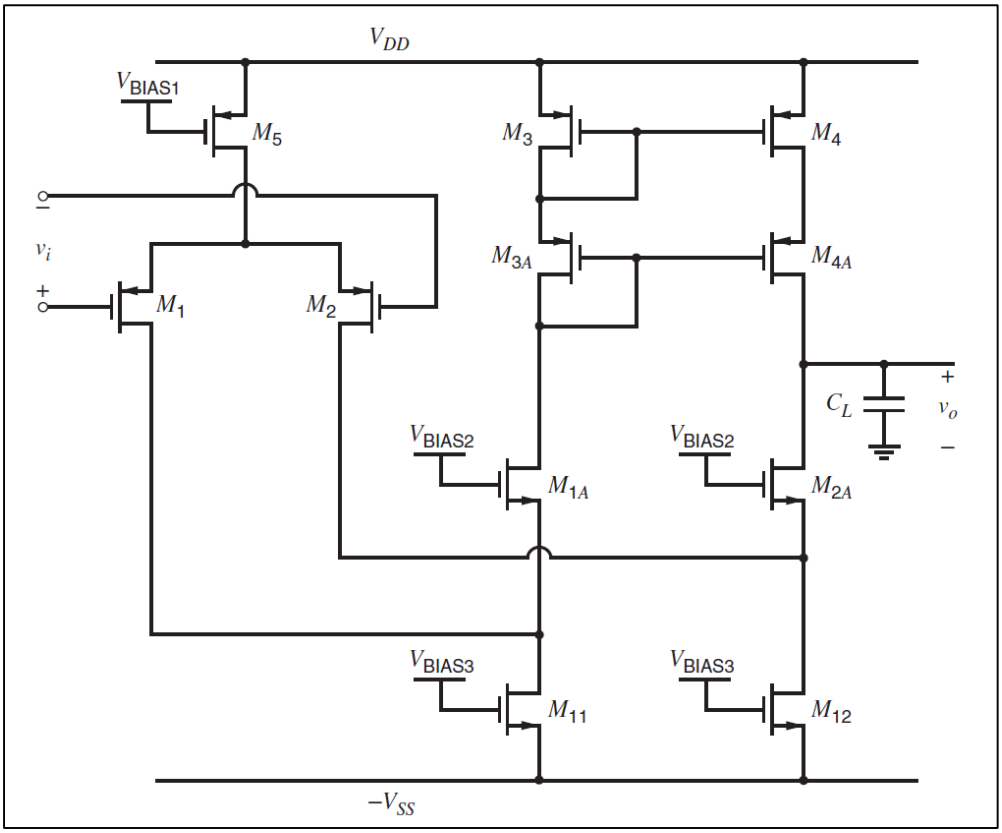

Figure 2.2: Detailed schematic of a folded cascode op-amp.

Transistors M_3 and M_{3A} are diode connected, then the voltage from V_{DD} to the gate of M_{4A} is $2|V_{tp}|+2|V_{0v}|$. Hence, source-drain voltage of M_4 is $|V_{tp}|+|V_{0v}|$. Maximum output voltage for both M_4 and M_{4A} are calculate using $V_{OUT(\max)} = V_{DD} - |V_{tp}| - 2|V_{0v}|$.

Since M_3, M_{3A}, M_4, and M_{4A} are all p-type, so the threshold voltage, V_{tp} can be eliminated from the equation.

$$V_{OUT(max)} = V_{DD} - 2|V_{0v}|$$

Then for minimum output voltage, assuming that M_{12} is active, drain-source voltage of M_{12} is V_{0V}.

$$V_{OUT(min)} = -V_{SS} + 2V_{0v}$$

At low frequency, the small-signal voltage gain of the folded cascode circuit in Figure 2.2 is $A_V = G_m R_0$, where G_m is the transconductance and R_0 is the output

resistance. The typical gain magnitudes can range from a few hundred to several thousand when all the transistors are operating in the active region(Gray et al. 1990).

Others criteria that use to measure an operational amplifier are common-mode rejection ratio, Power supply rejection ratio, slew rate and settling time(Daoud et al. 2008).

2.4 Common-mode Feedback Circuit

Common-mode feedback circuit is functioning in three operations, which is sensing the output common mode level, comparison with a reference, and returning the error to the amplifier's bias network. Common-mode feedback using two differential pairs, which is a circuit use only transistors is shown in Figure 2.3. From Figure 2.3, M_{21} and M_{24} are matched, same go to M_{22} and M_{23}. The source-coupled pairs, $M_{21} - M_{22}$ and $M_{23} - M_{24}$, sense the common mode output voltage and generate an output that is proportional to the difference between V_{oc} and V_{CM}(Gray et al. 1990).

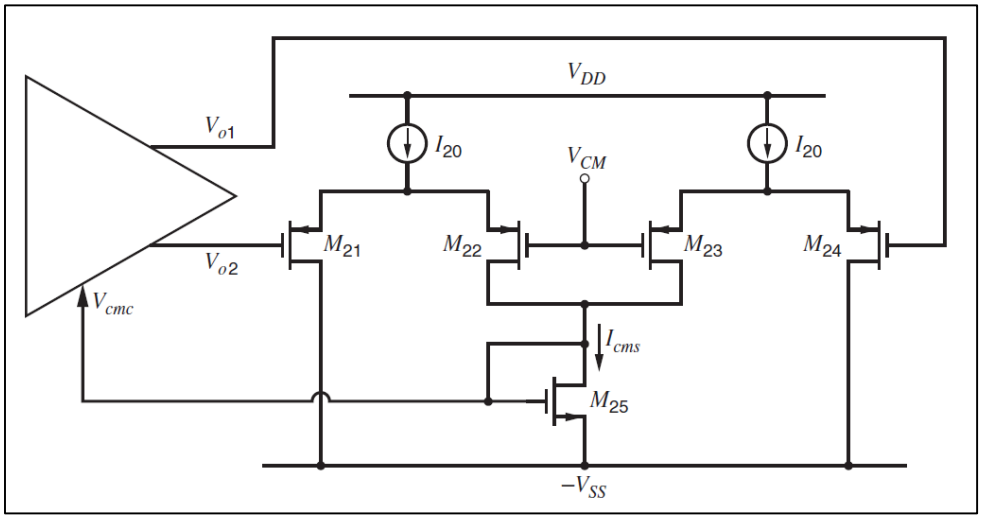

Figure 2.3: CMFB using two differential pairs.

Fully differential circuits use common-mode feedback circuit to operate accordingly. Common-mode feedback circuit is use for two reasons, which are to

control the common mode voltage at different nodes that cannot be stabilized by the negative differential feedback and to avoid the common mode components that tend to saturate different stages by applying common mode negative feedback. Common mode feedback is usually used as a reference voltage to get the maximum differential voltage gain and/or maximum output voltage swing (Razavi 2002; Gray et al. 1990). This kind of CMFB also been preferred over low power switch-capacitor CMFB because of better accuracy (Hati & Bhattacharyya 2011).

The main reason to implement this common-mode feedback circuit into this research is to overcome the mismatch of the current source. The common- mode feedback circuit will cancel the output common-mode current component, and to fix the dc outputs to the desired level.

2.5 1.5-bit Pipelined ADC

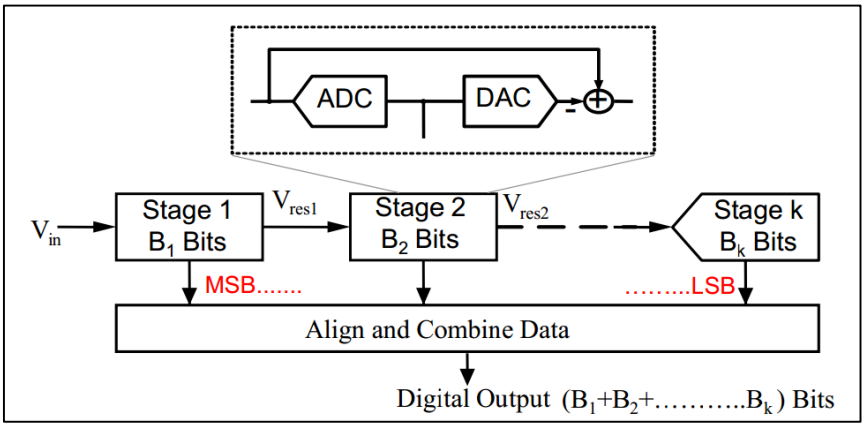

Figure 2.4: Block Diagram of a Pipelined ADC

As shown in Figure 2.4, the idea of a pipelined ADC is to cascade several low resolution stages to obtain high overall resolution result. For example, a 12 bit ADC can be built with series of 12 ADCs with each 1 bit only. Each stage performs course analogue-to-digital conversion and computes its quantization error.

Each stage is considered as low resolution ADC. Combining all low resolution ADC will form a high resolution of ADC that have more bits. Each stage only have 2 bits that represent the digital conversion, hence it is called the 1.5 bit Pipelined ADC(Neubauer et al. 2008).

Each stage analogue input, V_{in} is sampled and held by a sample and hold (S/H) circuit then the low bit ADC quantizes into 2 bits. Decision is made by comparing the value with one quarter of the reference voltage, V_{ref} in the quantization process. The resulted 2 bits quantized signal is then fed into the Digital-to-Analog converter (DAC). The signal is then being subtracted by the multiplied by 2 of held value. The output will then be the input of the next ADC stage(Agarwal 2009).

Table 2.1: 1.5-bit per stage pipelined ADC process information

V_{in}	B1	B0	DAC Output	Residue Output
$V_{in} > V_{ref/4}$	1	0	V_{ref}	$2V_{in} - V_{ref}$
$-V_{ref/4} < V_{in} < V_{ref/4}$	0	1	0	$2V_{in}$
$V_{in} < -V_{ref}$	0	0	$-V_{ref}$	$2V_{in} + V_{ref}$

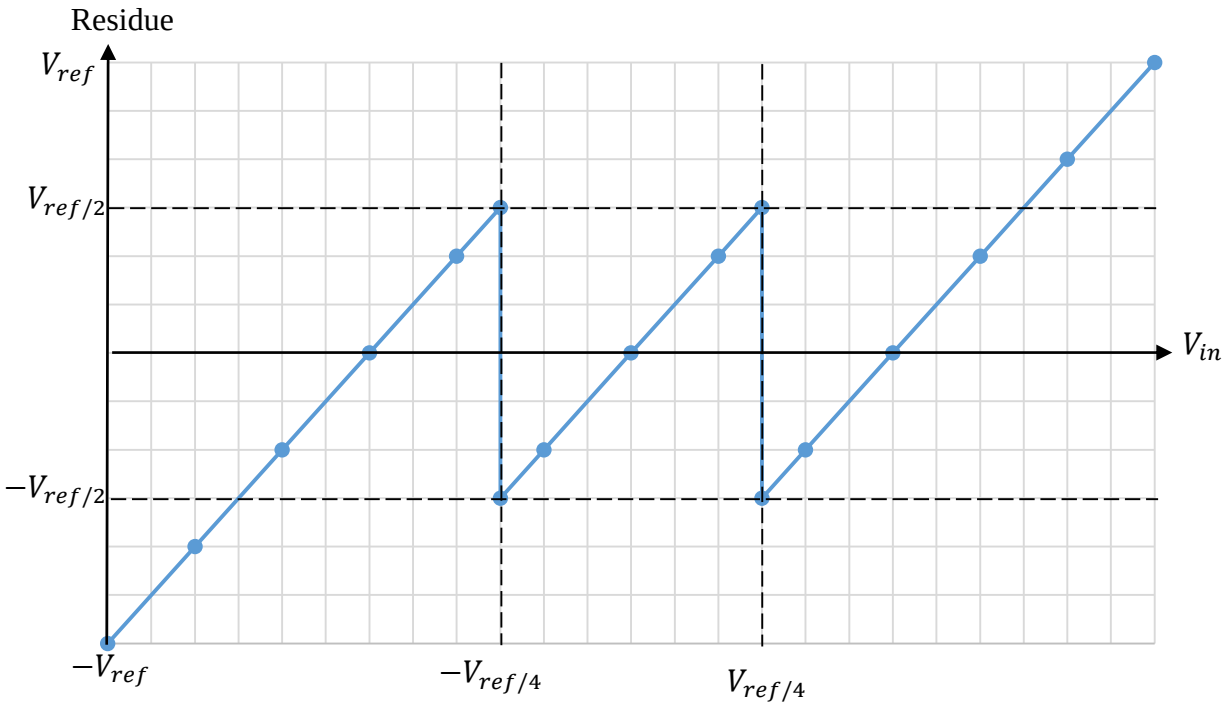

Figure 2.5: Transfer function of 1.5-bit per stage pipelined ADC

All stages are operate concurrently. The number of components needed grows linearly with the resolution. Because of each sample must propagate through the entire pipeline before all its associated bits are available for combining, data latency is expected. Pipelined ADC trades data latency for resolution(Measurement et al. 2000).

2.6 Multiply-by-two circuit

Sample-and-hold circuit is use to sample an analogue input signal and hold thee value over a certain amount of time for subsequent processing. By taking the advantages of the excellent properties of MOS capacitors and switches, switched capacitor techniques can be used to design the sample-and-hold circuit(Razavi 2002). To design the sample and hold architecture, the following steps is followed(Lailatul et al. 2012):

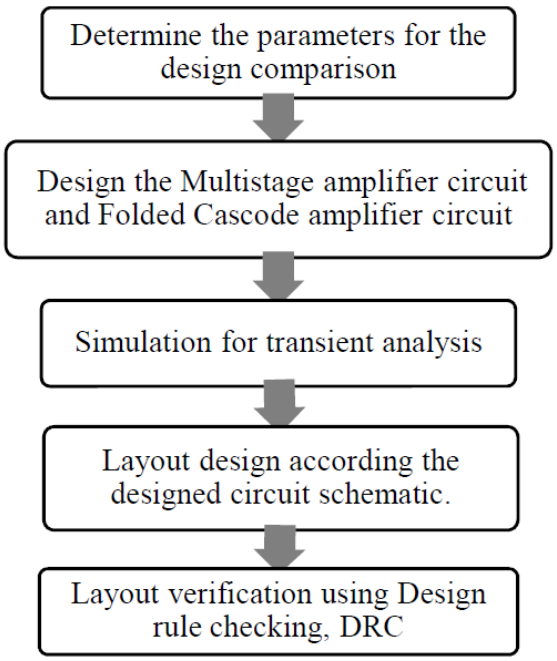

Figure 2.6 : Flow chart to design the sample and hold architecture(Lailatul et al. 2012).

In this research, precision multiply-by-two circuit is used to get a nominal gain of two while achieving a higher speed and lower gain error. The circuit is shown in Figure 2.7(a). To get the result of multiply by two, the amplifier incorporates two equal capacitors, $C_1$and C_2. During sampling mode, which is shown in Figure 2.7(b), C_1 and C_2 is charged while a virtual ground at X is established. Then, S_3 is turn off, followed by the turn on of S_1 and S_2. The total charge on C_1 and C_2 are equal to $2V_{in}C$, neglecting the charge injected by S_3. Then voltage across C_2 is approaching zero during amplification mode, the final voltage across C_1 and hence the output voltage are around $2V_{in}$, which is shown in Figure 2.7(c).

The charge injected by S_1 and S_2 and absorbed by S_4 and S_5 are not significant, compare to the charge that injected by S_3, which introduces a constant offset that can surpassed by differential operation.

The advantage of this circuit is the higher feedback factor for a given closed loop gain. However, the input capacitance of the multiply-by-two circuit in the sampling mode is higher (Razavi 2002).

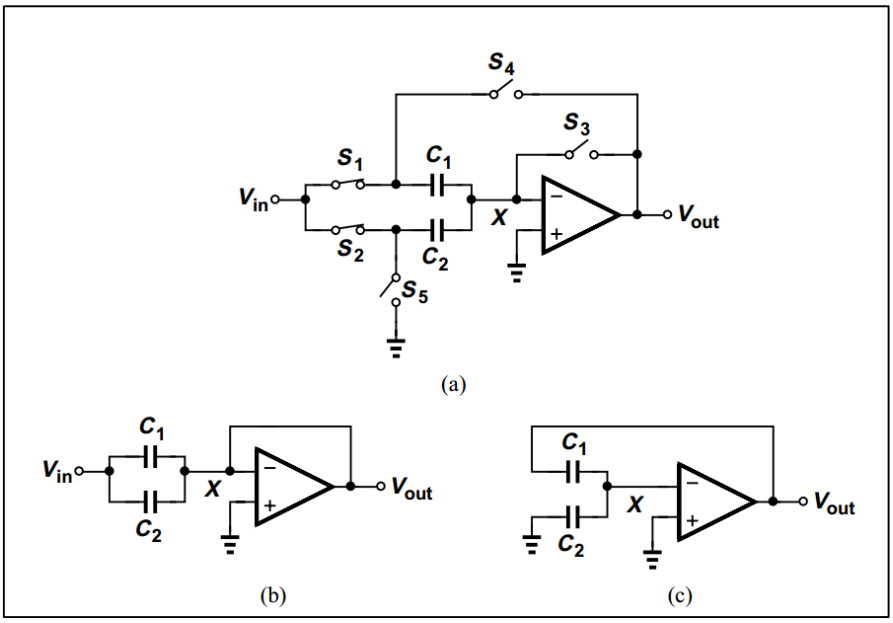

Figure 2.7: (a) Multiply-by-two circuit, (b) Circuit of (a) in sampling mode, (c) Circuit of (a) in amplification mode.

Process variation in fabrication of high speed, high resolution Analogue to Digital Converter is one of the biggest sources of accuracy degradation. For switch capacitor system, it cause mismatches between the fabricated capacitor and change the whole system's transfer function. Hence, it is very important when designing the multiply-by-two circuit to reduce the effect of mismatches(Zare-hoseinil et al. 2006)(Lu & Tung 2008)(Gama et al. 2009).

2.7 Parasitic capacitance

In electrical circuits, parasitic capacitance is common elements which is usually unwanted and unavoidable that exists between the part of electronic components or circuit (Gray et al. 1990). Parasitic capacitance in an amplifier may affect the amplifier

to have lower gain due to the parasitic loss (Silva-martinez & Carreto-castro 1996; Kim et al. 2008). While a MOS transistor is in saturation region, the gate-source capacitance C_{gs} and the gate-drain capacitance C_{gd} will have small amount of value. It can be calculated using

$$C_{gs} = \frac{2}{3}WLC_{ox} \text{ and } C_{gd} = 0$$

where C_{ox} is the oxide capacitance per unit area from gate to channel, W is the width and L is the channel length.

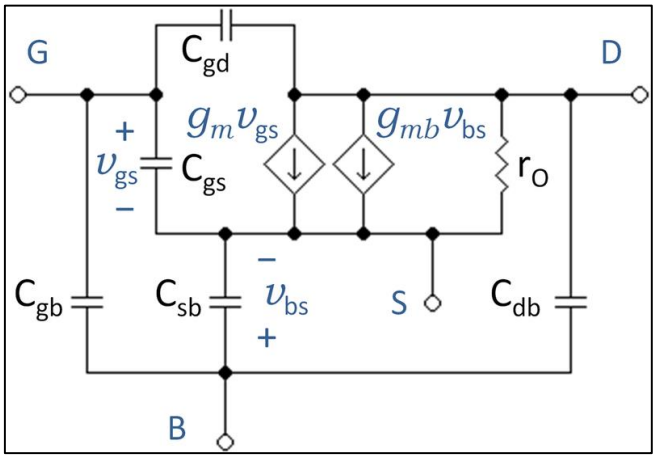

Figure 2.8: Small signal of a MOS transistor with parasitic capacitance.

From Figure 2.8, there is actually some parasitic capacitance in a MOS transistor which consist of gate-body capacitance C_{gb}, source-body capacitance C_{sb}, and drain-body capacitance C_{db}. Gate-body capacitance C_{gb} is usually depends on the oxide thickness of the MOS transistor. The oxide thickness of the MOS transistor with 100Å will have about 3.45f F per square micron of gate-body capacitance C_{gb}. The other two parasitic capacitances, source-body capacitance C_{sb} and drain-body capacitance C_{db}, can be calculated by assuming φ_0 to be constant.

$$C_{sb} = \frac{C_{sb0}}{\sqrt{\left(1 + \frac{V_{sb}}{\varphi_0}\right)}} \; and \; C_{db} = \frac{C_{db0}}{\sqrt{(1 + \frac{V_{db}}{\varphi_0})}}$$

CHAPTER 3

Methodology

3.1 Overview

This chapter will elaborate the design of the operational amplifier, common-mode feedback circuit, and the multiply-by-two circuit. Method to measure the characteristic of the operational amplifier is describe in this chapter. The design of the layout is covered in this chapter too.

3.2 Operational amplifier design

The requirement of the operational amplifier is to have average speed amplifier, low power consumption and high accuracy for sensor application. The design used the 0.13um Silterra process technology with voltage supply 1.2V to -1.2V which have 1MHz cut-off frequency. The open loop gain is 40dB, which is 100 in amplitude, DC gain and 1MHz cut-off frequency, therefore the gain bandwidth product is 100 x 1MHz = 100MHz.

To get the drain current flow to the PMOS transistor for the amplifier input, R_o must be determined first.

$$GBW = Gain\ of\ folded\ cascode \times Bandwidth$$

$$GBW = \frac{G_m R_o}{2\pi R_o C_L}$$

$$R_o = \frac{1}{2\pi \times 1M \times 50p}$$

$$R_o = 3.183k\Omega$$

Then, by using the value of R_o, G_m can be determined by

$$G_m = \frac{G}{R_o}$$

$$G_m = \frac{100}{3.183k}$$

$$G_m = 31.416m$$

Lastly, by applying the G_m value into the I_D equation.

$$I_D = \frac{G_m(V_{GS} - V_{TH})}{2}$$

$$I_D = \frac{31.416m \times (0.6 - 0.45)}{2}$$

$$I_D = 2.356mA$$

The summary of the specification of the operational amplifier is tabulated in Table 3.1. The step to design the operational amplifier is shown in Figure 3.1.

Table 3.1: Summary of specification of the Op-amp.

Gain	40dB
Cut-of-frequency	1MHz
G_m	31.416mS
I_D	2.356mA
VDD	1.2V
VSS	-1.2V

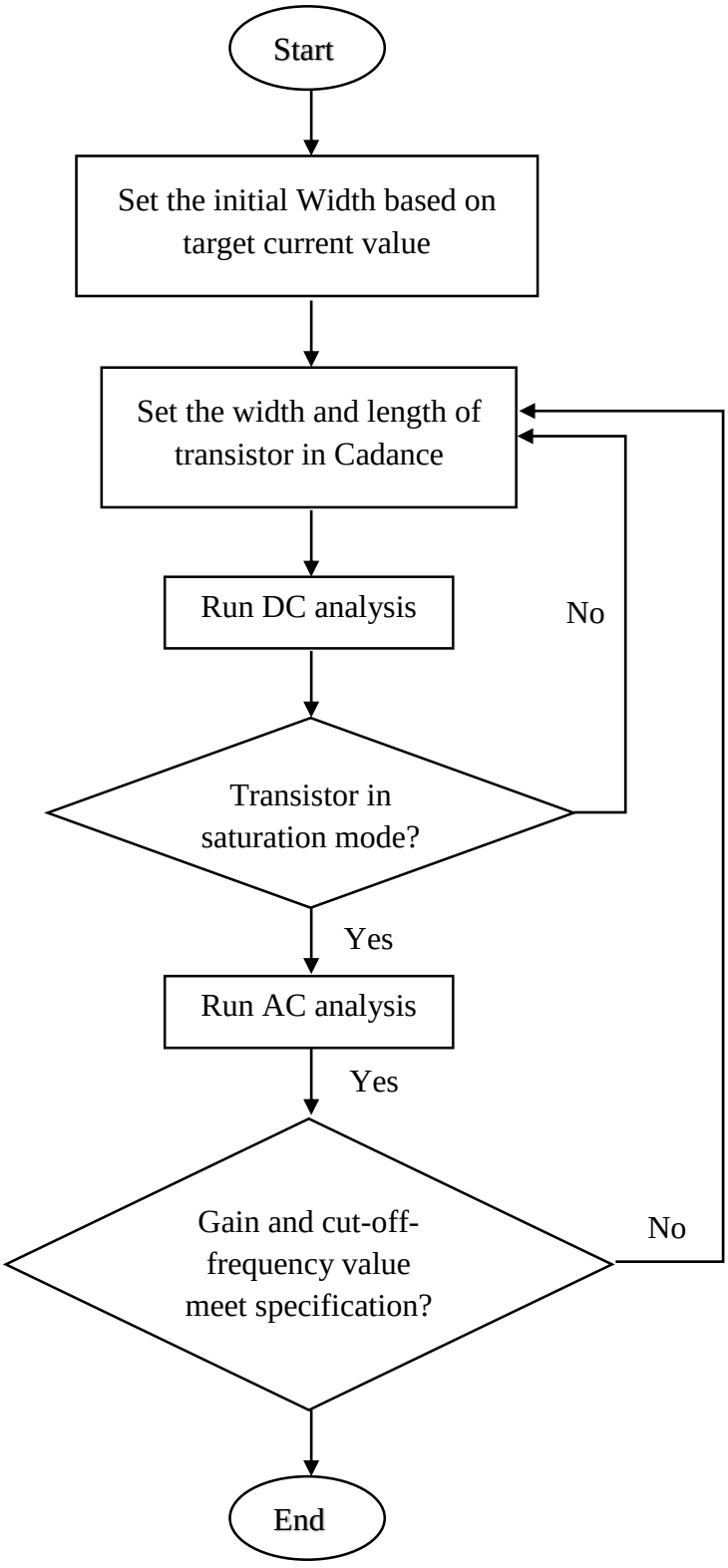

Figure 3.1 : Design flow of the operational amplifier.

3.3 Folded Cascode Op-amp

While designing an Op-amp, there are a few parameters to consider, which are gain, power dissipation, speed, linearity, supply voltage, voltage swings, input/output impedance and noise. Usually there will be trade-off between these parameters, improving one parameter will usually affect the other parameters as well. So it is very crucial while setting the requirement of the desired properties of the Op-amp.

Stacking all the other MOS transistors to complete the folded cascode circuit as shown in Figure 3.2. The folded cascade topology included two stages from the input until the output, which are common source stages and common gate stages. Transistors $M1$ and $M2$ in Figure 3.2 form the common source stage and transistors $M1A$, $M2A$, $M11$, and $M12$ form the common gate stages. Transistors $M3$, $M4$, $M3A$, and $M4A$ are the load which will be used to determine the output resistance which shown in Figure 3.1.

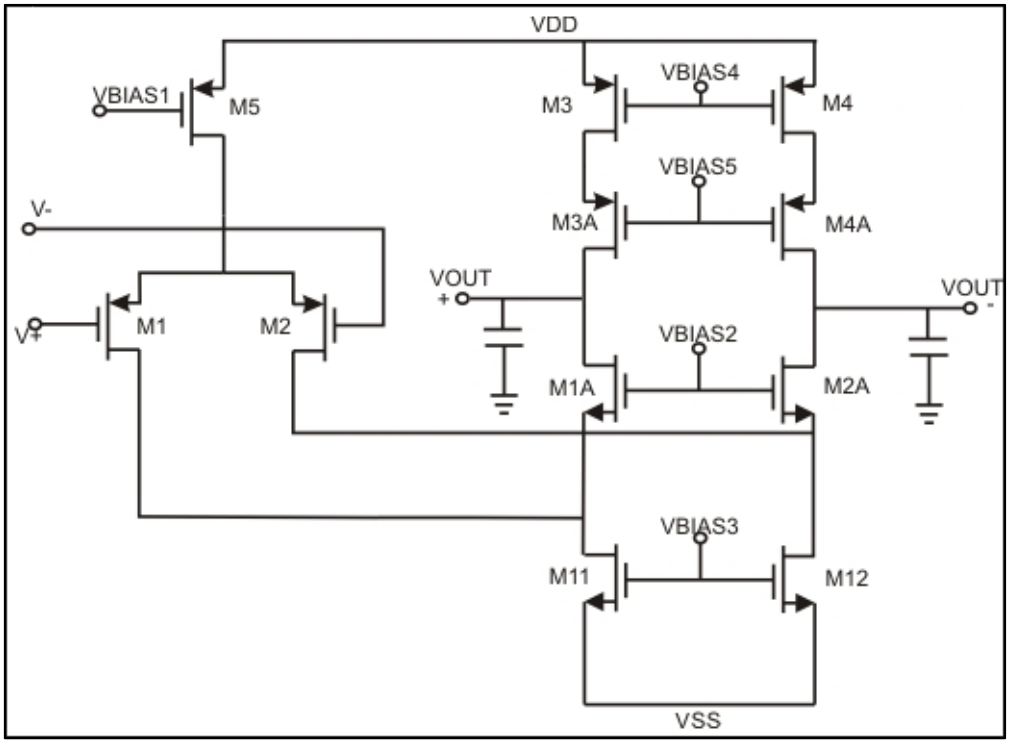

Figure 3.2: Foleded Cascode topology.

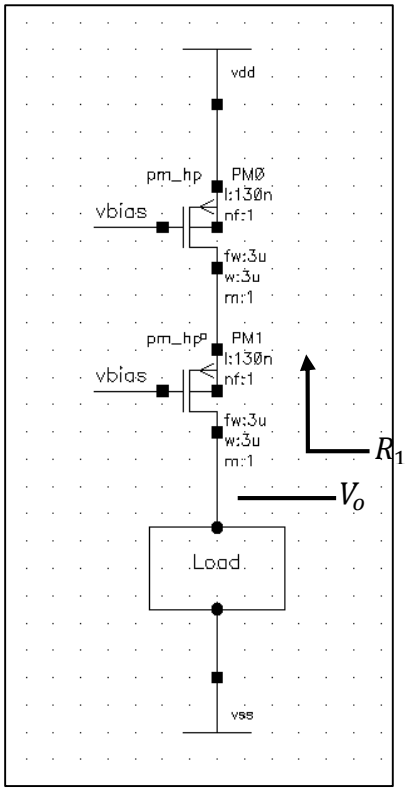

Figure 3.3: Cascode of MOS transistors.

The total output resistance of the cascoded transistors can be calculated by assuming the load of the NMOS is very high as shown in Figure 3.3.

$$R_o = R_1||\infty$$

$$R_o = R_1$$

$$R_1 = g_{PM1} r_{PM1} r_{PM0}$$

Hence, $R_o = g_{PM1} r_{PM1} r_{PM0}$

In real world, the load of transistors $M1A$, $M2A$, $M11$, and $M12$ which are not infinity, so the equation will need to be change to consider also those NMOS transistors.

V_{DD} is set to 1.2V and V_{SS} is set to -1.2V, and the common mode of the output voltage is designed to be at 0V. Two capacitors, C_L are place at both of the outputs for compensation. The reason of the compensation is to make the output node is the dominant pole with the desired magnitude. Since Folded cascode topology is a single-stage CMOS op amps, which Miller compensation cannot be used. So only option is to

add the load capacitor, C_L (Gray et al. 1990). All the transistors' gate are fed with different V_{bias} to achieve saturation mode.

3.4 Gain and Phase Margin of the amplifier

Gain and Phase margin is the very important characteristic of an amplifier. To test it, all the transistors in the amplifier must be in saturation mode(Mohd Fairus 2010). Then both inputs is fed with sinusoidal signal inversely which is shown in Figure 3.4. Then gain can be calculate after measuring both of the output using Eq. 1.

$$Gain = \frac{(output+) - (output-)}{(input+) - (input-)} \qquad Eq.\ 1$$

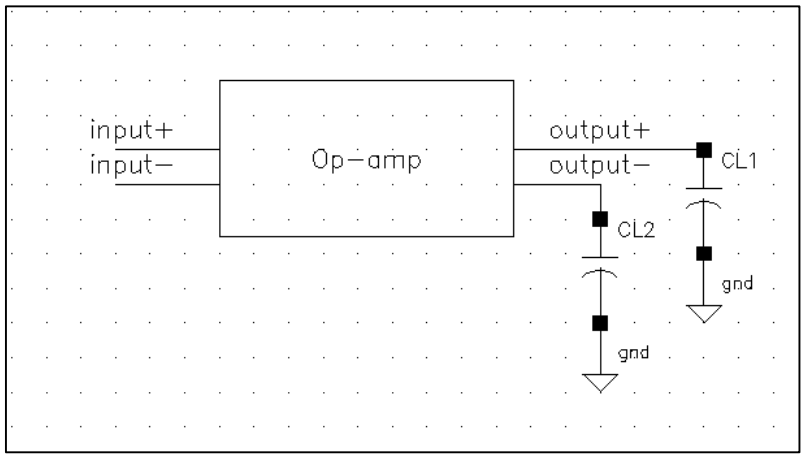

Figure 3.4: Amplifier gain measurement.

With the help of Cadance tools, Phase Margin can be measured. Phase margin for an amplifier is the difference between the phase shift of the amplifier and -180 degree. Phase margin must be positive so that the system is stable.

3.5 Common-mode Feedback circuit

Common-mode feedback circuit is design to make sure the common-mode of the output to be at 0V. The outputs of the amplifier is connected as the inputs of the

common-mode feedback circuit which are the gate of PM40 and PM41 respectively as shown in Figure 3.5. V_{ref} is properly set at a value so that it will set the common-mode of the amplifier to be at 0V. V_{cmc} source or gate will be connected to the gate of M11 and M12 of the amplifier in Figure 3.5 as the feedback.

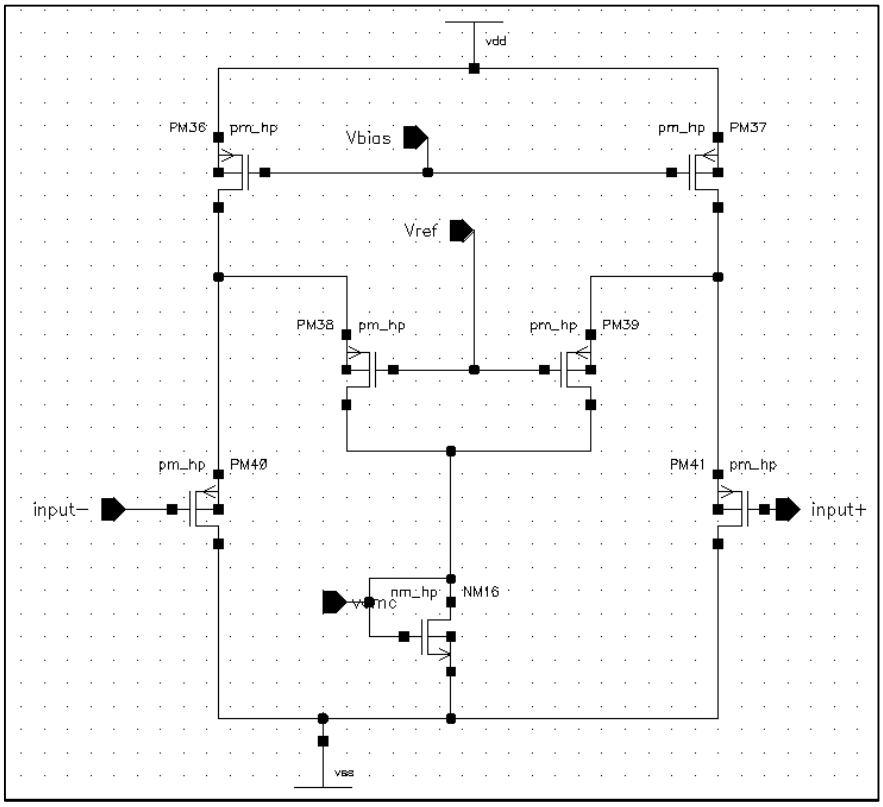

Figure 3.5: Common-mode Feedback circuit.

3.6 Characteristic of the Op-amp

There is four characteristic of the operational amplifier that will be measured in this project, which is common-mode rejection ratio (CMRR), power supply rejection ratio (PSRR), slew rate, and settling time.

For measuring common-mode rejection ratio, both of the inputs of the operational amplifier are connected to a DC voltage supply in series with a sinusoidal source as shown in Figure 3.6(Mohd Fairus 2010). CMRR then can be calculated by using

$$CMRR = dB20\left(\frac{V_{out}}{V_{in}}\right) \qquad \textit{Eq. 2}$$

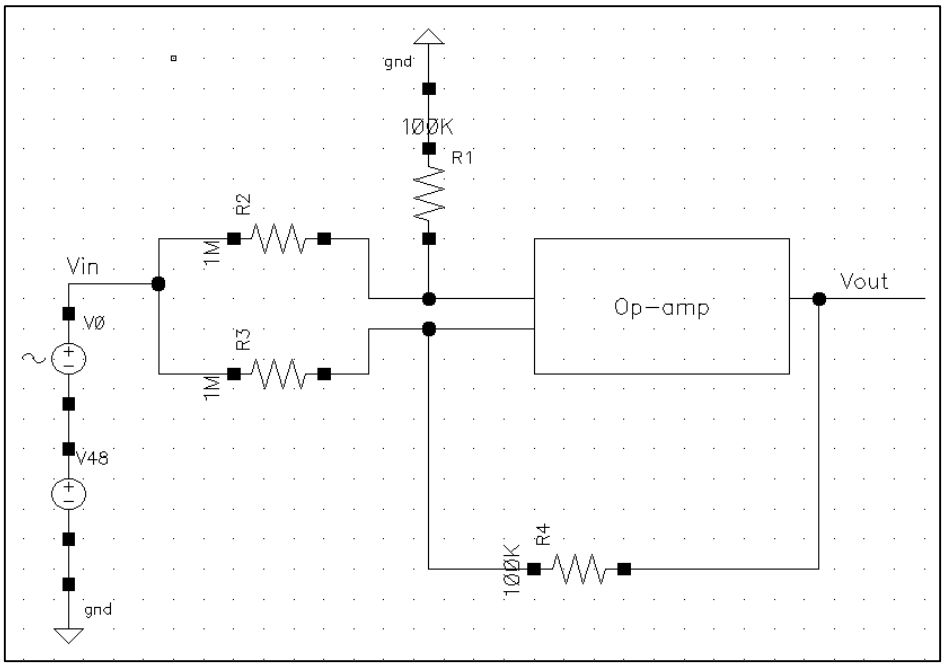

Figure 3.6: Test circuit for CMRR.

For measuring Power rejection ratio (PSRR), the input and the VDD of the operational amplifier need to be connected as shown in Figure 3.7(Mohd Fairus 2010). Then PSRR can be calculated by using

$$PSRR = dB20\left(\frac{V_{out}}{V_{dd}}\right) \qquad \textit{Eq. 3}$$

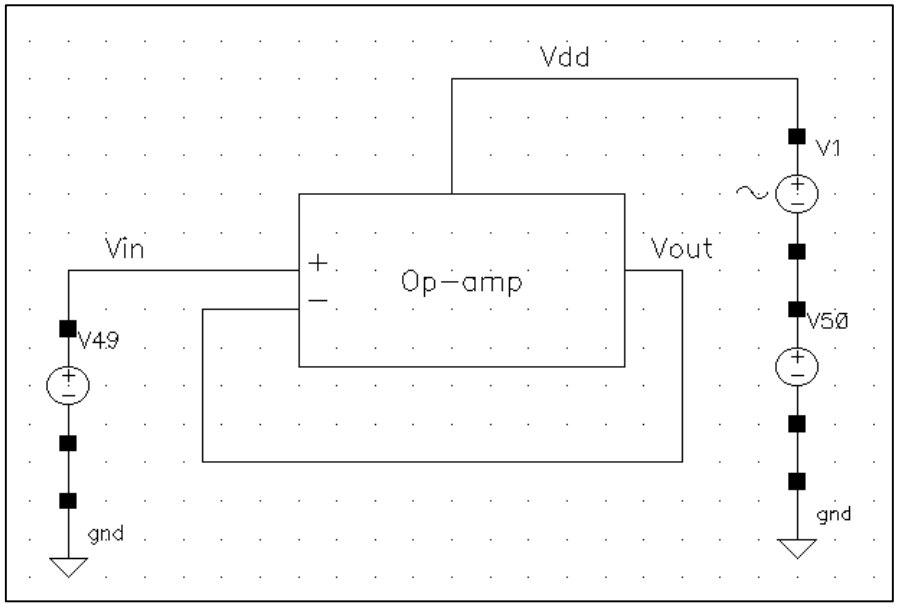

Figure 3.7 : Test circuit for PSRR.

To measure slew rate and settling, a same test circuit can be used but different input voltage supply will be used as shown in Figure 3.8(Mohd Fairus 2010). For testing slew rate, a step from 100mV to 1V is set as the voltage supply(Mohd Fairus 2010). For settling time, the voltage supply sill be only step from 500mV to 700mV.

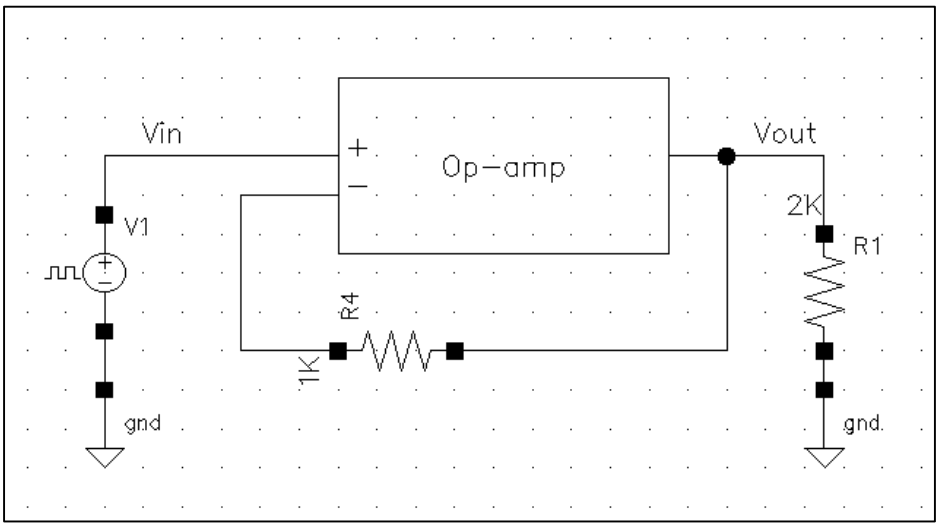

Figure 3.8 : Test circuit for Slew rate and Settling time.

3.7 Figure of Merit

Figure of merit is another way to evaluate the creditable of the design of the operational amplifier. According to Assaad and Silva-Martinez, figure of merit have two different ways to calculate(Assaad et al. 2009).

$$FOM_1 = \frac{GBW \times C_L}{Current\ consumption} \qquad Eq.\ 4$$

$$FOM_2 = \frac{Slew\ rate \times C_L}{Current\ consumption} \qquad Eq.\ 5$$

In this research, the focus is on the speed and the current consumption. So these figure of merit is being used to verify the proposed operational amplifier. The higher the value of FOM means the operational amplifier have a higher speed and lower current consumption.

3.8 Multiply-by-two circuit

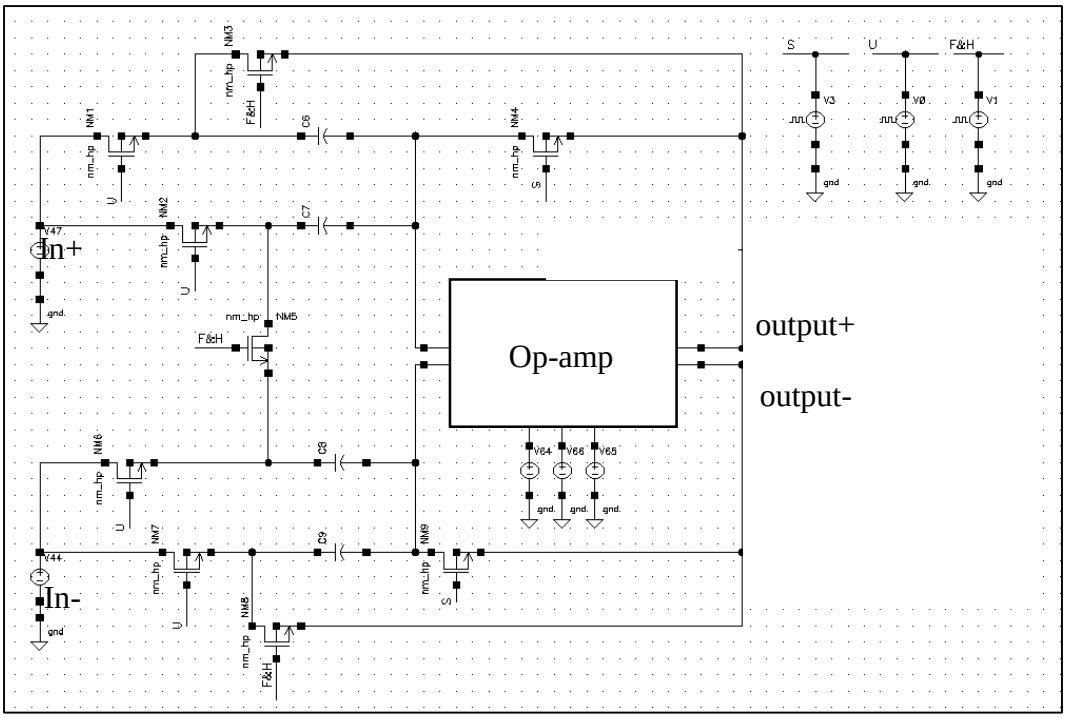

Figure 3.9 : Multiply-by-two circuit with op-amp.