OPTIMIZATION OF POTASSIUM HYDROXIDE (KOH) ETCHING ON THE FABRICATION OF P-TYPE SILICON NANOWIRE TRANSISTOR PATTERNED BY ATOMIC FORCE MICROSCOPY LITHOGRAPHY

by

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LIST OF ABBREVIATIONS

AFM	Atomic Force Microscopy
CVD	Chemical Vapor Deposition
DFM	Dynamic Force Microscopy
DIW	De-ionized Water
EDX	Energy disperse X-Ray
FESEM	Field-emission Scanning electron Microscopy
FIB	Focus Ion Beam
JLT	Juntion Less Transistor
LAO	Local Anodic Oxidation
RCA	Radio Corporation of America
SEM	Scanning Electron Microscopy
SOI	Silicon On Insulator
SPM	Scanning Probe Microscopy
SPA	Scanning Probe Analyzer
STM	Scanning Tunneling Microscopy
SiNW	Silicon Nanowire
SiNWT	Silicon Nanowire Transistor
TEM	Transmisssion Electron Microscopy
VLS	Vapor Liquid Solid

PENGOPTIMUMAN PUNARAN KALIUM HIDROKSIDA (KOH) TERHADAP FABRIKASI TRANSISTOR NANOWAYAR SILIKON JENIS-P DICORAKKAN DENGAN LITHOGRAFI MIKROSKOP DAYA ATOM

ABSTRAK

Transistor nanowayar silikon (SiNWT) telah berjaya difabrikasi dengan lihografi mikroskop daya atom (AFM) melalui proses punaran basah. Wafer silicon di atas insulator (SOI) <100> telah digunakan sebagai bahan asas. Sebelum digunakan, wafer dibersihkan dengan menggunakan ammonium hidroksida (NH_4OH), hidrogen peroksida (H_2O_2), asid nitrik (HNO_3), air dinyah-ion (DIW) serta asid hidroflorik (HF) untuk menyingkirkan bahan organik, bahan bukan organik dan lapisan teroksida daripada permukaan wafer. Mod AFM tanpa sentuh telah dipilih untuk proses AFM lithografi di atas wafer SOI yang telah dibersihkan. Struktur SiNWT telah direka dengan menggunakan pengaturcaraan raster. Konduktif tip AFM (Cr/Pt *cantilever tip*) telah digunakan untuk menghasilkan corak SiNWT di atas permukaan SOI berdasarkan struktur yang direka sebelumnya. Struktur yang dicorakkan (topeng oksida) telah dipunar melalui dua langkah proses punaran basah. Pertama, kalium hidrosksida (KOH) dan isopropil alkohol (IPA) digunakan sebagai larutan punaran untuk membuang lapisan silikon. Didapati bahawa larutan punaran 30 wt.% KOH + 10 vol.%, masa punaran 22 saat dan suhu larutan 65^{o}C memberi keputusan yang terbaik. Pada langkah kedua, HF yang dicairkan telah digunakan membuang topeng oksida untuk menghasilkan peranti SiNWT yang lengkap. SiNWT yang telah difabrikasi telah dicirikan menggunakan AFM, SEM, EDX, mikroskop laser 3-D, FIB-TEM dan penganalisis parameter semikonduktor. Daripada ciri arus-voltan, telah dapat dibuktikan bahawa peranti ini beroperasi sebagai SiNWT jenis-p.

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ABSTRACT

Silicon nanowire transistor (SiNWT) has been successfully fabricated by atomic force microscopy (AFM) lithography through wet etching process. The silicon on insulator (SOI) <100> wafer was used as a starting material. Prior to use, the SOI wafer was cleaned by using ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2), nitric acid (HNO_3) and Di-Ionize water (DIW) and diluted hydrofluoric acid (HF) to remove the organic, inorganic contaminants and native oxide from the wafer surface. A non-contact AFM mode was chosen to perform the AFM lithography process on pre-cleaned SOI wafer. The SiNWT structure was designed by using raster programming. A conductive AFM tip (Cr/Pt cantilever tip) was used to fabricate SiNWT patterns on the SOI surface based on pre-designed structures. The patterned structure (as oxide mask) was etched through two steps of wet etching processes. First, the potassium hydroxide (KOH) and isopropyl alcohol (IPA) were used as the etchant solution for silicon removing. It was found that etchant solution of 30 wt% KOH + 10 vol% IPA, etching time of 22 seconds and solution temperature of 65 ^{o}C as an optimum etching parameters. In the second step, diluted HF was used to remove oxide mask in order to produce a completed SiNWT device. The fabricated SiNWT was characterized by AFM, SEM, EDX, 3D laser microscope, FIB-TEM and semiconductor parameter analyzer. From current-voltage characteristics, it was proven that the device is working as a p-type SiNWT.

CHAPTER 1

INTRODUCTION

1.1 Background

It is well known that the fundamental building block for all electronic devices is *transistor*. Furthermore, the downscaling of this component has taken place for over the last half century in order to fulfill the market demand of various electronic products. Electronic is expected industry to continue in miniaturization of device hence make research works are ongoing. Many works are ongoing to ensure that these devices will have a better performance in terms of electrical properties, or even for the assurance of green environment.

Nowadays, most researchers are using complicated, high cost and not so environmental friendly approach techniques. Some of them tend to produce nano-scaled transistor in lab scale production, but they are still facing high cost operations and employing complicated methods. So far, a complicated approach had been used for fabricating these kind of devices that are more focused to top-down approaching. Recently most of them are focused on the electron beam lithography (EBL) (Hu *et. al*, 2004 and Hashim *et. al,* 2007), chemical vapor deposition (Yang *et. al,* 2010) and vapor-liquid-solid (VLS) (Lew *et. al,* 2003). Some of them rather used to combine these techniques such as low-pressure chemical vapor-deposition (LPCD) and AFM, reported by Choi *et. al* (2008). All of these involve high technology equipments which are not user-friendly, expensive, and are not so

green-technology-friendly. In addition, they are also involved with a combination of complicated techniques, critical parameters and hazardous chemicals.

1.2 Problem statement

The outcomes amazingly produce the electronic device with good results from previous studies. The existing studies, however, is based on the complex techniques, high cost and not so friendly green and users. No study to date has randomly assigned a simple technique, low cost and friendly user or even green technology to produce this nanostructure device. The study intends to fabricate and optimize the simple technique, low cost, friendly user and more green technology compared from above mentioned.

One of the most common and popular techniques to be compared for fabricating this transistor with nanowire is electron beam lithography (EBL) combined with reactive ion etching (RIE) which is the top-down approach. This technique is, however, too complicated, and involves high cost operation as well the use of hazardous chemicals. Hence, this system is far too expensive.

As reviewed by Hu *et. al* (2004) and Hashim *et. a*, (2007), the EBL process begins with the programming of the integrated circuit by using computer-aided design (CAD) program and transferring it to the EBL instrument. This instrument, which will function accordingly as programmed, will scan a beam of electrons direct to the surface of the substrate which is covered with the resistance. This technique can be used to produce features of different

sizes, shapes and scales very precisely, especially for nanometer scale design. The process will be followed by dry etching process, in which the material will be exposed to a bombardment of ions (usually by reactive gases such as fluorocarbon, boron trichloride) to the exposed surface where the contents of these gases are hazardous. This technique is applied to remove very small portions of substrate layer where predominantly vertical sides are desired. In semiconductor material, such as silicon, these processes will work effectively because of the highly reactive particles called radicals which will react with the substrate. This will result in the production of the new molecule which is energetically more favorable than the original bond. Subsequently, the new molecule is removed from the surface and etching process is achieved. Due to the unique ability of this technique, dry etching process will produce anisotropic etching that is very useful in the semiconductor fabrication process to create the high aspect ratio structures, such as capacitor trenches. The combination of EBL technique and RIE process is very promising. This technique involves many stages of process, or, it can be said as a layer-by-layer process to produce even the simplest circuitry. The substrate needs to have a resistant layer before it can be recorded by EBL and then followed by the RIE process. There are a lot of parameters that need to be considered, starting from the stage of layering the resistance which includes the type of resistance, spinning rate, spinning time and the desired thickness. Whilst the parameters, such as current applied, travel range and rapid exposure, need to be considered for the EBL process, however, the RIE process is even more complicated because the parameters need to be controlled in order to get very precisely desired structures.

In order to achieve cost reduction, a simple technique should be employed which involves only an average cost and is green-technology-friendly. Then, the mask less technique,

atomic force microscopy (AFM) lithography, is the answer to fabricate the simple nanowire transistor. This system is also more user-friendly and uses the available scanning probe microscopy (SPM) which is constructed together with the atomic force microscopy (AFM) lithography system. The non-contact mode of AFM will design the desired pattern on the surface via raster programming in the system. Then the pattern will further process for the achievement of the final product via etching step. J. Martinez *et. al* (2008) have demonstrated the microelectronic processes by employing and controlling the AFM parameters and the etching processes.

The etching process can be done through dry etching or wet etching method. However, the dry etching (reactive ion etching – RIE) method will produce hazardous gases such as silane (SiH_4) which are not green-friendly and they also will consist of high-cost operation. On the other hand, wet etching is a more efficient process in terms of cost and there is a wide selection of etchants which are either green-friendly or vice-versa. This etching process can have either anisotropic or isotropic effects on the samples but this depends on the application of the final product. Whether it is the dry etching or wet etching method being used, both processes need to be optimized in order to achieve the parameter effects on the nanostructures so as to produce an excellent quality of the final product. This is the critical issue which needs to be discussed in the preparation of nanostructures devices.

Since the RIE is a complex system and also expensive to be performed, the wet etching process will be used in this study in order to produce the final device. The beauty of this technique is the trend of the etched pattern, which is isotropic or anisotropic. This trend depends on the application of different etching solutions. This study will use anisotropic etchant to etch the circuitry structure which will give similar results as that obtained

through the use of RIE process. Here, the etchant solution used in this study is Potassium hydroxide (KOH) admixture with Isopropyl alcohol (IPA). By controlling the parameter such as the soaking time, ratio of etchant, additional of initiator and some related factors, it is possible to optimize the final nanostructure devices fabricate through this technique.

This study will involve the standard cleaning procedure for silicon substrate; followed by patterning the circuitry and the etching procedure through the use of wet etching process which will produce anisotropic pattern on the structure.

1.3 Research Objectives

The aim of this study is to achieve the following objectives:

1. To fabricate silicon nanowire transistor by using atomic force microscope (AFM) lithography and kalium hydroxide (KOH) etching process.
2. To optimize etching parameters on the fabrication of silicon nanowire transistor (SiNWT).
3. To characterize electrical properties of the fabricated SiNWT.

1.4 Research Scope

The scope of this study is the fabrication of silicon nanowire transistor through atomic force microscopy (AFM) lithography and followed by wet etching processes. The overall processes include silicon-on-insulator (SOI) wafer preparation, AFM lithography of design SiNWT structures on SOI, and two steps of etching processes. Pre-design SiNWT structures will be patterned by AFM lithography on SOI surface by controlling the voltage applied to the AFM tip, tip writing speed and the humidity. Patterned structures will be etched in KOH and IPA in order to remove the uncovered Si layer. SiNWT will be produced after being etched in HF solution so as to remove the oxide mask. The concentration of KOH and IPA etchants will be controlled so as to obtain the optimum condition.

The topography and morphology of the structures will be investigated by using AFM, 3D measuring laser microscope and field effect scanning electron microscope (FESEM). This FESEM is equipped with EDX spectrometer that is used to examine the elemental composition. Transmission electron microscopy (TEM) and AFM will also be used to determine the size and cross sectional observation of SiNWT. The Semiconductor parameter analyzer (SPA) will need to be used also in order to characterize the electrical properties using nanotech probe station.

CHAPTER 2

LITERATURE REVIEW

2.1 Nanostructured Materials

Nanostructure is described as objects between molecular and microscopic structures (Goddard III *et. al*., 2007). It is necessary to differentiate the dimension of the size in nanoscale. This nanoscale structure (such as atomic, molecular or macromolecular) lies between 1 to 100 nm along at least one dimension (NSF, U.S, 2000). In other words, it means that the entity has at least one nano-size functional component susceptible to make physical, chemical or biological properties or effects available uniquely. These are attributable to the nano-scale according to World Intellectual Property Organization (WIPO). Single nanostructure includes a single molecule, nanotube, quantum dot and nanowire (Goddard III *et al.*, 2007). These nanostructure properties, either physical or chemical properties, can differ significantly in the same composition of atomic-molecular or bulk material (Gogotsi, 2006). Whereas the ongoing miniaturization and the nanostructures are concerned, it will start from solving the dimension, at least within nanoscale.

The simplest form of nanostructures is *nanoparticles* which is considered zero-dimenional (0-D) nanoelement and usually known as *quantum dot*. At this dimension, these nanoparticles do not move freely moving but are at the confined states. This is followed by

the one-dimensional (1-D) nanoelement, which consists of particles travelling along the structures. This dimensional nanoelement is slightly complex in nature. The nanotube, nanorod and nanowire are included in this type of dimensional nanoelement. However, the two-dimensional (2-D) nanoelement is even more complex and it will confine the particles along the thin layer. These types of dimensional nanostructure are very useful for the construction of the nanodevices along with one-dimensional nanoelement. The nanoplatelet, nanodisk and quantum well are also included in this category. In addition, the three-dimensional (3-D) nanoelement will hold down the particles moving in all directions. The bulk material is also included in this category. Figure 2.1 shows the quantum confinement for all dimensions discussed above.

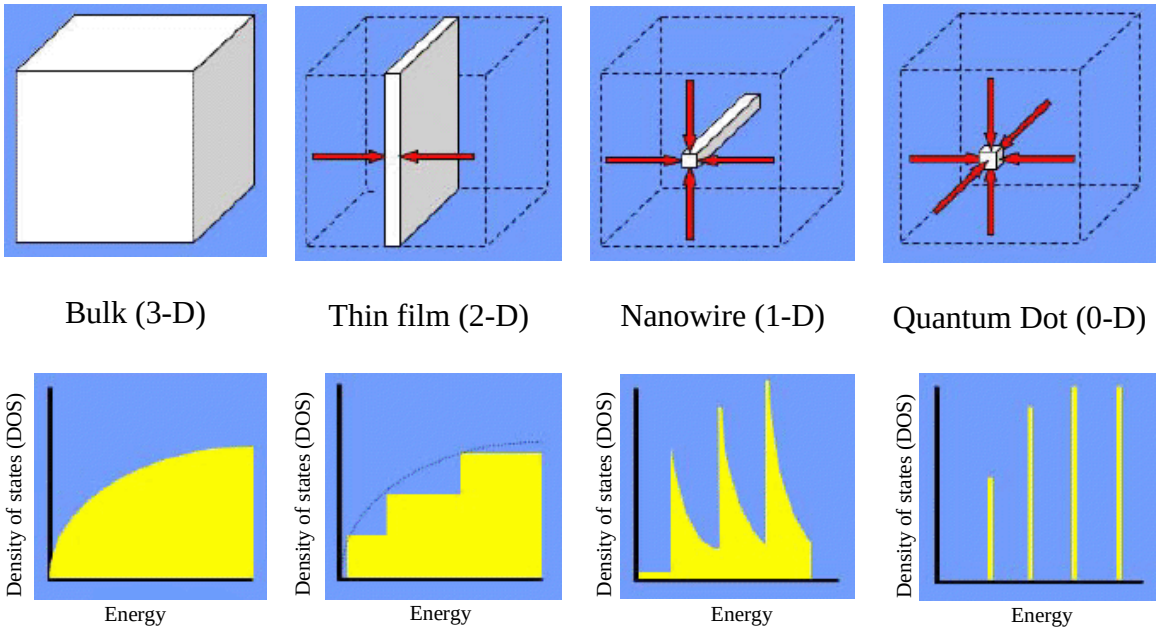

Figure 2.1: Quantum confinement (Hoogland, 2008)

The properties of nanostructures will change as the dimension changes and their functions also differ from one to another. The nanostructure interface and surface will decrease when

the length of the scale decreases. Generally for the bulk material, the energy contribution from the surfaces and interfaces are relatively very small, but they are usually ignored for the discussion of the energetic of the system (Hoogland, 2008). The decreasing of the size of these structures will increase the importance of this area. The behaviors of the materials are however influenced by the surface and interface energies and there are possibilities to measure quantitatively the increased surface area and its functionality by using a simple geometrical model. The reduction of the material size will enormously change the properties of that material compared to that exhibited in macro scale. The physical properties of bulk material are significantly different from the macro scale properties, and this is due to the reason discussed above. For example, aluminum will become combustible; solid gold will change its color and will turn into liquid form at a temperature of 500 degrees which is lower than its normal melting temperature, and copper will change from its opaque to a transparent form. In addition to these facts, it was discovered that silver, copper and aluminum also possess potent anti-bacterial properties. Besides these, there are other materials which have shown some interesting properties, For example, platinum will change from being inert to a catalyst form and aluminum, which is a stable material, will become combustible. Some of the materials discussed here will have more interesting properties if they are examined in nanoscales, for example, gold which is inert in normal scale will become a potential catalyst in nanoscale. Some properties of the materials are commonly known for their behavior under normal conditions, but there are plenty of possibilities to explore the potentiality of nanostructures. However, there are materials which are known for their nanostructure physical properties of that are related to

different origins; such as large surface energy, spatial confinement and reduced imperfection.

Nanostructures will have significantly different sensitivity in their reaction and their epitaxial growth from the bulk material. For example, there are many reviews in sensor applications which claim that there is a big difference of sensitivity between this type of structure and the bulk structure. Karl Skucha *et al*. (2010) had produced a review on SiNW with Palladium (Pd) contact in H_2 sensor. He was successful in achieving the sensitivity which is able to reliably detect H_2 concentration down to 5 ppm H_2 concentration; while the bulk sensor (diode based sensor) only have a sensitivity of 154 ppm H_2 concentration.

Besides that, optical properties of nanostructure are also significantly different from that of bulk crystals. This is due to an increase of the band gap which causes the optical absorption peak of semiconductor nanoparticles to shift to a short wavelength. Because of this reason, the color of metallic nanoparticles will also change in size due to the surface plasma resonance.

In general, the conductivity of a nanowire is expected to be much less than that of the bulk material (Gogotsi, 2006). This is due to the scattering of the wire boundaries. This phenomenon happens when the width of the wire is below than the free electron path. The nanowire is also strongly influenced by the edge effects. This effect is due to the atoms that lay at the nanowire surface and are not fully bonded to the neighboring atoms with the bulk of the nanowire. The unbounded atoms are often the source of defects within the nanowire, and this may cause the nanowire to conduct electricity more poorly than the bulk material. As a nanowire shrinks in size, the surface atoms will become more numerous compared to

the atoms within the nanowire, and the edge effects will become more important (Takayanagi, 2001). In certain cases, due to better ordering in nanostructure or microstructure, the electrical conductivity will also enhance appreciably. Whilst for the bulk material, the electrical conductivity will be reduced remarkably if the dimension is reduced in size due to the increased surface scattering (Takayanagi, 2001).

Huge surface energy is created in nanometer-scaled structure. In return, it is highly likely that superparamagnetism will occur. Whilst for the bulk material, ferromagnetism will disappear or transferred. This shows that the magnetic properties of nanostructures and the bulk material are distinctly different (Gogotsi, 2006).

2.2 Nanowires

Nanowire is a one-dimensional (1-D) structure which allows the particles to travel along the wire. This is a very attractive area of study in nanoscience because it has a wide range of nanotechnology applications. Until now, there are more than 17,000 articles and publications in science journals which discuss about this area of study. Nanowire is actually the nanostructure which has a diameter of less than 100nm. Alternatively, this nanowire can be defined as a structure that has the thickness or diameter constrained to tens of nanometer or less and unconstrained length (Skatssoon, 2006). This nanowire is the link component to the tiny small world in the near future of nanotechnology application. Nanowire has become important because it represents the smallest dimension for an efficient transportation of electron and exactions, and thus will be used as an

interconnection and as critical devices in naoelectronics and nano-optoelectronics (Lieber, 2007).

Nanowire has two quantum confined directions and one unconfined direction for electrical conduction. Due to this reason, it will require the electrical conduction to be used in the application. Nanowire also has a unique density of electronic states. If the nanowire has very small diameters, it will significantly exhibit the optical properties, electrical properties. However, the magnetic properties differ from that of the bulk material.

There are many types of nanowire and there are many publications which discuss about their properties and applications. Nanowire can be formed as a single crystal (Wu *et al*., 2004), polycrystalline (Jamaa *et al*., 2009), amorphous (Yan *et al*., 2000) or organic chains (Assad *et al*., 2008), or it can also be metallic (Dong *et al*., 2009), semiconducting (Chen *et al*., 2008) insulating (Zhang *et al*., 2009), or as molecular nanowire (Wu *et al*., 2004) which composes of repeating molecular organic or inorganic units. Each type of these forms has its unique properties, but the most inventively studied is the single crystal nanowire. This is due to its very unique properties in terms of electrical, optical, mechanical and magnetic properties. This single crystal nanowire grows along the specific axial direction, but its side surface may or may not be well defined. It can be round, hexagonal or polyhedron in shape according to the crystallography of the material when it comes to cross section. The length of the nanowire can vary from a few hundred nanometers to microns or sometimes to millimeters, but the thickness is always legibility small compared to its length. However, in some cases *nanorods* and *nanoneedles* are the terms used to describe the short nanowire with the length from tens to hundreds of nanometer.

In fact, nanoscale materials also exhibit a different behavior compared to bulk materials. Nanowires are structures of enormous surface area with respect ratios (length to diameter), and this contributes to its unique properties. In other words, nanowire has an increased surface area, more excitation binding energy and an increased surface scattering for for the electron and phonon. All these reasons will have good theoretical predictions on the quantum confined direction in nanowire which has good properties compared to the parent materials in bulk properties.

Nanowire has an advantage over bulk materials when it comes to its applications. It is because some parameters are more independently controlled in nanowires compared to that of bulk materials, such as thermal conductivity and electrical properties. By exploiting the singular aspects of one dimensional electronic density of state, it can be clearly observed that the properties of smaller diameter nanowire is relatively different in certain properties.

When it comes to fabrication and synthesizing the nanowire, there are two approaches that have to be considered, that is the bottom-up and top-down approaches. However, the top-down approach is more successfully used to fabricate or to synthesize nanowires (Bently *et al*., 2005; Lieber *et al*., 2007; Kim *et al*., 2008). The key parameters of single crystal nanowire can be obtained by controlling the growth time, growth temperature, chemical composition and much more (Liber *et al*., 2007; Kim *et al*. 2008). Findings of current researches on this technology revealed that the smaller and the smallest scales are being used in semiconductor, optoelectronics, electronics, and magnetic field and also in biochemical industries. It is definite that the global market for such nanomaterials will reach USD4.2 billion by 2011 (Gomez, 2009), and of course nanowire will be included in this research.

2.3 Nanowire Transistor

The electronics device which is beyond the reach of engineers in conventional ways was discussed in the year 2000 and above. In 2003, Lars Samuelson discussed in detail about this topic an article on materials today. In his article, he mentioned that the development technique of fabrication of the devices itself depends on the limitation of the current technological facilities. The crucial factors in device development are the extremely narrow rods or nanowires which are applied to the devices. The bottom-up techniques which is widely used in the self-assembly process enables the researcher control the accurate dimension, location, composition and other properties of nanowire. In certain ways, there is a limitation in the fabrication of complicated design structure so as to suit with the current needs. The materials that are still being used for the semiconductor base are such as Si and GaAs which were established almost fifty years ago. However, the top-down approach has to be relied upon for the formation of the basic fundamental block and the shaping of the device and circuits. The basic approach of top-down, such as conventional lithography, limits the dimensions of the device to what is technically achieved previously. During those days, this technique could create a kind of device features as narrow as 130 nm and now researchers are looking forward to see if this technology can pretty well draw the line-width down to ~50 nm. This limitation of dimensions encourages researchers to examine opportunities of reaching a target beyond this limitation as time passes through.

In the year 2006, it was reported by Li *et. al* regarding the growing demand and interest in nanoscale device that could enable new functions and greatly enhance performance, and open up the substantial opportunities for novel nanoscale photonic and electronic devices. One main focus in the review is nanowire transistor that could enable a diverse and exciting application in the future. In this review, it was revealed that the silicon nanowire-field effects transistor could be prepared. The evaluation of the performance level of this device has been made for the purpose of comparing it with corresponding planar devices. The SiNW-FET can be prepared with doped SiNW with the representative material such as Si, Ge and GeN with complementary of n- and p-type doped. The analysis result has demonstrated that the NW-FETs can exhibit a performance comparable to that of the planar devices made from the same materials. Figure 2.2 shows the results regarding this review published in Materials Today on October, 2006.

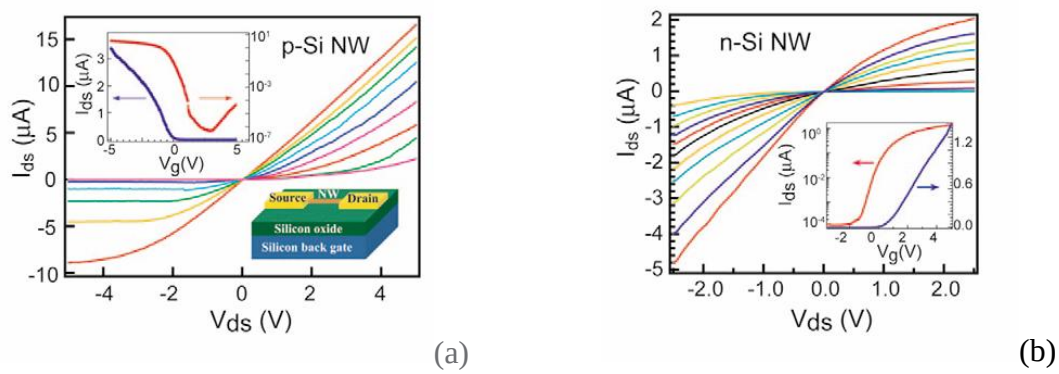

Figure 2.2: Si NWFETs: Family of current versus drain-source voltage (Ids-Vds) plots for a representative (Li *et. al*, 2006), (a) 20 nm p-Si NW array device (channel length of 1 μm; from red to pink, Vg = -5 V to 3 V) and (b) 20 nm n-Si NW device (channel length of 2 μm; from yellow to red, Vg = -5 V to 5 V) in a standard back-gated NWFET geometry as illustrated (Li Y. *et. al*., 2006).

2.4 Atomic Force Microscopy (AFM)

The revolution of the atomic resolution was documented in 1982 through development and invention of the scanning tunneling microscope (STM) by Binnig and Roher (Blanchard, 1996). This system is only limited for images and for measuring material surface morphology for good electrical conductor. In 1986, a study was conducted to develop the system which could have a broad application in the detection of atomic scale features on a wide range of insulating surface. This system was developed by Binnig, Quate and Gerber who named the system as *Atomic Force Microscope* (AFM).

AFM provides a number of advantages over the conventional microscopy techniques. This system can examine the sample surface and produce measurements in three dimensions, *x, y* and *z,* thereby enabling the measurement in three dimensional images of the sample surface. The resolution of the surface in direction *x-y* plane ranges from 0.1 to 1.0 nm and *z*-direction is 0.01 nm (atomic resolution). In addition, this system can either operate in a vacuum environment or for any special sample preparation, and can also be used in either an ambient or liquid environment. With these advantages, this system has a significantly impact on the fields of study of material science, chemistry, biology, physics and the specialized field of semiconductors.

The AFM non-contact mode is widely used in the scanning probe mode. This mode operates by rastering a sharp tip across the sample. It will be maintained by applying an extremely low force on the cantilever which is ~10^{-9}N (inter-atomic force range), thereby pushing the tip against the sample as it rasters. The repulsive force between the tip and the

sample, or the actual tip deflection, is recorded relatively to spatial variation and then converting it into an analogue image of the sample surface. The principal operation of the contact AFM mode is shown in Figure 2.3. The advances of AFM technology have led to a number of useful imaging modes, including the tapping mode and the lift mode AFM (Blanchard, 1996). These modes are useful for biological samples for the prevention of damage to the soft specimens The normal contact mode normally will be pushed out of the field of view by the rastering tip. The continuing development of AFM technology provides scientists with powerful tools that can be employed to characterize a variety of the sample surfaces. It is not just to characterize the sample surfaces in minimal sample preparation, but the recent market demands and the innovation technology has led to the development of AFM lithography, which is more adequate and cheaper than the lithography tool.

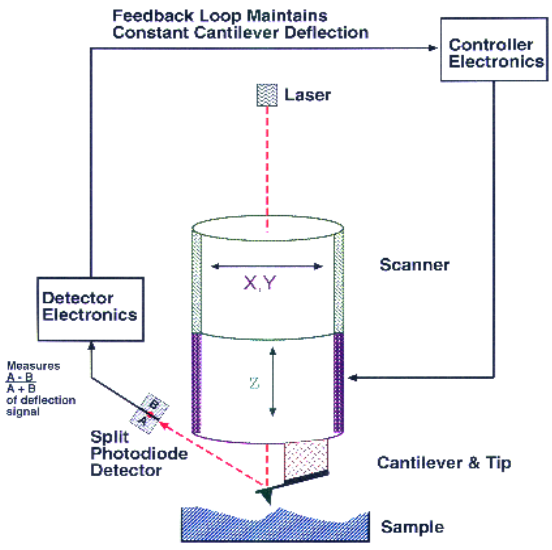

Figure 2.3: Schematic diagrams showing the operating principles of the AFM in the non-contact mode (Giessibl, 2003)

2.5 Preparation of Silicon Nanowires and Silicon Nanowire Transistor (SiNWT)

This reviewed is focused on fabrication and the way of synthesizing silicon nanowires. As mentioned earlier, there are many techniques that have been developed for this purpose through the years. Some of the developed techniques had been explored extensively, while others have attracted less attention and some are just based on trial and error. Whatever they are, the method of fabrication and the way of synthesizing nanowire employs either the top-down or bottom-up approaches while some other techniques will make use of the combination of these two approaches.

Basically, both techniques are strategies for the processing of information and the ordering of knowledge involving the software, humanistic and scientific theories through practice in order to build, fabricate or to synthesize the subject needed. In many cases of technical studies, the top-down approach involves analysis-making (or decomposition) while the bottom-up approach involves synthesis-making (Goddard III *et. al*, 2007).

The bottom-up approach is used more for the piecing together of the systems so as to give rise to grander systems. This technique is free in material choices and appears promising in the next generation of highly integrated circuit (Wan *et al.*, 2009). It is similar to the technique of making original subsystems of the emergent system where the system's individual base elements are specified in details. These individual sub-systems then will be linked up together to form larger systems, which sometimes involves the linking up of many levels until the completed top-level is formed. This approach resembles the 'seed' model which is begins with small elements. This is a simple technique and eventually

becomes more complex. It may result in a tangle of elements or subsystem and this will further develop an isolation system generating from organic strategies in subject to achieve the global purpose. In other words, this technique makes use of chemical properties of single molecules to utilize the concepts of molecular self-assembly and/or molecular recognition in order to synthesize the nanowire. The methods employed in this approach are solution growth, vapor-liquid-solid mechanism and thermal evaporation (Chen, 2007).

The top-down approach is also known as the step-wise design. In this approach, the system will eventually be broken down in order to gain an insight into the compositional sub-systems. The overview of the system is first formulated; specified but any first-level subsystem will not be examined in detail. Then each of the subsystem will be refined in greater detail, and sometimes in many additional subsystem levels as well. This detailed examination of the subsystems will be specified until the entire specification that is needed is reduced to the base elements. The model of top-down approach is often specified with the assistance of some software or 'brain' that makes it easier to manipulate the system. This technique has several advantages, such as it will separate the low level of work from the higher level abstractions and this will lead to the formation of a modular design which can be self-contained. This technique also has an illustrator code which shows the integration of the low level module. This will reduce the operation errors or will only cause fewer operation errors during the running of the system. This technique has many advantages. For example, it can reduce errors because each module has to be processed separately. Besides, it will give enough time for the programmers to perform the process separately. In other words, this technique will also optimize the way of processing because each programmer has to apply his or her own personal knowledge and experiences

to their modules. Therefore, only a part of the big project can be involved. This technique is also easy to maintain because it is easy to identify the errors if they occur in the output. This happens because each module is being run separately. However, this technique is a relatively new technique gives focus on ion beam (FIB), electron beam lithography, reactive ion etching (RIE), atomic force microscopy (dip-pen of AFM field evaporation) lithography and many others which have been perused in a few years (Pennelli, 2009; Wolfsteller *et al.*, 2010; Kuan-I Chen *et. al.*, 2011).

Table 2.1: Summaries of fabrication of SiNWT

Fabrication of SiNWT	
Bottom -Up	***Top-Down***
Vapor-liquid-solid mechanism and thermal evaporation, solution growth (eg. CVD) (Chen 2007)	EBL, FIB Lithography, LAO (AFM lithography), UV/ DUV lithography (Pennelli 2009, Wolfsteller *et al.* 2010, Kuan-I Chen *et. a.l* 2011)

2.5.1 Solution growth

As a review, the bottom-up approach is employed for the development of silicon nanowires. This approach also includes the chemical vapor deposition (CVD) technique. As reported by Hwang *et. al* (2000), the silicon nanowire is able to be grown on Si, SiO_2 and Si_3N_4 substrates by controlling the gas ratio. The growth mechanism of silicon nanowires was the cluster charged model (CCM), which is highly anisotropic and this can possibly be due to the Coulomb interactions between nanowire and the charged clusters.

Ansari *et. al* (2012) and Liber *et. al* (2007) also reported in a review that this approach necessitates nanoscale building blocks with precisely controlled and tunable chemical composition, structure, size and morphology, since these characteristics determine their corresponding physical properties. This technique is free in material choices. Wan *et al.* (2009) reported that this technique is applicable for the making of silicon nanowire (SiNWs) - related FETs. The large- scale high quality SiNWs are synthesized by CVD with metal catalyst and, subsequently, the grown SiNWs will then be transferred randomly on to the target substrate through the solution dispersing method. Next, the lithography is used to set metal wires as electrodes for FETs on the substrate, and this is followed by the process of annealing the contact and surface passivation on the nano devices in order to get higher carrier mobility. However, this technique cannot produce a high yield of FETs. In order to align the SiNWs on the target substrate, a flow-directed, Langmuir-Blodgett, dry-deposition, and electrical field technique has to be used. The single nanowire manipulation system is reported to be able to rearrange the nanowires which will improve the FET yield. Besides, the ordered growth SiNWs also helps to improve the yield of FETs. The SiNWs FETs fabrication technique is shown in Figure 2.4 and 2.5.

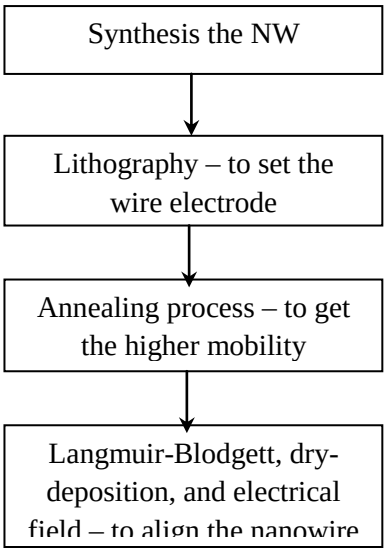

Figure 2.4: Flow chart the methodology of fabrication SiNW FETTs by using CVD technique

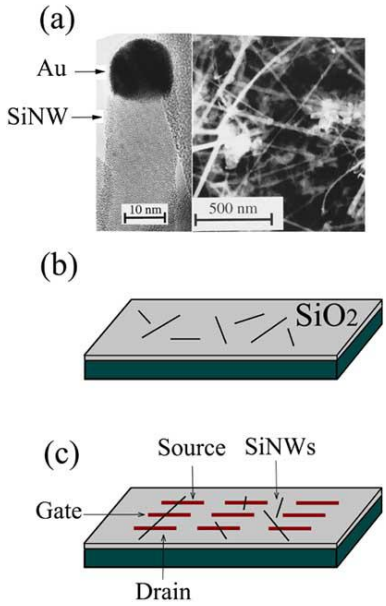

Figure 2.5: The "Bottom-up"technique for fabrication SiNWs FETs: (a) Left is a SiNW with gold catalyst particles, and right is the grown SiNWs by vapor-liquid-solid mechanism ; (b) transferring SiNWs to the target substrate; and (c) making electrodes with lithography on the substrate. Only the left FET works due to the difficulty to locate SiNWs and to make electrodes on the substrate. (Wan et al., 2009)

2.5.2 Electron Beam Lithography (EBL)

Electron beam lithography (EBL) is a well known technology and is commercially used as a technique for obtaining an ultra small scale design pattern for product application in nanoelectronics, nanophotocics and many others. This technology is very promising in the fabrication of this little tiny scale product because it has high throughput and high reproducibility. Many scientists are looking forward to do research on this technology due to the high demand from commercial manufacturers. A lot of discussions in the journals focus on the details the fabrication of nanoscaled size of transducer and devices in many applications.

According to Hu and his co-workers (2004), they managed to fabricate one-dimensional silicon nanowire transistor by using this fabrication technique. The one-dimensional silicon nanowire structures were fabricated in a p-type thin poly silicon substrate with 400 nm buried SiO_2. The nanowire structures were formed by electron-beam direct writing system (electron beam lithography system –EBL system) with electron-beam resist and etching by silicon dry etcher system. This technique consists of some complex processes that is the e-beam exposure, the pattern development, baking process and the etching process. Through these processes, Hu and his co-workers (2004) were successful in obtaining the one-dimensional neck-nanowire which varies from 20-72 nm by increasing e-beam dose from 9 to 13 mC/cm^2, and different designed gap and width of electrode pattern. Some of the results of this research were published and they are as shown in Figure 2.6.

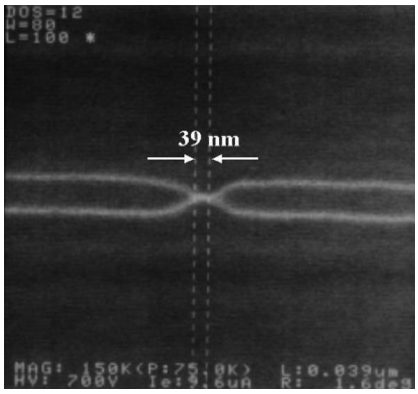

Fig. 2.6: Scanning electron micrograph of length of 39 nm silicon nanowire (Hu *et al.*,2004).

Jo *et. al.* (2010) also reported that they managed to fabricate the double-dot single electron in silicon nanowire. Jo *et. al.* (2010) fabricated the single electron transistors (SETs) on a SOI substrate by using the conventional Si-CMOS processes. From here, they made specially designed the Si nanowire (which has small constrictions at the end of the drain side of the wire) on the SOI substrate by using the electron-beam lithography and followed by dry etching. They were able to get the initial wire width of 44 nm, the length of 100 nm and the height corresponding to the thickness of the SOI layer which was 25 nm. By using pattern-dependent-oxidation (PADOX) method, they deposited a 50 nm thick Si gate over the pattern so as to complete the structure as shown in Figure 2.7.