Automated Tool to Generate Global Clock Distribution for Spine Structure

By

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List of Abbreviations and Nomenclature

Abbreviation	Meaning
IC	Integrated Circuit
SoC	System on Chip
IP	Intellectual Properties
OCV	On Chip Variation
CTS	Clock Tree Synthesis
HDL	Hardware Description Language
RTL	Register Transfer Logic
ICC	Integrated Circuit Compiler
STA	Static Timing Analysis
FC	Full Chip
ECO	Engineering Change Order
CAD	Computer Aided Design
APR	Auto Place and Route
PnR	Place and Route

Abstrak

Jam signal adalah isyarat yang mengawal dan menyegerakkan activiti-activiti logik serta activiti-activiti baca daripada/tulis kepada daftar-daftar dalam sesebuah litar segerak. Jadi, cara untuk mereka bentuk rangkaian pengedar signal Jam sentiasa dikeutamaan dalam reka bentuk litar bersepadu. Skim tulang belakang jam terkenal dengan kualiti isyarat yang diedarkan. Skim tersebut mempunyai prestasi yang baik jika dikajikan dari segi pencong, ketar dan OCV. Oleh itu, skim ini telah pun terjadi popular terutamanya litar berkelajuan tinggi seperti CPU. Walau bagaimanapun, skim tulang belakang jam ini tidak biasa digunakan dalam SoC. Hal ini adalah kerana kesulitan untuk mereka bentuk dan juga kerumitan dalam mengesahkan prestasi skim ini. Banyak alat-alat reka bentuk bagi SoC tidak menyokong skim tersebut sehingga hari ini. Jadi metodologi untuk memperkenalkan and mengintegrasikan skim tulang belakang jam serta membuktikan qualiti signal yang diedarkan akan dibincangkan di dalam tesis ini. Perbincangan termasuklah pengetahuan dan automasi metodologi yang boleh mengurangkan kerumitan mereka bentuk skim tulang belakang jam.

Abstract

Clock is a signal which synchronizes the logic as well as register read/write activities of a synchronous circuitry. Therefore a good way to design a reliable clock distributor network is always the top priority in IC design. Clock spine is well known for the robustness in clock signal quality delivered. Spine structure had shown good performance in terms of skew, jitter and OCV. Thus this scheme is popular for the high speed circuitry such as CPU chipset design. However, the clock spine is not commonly employed in SoC, due to the design as well as the validation complexity of this scheme. Many SoC design toolsets do not support this scheme up until now. So in this thesis, an automated methodology will be introduced and proven to integrate clock spine into a SoC to distribute a high frequency clock signal. These include the know-how and automation of the methodologies to minimize the complexity of designing the clock spine.

CHAPTER 1

INTRODUCTION

1.1 Overview

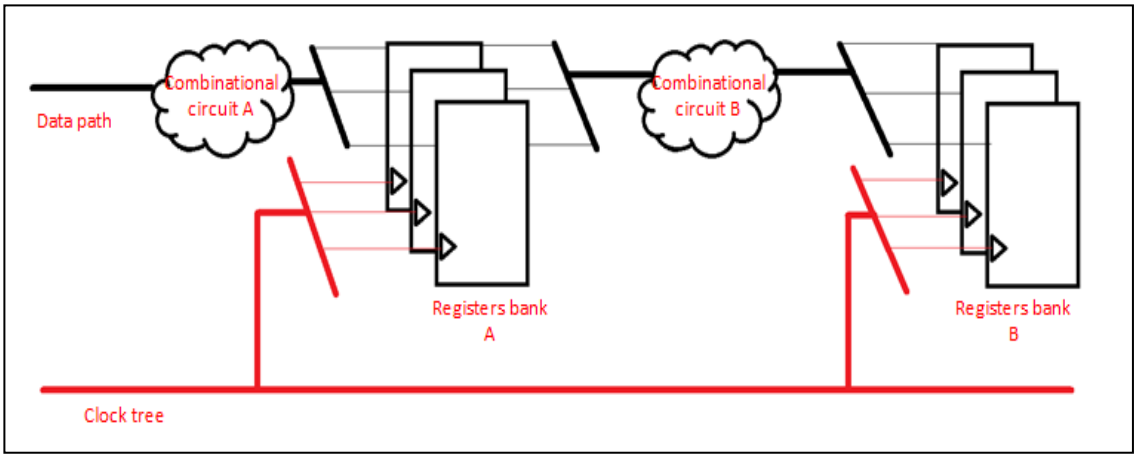

Figure 1.1 Typical Synchronous Circuits

As shown in Figure 1.1, this is a typical synchronous circuit. Combinational circuits are a group of functional or computational combination of logic gates, such as adder. In between the combinational circuits, there will be a registers bank. The registers are flip-flops employed to hold the computed data.

Usually the flip-flops used will be of edge triggered flip-flops. When the clock signals is in transition from low to high, the registers load in bits output from the combinational circuit. Then the data get transferred to the next stage. At clock signal transition from low to high, the data computed in Combinational circuit A will write into Register bank A. Then the data in Register bank A will get populated to Combinational circuit B.

The Combinational Circuit B will calculate the output. By the next low to high transition, the output will be written into Register bank B. And at the same time, the content in the Register bank A will be overwritten by a new set of data computed by Combinational Circuit A.

Clock signals in IC design world are square wave signals, toggling between two states namely high and low. There are several clocking signals oscillating at different frequencies and driving different partitions in practical chip design. The full chip is partitioned based on functionality and operating frequencies.

From the example explained in previous text, the clock is ultra-vital in term of the chip's functionality. The quality of the clock signals distributed to the registers will directly cause an impact to the chip's functionality and even may cause the design to be malfunction. Nowadays, whenever a new project to design a new chip started, the clock distribution networks were to be redesigned again. So a very significant design effort

was channeled to make sure the clock distribution networks delivered good quality clock signals.

In SoC design, some IP is getting reused. Take the multicore processor as an example, the similar core is duplicated and integrated as a duo-core or quad-core processor. Yet these cores are run by the same frequency clock signals. Thus, a global distribution network is needed to distribute the clock signal to these cores. Binary tree for example is employed to serve as a global clock distribution network. The clock designer needs to re-synthesize the clock tree taking various clock quality issues such as clock skew into consideration. The clock tree is synthesized by process called Clock Tree Synthesis (CTS) with the aid of Computer Aided Design (CAD) toolsets. Tree populated by CTS is however sensitive to On Chip Variation (OCV) problem.

For high speed circuitry such as CPU, another scheme named clock spine is commonly used. Clock spine is well known to have better skew, jitter and OCV performance against other kind of distribution network schemes. However, this structure is not supported by the SoC design toolsets and thus designers need to manually do the place and route task. The manual work is very time consuming.

To be competent in the time-to-market, IC design companies wish to market the product in a fast and qualified manner. In this thesis, a new tool or approach to automate the clock spine place and route work will be discussed. The proposed solution is able to

reduce the timely effort if the clock designer chose to use a spine as the global clock distribution network.

1.2 Problem Statements

SoC is getting popular among IC design industries. In the SoC design, clock signals are important to synchronize the chip's logic activities. Without a high quality clock signals, the chip might not able to function as expected. Computation errors will lead to malfunction of the design. The major error sources for a clock signal are clock skew and jitter.

Clock spine had been commonly used in high speed circuitry design such as CPU. It provides great quality of results in skew and jitter reduction. But it has not been commonly used in a SoC design. The clock spine is not yet supported by many SoC design toolsets up until now. The clock spine needs to be placed and routed manually. The manual work consumes a great amount of design effort. The parasitic RC of the spine needs to be extracted for timing quality verification.

Therefore, in this thesis, a methodology and apparatus will be introduced and proven to integrate clock spine into a SoC to distribute a high frequency clock signal. These include the know-how and automation of the methodologies to minimize the complexity of the clock spine.

1.3 Aim and Objectives

The aim of the research is to design, implement, and evaluate a new methodology and apparatus of a clock spine distribution network in a SoC. To realize this aim, the following objectives are adopted:

i. To prove the concept of automating the clock spine generation as a global clock network in IC design.

ii. To evaluate the performance of the automated generated clock spines versus CTS tree in term of the signal quality.

1.4 Research Methodology

Overall, the research's methodology is divided mainly into three phases.

i. Literature review: The literature starts by reviewing the basic concept of clock signals. This includes the fundamentals to understand the source of errors to the clock signals. Various clock schemes used in existing IC design industry will be introduced in brief. The limitation of designing clock tree by CTS as well as designing clock spine with manual effort will be discussed.

ii. Design and Implementation: A Perl script is used to generate the netlist files and TCL placement command file for the clock spine. Using Auto Place and Route (APR) in Synopsys ICC tool, the spine's layout would be generated. The parasitic RC of the Spine clock will be simulated with using SPICE.

iii. Evaluation, Benchmarking, and Case study: The clock spine simulated result would be compared to the Clock Tree Synthesis (CTS) result. The spine performance will be benchmarked with the CTS result.

1.5 Thesis Organization

This thesis is organized into five chapters. The rest of the thesis is organized as follows. Chapter 2 elaborates the key parameters and design specifications of a clock distribution design and the state-of-the-art for the clock distribution schemes in SoC industry. In the end of the chapter, the key problem statement and interest of the thesis will be explained.

Chapter 3 outlines the design flow and implementation of clock distribution network design. This includes the SoC industry commonly used toolset for CTS, ordinary way of populating a clock spine network as well as the proposed automated way to generate the clock spine network.

Chapter 4 compares the quality of results for both clock spine and CTS tree (as elaborated in Chapter 3). Benchmarking of both clock schemes will be elaborated and discussed in details.

Finally, in Chapter 5, the conclusions of the research are presented as well as the findings and contributions of the research are highlighted clearly. In addition, the chapter highlights the possible future works as a continuation of this work.

CHAPTER 2

LITERATURE REVIEW

In this chapter, the basic concepts of clock design in Integrated Circuit (IC), particularly SoC will be discussed. These include the elaboration of the primary design requirements and interests of a clock signal. Different clock schemes available in the industry and their advantages and disadvantages will be discussed.

2.1 Introduction to Clock in Synchronous System

All signals are expected to propagate and update all the memory elements within the expected time frame in a fully functional sequential circuit. Therefore, the idea of synchronous system is introduced to achieve that. In the synchronous system, all the signal propagation activities will be overseen by “clock”. The clock is actually a periodic signal distributed globally to synchronize the signal propagation.

The clock signal window will synchronize the fast signals and slow signals in order to make sure all the logic states are updated at the same time instance. This is vital to

ensure the intended logic result is correctly computed. In other word, the system fastest clock frequency will be dependent on the slowest signal.

The clock signal performance is judged by the clock frequency, uncertainty, and usage overhead. All mentioned factors will determine the functionality and performance of a synchronous system (Rusu, 2001). The frequency of the clock determines how frequent the logic states in the design could be updated within a second. This means that the higher the clock frequencies, the faster system computation ability. And since the clock will directly affect the performance of the whole system, the clock is usually imposed by strict timing constraints. If the clock signals do not comply with the timing constraints imposed, the memory elements could get wrong data updated and thus lead to malfunction (Rabaey, Anantha & Nikolic, 2003).

2.1.1 Transition Time

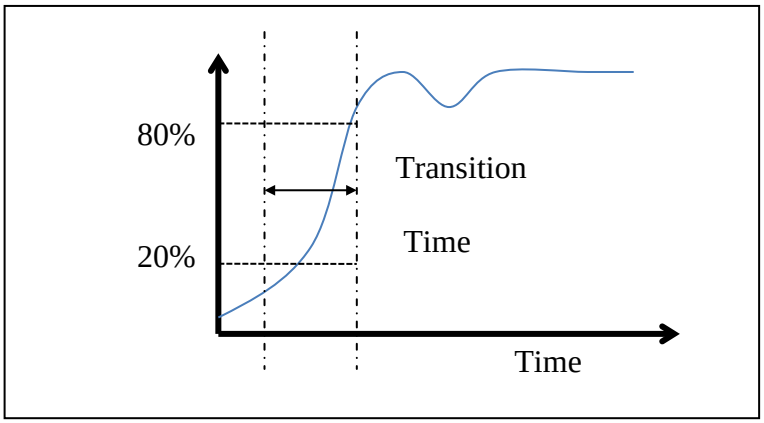

Figure 2.1.1 Illustration of Transition Time

Transition time is refers to as a period of time used for a signal to change from the original logic state to another logic state. In this thesis, the transition is mainly focus on the clock signal. Thus the transition time could be low-to-high (0 to 1 transition) or vice versa. The most common used way is to take the time period starting from 20% of VCC to 80% of VCC for the rising edge; and similar 80% to 20% for the falling edge (Rusu, 2001).

Transition time is very important to clocking signals. This is one of the main factors that limit the maximum frequency the clock signal can go (Wong, 2002). Besides, transition time of the clock signal also determine the total power consumption and radiation interference (Rabaey, Anantha & Nikolic, 2003). Slow transition time suppresses the clock maximum frequency; Fast transition time consumes more power for the sake of

faster respond and could introduce crosstalk to nearby signals thus affect the signal integrity.

2.1.2 Duty Cycle

Duty Cycle is the ratio of the positive pulse period over the entire clock period. For example if the clock signal is having the exact equal time for the high and low, the duty cycle will be 0.5 or 50%.

$$Duty\ Cycle = \frac{T_{+VE}}{Total\ Period} \ldots\ldots\ldots (Eqn\ 2.1.2)$$

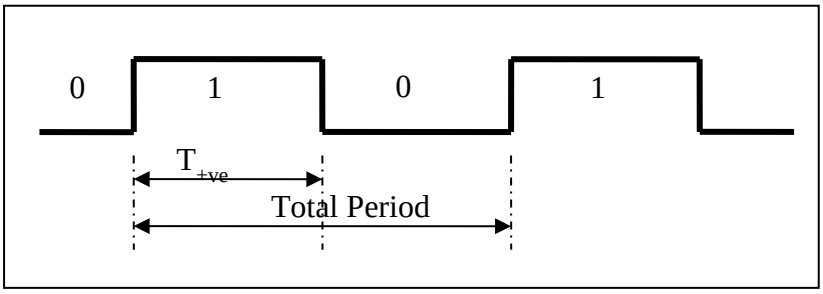

Figure 2.1.2 Illustration of Duty Cycle

Ideally, the clock signal would be designed to have a 0.5 duty cycle. However the reality is that this is hard to meet. The nature of faster electrons mobility in the NMOS than the holes mobility in the PMOS of the CMOS technology makes the variations in the rise time and fall time.

This will result a distortion to the duty cycle. The size ratio of the PMOS to NMOS could be justified to reduce the mentioned effect but an ideal duty cycle would hard to be met. Furthermore, temperature is another variable that come from the surrounding environment that the designers have no control over it. Mobility would be affected by the temperature (Sze, 2002).

Duty cycle is vital to, especially level sensitive or edge sensitive elements.

2.1.3 Clock Skew

Clock Skew is the difference in the arrival time of the clock signal on the sequentially adjacent registers (Cadence, 2013). This could be due to the difference in clock path distance and the clock loading.

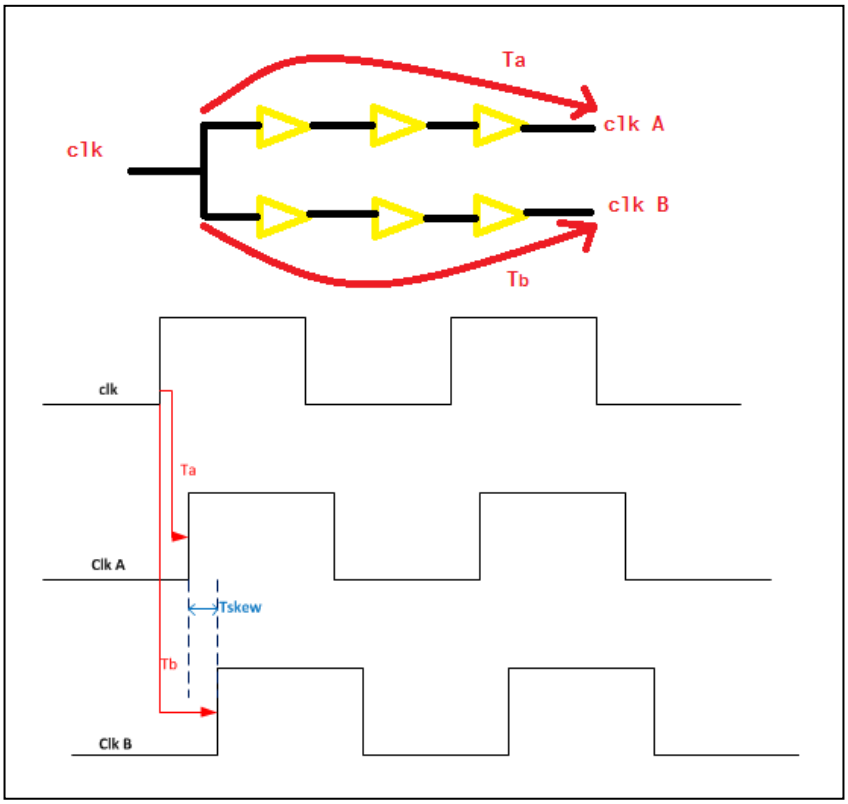

Figure 2.1.3 Illustration of Clock Skew (Rusu, 2001)

The clock skew as illustrated in Figure 2.1.3 is given by the:

$$T_{skew} = |T_a - T_b| \ldots\ldots\ldots (Eqn\ 2.1.3)$$

The clock skew, by theory should be constant from cycle to cycle (Rabaey, Anantha & Nikolic, 2003). Let's consider two clock paths, ClkA and ClkB, as shown in the Figure

2.1.3. Both clock paths are generated from the same clock source Clk. In ideal situation, both clock path should be having the same delay and suppose to arrive at the destination at the same time. However, in the real situation, both could have very different environments while travelling to the destination.

The below factors are commonly seen to introduce clock skew (Rusu, 2001):

1. Physical wire line length and load mismatch of both clock paths.
    a. The RC parasitic properties of wires differ with the length. The loads driven by each clock branches are also of different weight.
2. Process and power supply variations across the die.
    a. Oxide Thickness (T_{ox}), Effective Channel Length (L_{eff}) and etc. resulting in different channel lengths and device threshold voltage V_t across the die.
3. Temperature variations across the die on operation.
    a. Critical regions and highly active regions in an IC tend to generate more heat. The more heat the wire receives, the more resistance the wire has and thus signals get through slower.
4. Inductive effects from surrounding active elements activity.
    a. Neighbor's active components will have coupling effects and affect the clock signals.