DEVELOPMENT OF LASER ASSISTED DEVICE ALTERATION (LADA) TECHNIQUE FOR FAILURE REGION IDENTIFICATION IN INTEGRATED CIRCUIT

By

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DECLARATION

I hereby declare that the work in this dissertation is my own except for the quotations and summaries which have been duly acknowledge.

3 August 2015

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LIST OF ABBREVIATIONS

1D	-	One Dimensional
2D	-	Two Dimensional
3D	-	Three Dimensional
ADCs	-	Analog Digital Converters
API	-	Abbreviation of application Program Interface
ARC	-	Anti-Reflective Coating
ATE	-	Automated Test Equipment
ATPG	-	Automatic Test Pattern Generation
CMOS	-	Complementary Metal Oxide Semiconductor
CPU	-	Central Processing Unit
DACs	-	Digital Analog Converters
DUT	-	Device Under Test
EBAC	-	Electron Beam Absorbed Current
E_g	-	Energy Bandgap
FA	-	Failure Analysis
FIB	-	Focus Ion Beam
FinFET	-	Fin-Shaped Field Effect Transistor
Ge	-	Germanium
I/O	-	Input/output
IC	-	Integrated Circuit
IP	-	Intellectual Property
IR	-	Infrared
IREM	-	Infrared Emission Microscopy
JTAG	-	Joint Test Action Group
LADA	-	Laser Assisted Device Alteration
LSM	-	Laser Scanning Microscope
LVP	-	Laser Voltage Probe
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor

PLL	-	Phase Locked Loop
PMC	-	Power Management Controller
PMOS	-	P-channel Metal Oxide Semiconductor
RC	-	Resistor-Capacitor
RTL	-	Register Transfer Level
SEM	-	Scanning Electron Microscopy
Si	-	Silicon
SoC	-	System-on-Chip
SOI	-	Silicon On Insulator
TAP	-	Test Access Port
TCK	-	Test Clock
TDI	-	Test Data In
TDO	-	Test Data Out
TEM	-	Transmission Electron Microscopy
TMS	-	Test Mode Select
ULSI	-	Ultra Large Scale Integration
USB	-	Universal Serial Bus
USM	-	Universiti Sains Malaysia
V_{dd}	-	Drain Supply Voltage
V_{ss}	-	Source Supply Voltage

ABSTRAK

Tujuan kajian ini adalah untuk mewujudkan satu kaedah untuk menyelesaikan halangan yang dihadapi ketika melakukan Analisa Kegagalan Litar Bersepadu. Kegagalan yang berlaku dalam Litar Bersepadu meningkat berkadaran dengan peningkatan bilangan transistor, margin proses yang terhad dan juga peningkatan kerumitan Litar Bersepadu. Pasaran Litar Bersepadu amat bergantung kepada Kegagalan Analisis (FA) untuk memacu masa untuk pasaran, sebagai hasil pembelajaran dan kebolehpercayaan, penilaian eksperimen dan mendapat kelayakan teknologi. Oleh itu, teknik Laser Peranti Bantuan Pengubahan (LADA) digunakan bersama dengan Peralatan Ujian Automatik (ATE) dengan berdasarkan pada skrip Perl dicadangkan dalam kajian ini untuk menyelesaikan halangan ketika Analisa Kegagalan dalam Litar Bersepadu.

ABSTRACT

The purpose of this research is to create a solution for some of the obstacles faced during Integrated Circuit (IC) Failure Analysis (FA). Faults in ICs increase proportionally with the growing number of transistors, narrower process margins and increasing complexity of IC design. The IC industry depends heavily on FA to drive the time to market, yield and reliability learning, experiment evaluation and technology qualification. However, current FA flow is not straight forward and robust enough to solve every IC failure type, especially in solid failing cases. Therefore, a Laser Assisted Device Alteration (LADA) technique combined with Perl scripting that works on Automated Testing Equipment (ATE) is proposed in this study to solve the obstacles faced during FA. The said Perl script will act as a looping agent, test result comparator, triggering controller to enable LADA scanning and to find the sensitive transistor or circuit device towards the failure. Results from some actual case studies proved that the proposed technique can work with design as well as defect based failures, either through structural or functional tests which also needs consideration of specific sensitive circuitry within the IC design. As a conclusion, the contribution of the proposed technique is its ability to resolve solid failure problems in ICs, the capability to pin point the defective area to within a small region of up to a single transistor size and finally to simplify the entire FA process for a 3D FinFET System on Chip (SoC) IC.

CHAPTER 1

INTRODUCTION

This chapter briefly describes the main focus of the research which is IC Solid Failure Analysis (FA) with Laser Assisted Device Alteration (LADA) technique. In addition to this, the background, problem statement, objectives and scope of study, as well as the thesis organization is also determined to complete this research.

1.1 Background

The IC is one of the most significant inventions of the 20th century, introduced in 1959 by Kilby and Noyce [1]. It can be defined as a set of inter-connected active (transistor) and passive (resistor, capacitor and inductor) electronic components. These electronic components are generally made of semiconductor material (Si or Ge) and inter-connects among them could be formed by one or a few layers of conductive material and fabricated in a single chip. With Ultra Large Scale Integration (ULSI) process, the transistor count in an IC is increasing from thousands to billions on a single chip today [1]. Besides that, more complicated structures such as the 3D FinFET transistor and SoC are also being implemented in a single IC. As a result, faults that happen inside ICs also increase proportionally due to the huge number of transistors, narrow process margins and complexity of the IC. IC industry will depend critically

on FA. Speed and accuracy in FA will drive the time to market, yield and reliability learning, experiment evaluation and technology qualification.

1.2 Problem Statement

As discussed in the previous section, FA plays an important role in the IC industry. However, current FA flow is not straight forward and not robust enough to solve every type of IC failure especially in the solid failure cases. Solid failure cases in ICs are heavily dependent on the Infrared Emission Microscope (IREM) to detect abnormal emission. Roadblock to FA progress will happen if no abnormal emission is observed under IREM. The inability to deliver timely and critical FA result will affect the time to market, yield and reliability of a product and directly impact the user, company, as well as the industry. The idea being proposed in this study is using the LADA technique to drive for the solution of solid failure cases that could not observe any IREM emission hence left idle in the middle of the FA flow. However, solely depending on LADA alone would not solve the problem at hand. A Perl script will be developed as an agent to collaborate together with the LADA console system, Automated Test Equipment (ATE), ATE's Test pattern and also the device under test to solve the issue in this study.

1.3 Objective

The main objective of this study is to prove the workability of LADA technique for IC solid FA assisted by the development of a Perl script. In order to support the main objective, the following specific objectives were structured:

i. To solve the problem faced on IC during solid FA.

ii. To develop a Perl script as an agent to enable the LADA technique on IC solid failure issue.

iii. To develop full solid FA flow on IC, equipped with LADA technique.

iv. To analyze the effectiveness of the proposed LADA technique with real life 3D FinFET SoC IC solid failure.

1.4 Scope of Study

This study focuses on the development to enable LADA technique to solve the IC solid failure issue. The technical details on the flow of using LADA console system, ATE and ATE's Test will be described in Chapter 2. The scopes of this research are defined as follows:

i. Validate the output and response from the developed Perl Script as an agent to work together with LADA console system, ATE, ATE's Test and also the device under test.

ii. Analyze the effectiveness of the proposed technique with a full solid FA flow on an actual 3D FinFET SoC IC solid failure.

1.5 Thesis Organization

In general, this dissertation will be partitioned into five chapters. Chapter 1 focuses on introduction to the dissertation, which briefly discusses the background,

problem statement, objective, proposed solution and scope of study as well as thesis organization.

Chapter 2 of the dissertation outlines the literature review which discusses the experimental components and also the present FA flow together with its weaknesses. Besides that, other related information regarding the research is also discussed.

Chapter 3 explains the methodology of the developed script flow, result verification flow during data collection and also the proposed full FA enhancement methodology.

Chapter 4 of the dissertation are the results and discussion chapter. It covers the output results and response on the developed script and also some actual 3D FinFET SoC IC solid failure case studies to prove the effectiveness and workability of the developed technique.

Chapter 5 are the final chapter of the dissertation which concentrates on the research conclusion and areas of improvement of this research.

CHAPTER 2

LITERATURE REVIEW

The literature review is conducted prior to carrying out the study. The crucial points on present knowledge of the subject including the background, essential findings, experimental components, FA flow, as well as methodological and theoretical contributions to this study will be presented in subsequent sub-topics.

2.1 Experimental Components

This sub-topic will review the components used in this study. A 3D FinFET transistor SoC Integrate Circuit (IC) is the main component in this study on which all experiments are performed.

2.1.1 3D FinFET Integrated Circuit

Besides the increase in transistor count, advanced technologies used in ULSI process could also produced 3-dimensional-ICs (3D-ICs), Ultra Performance ICs (UPICs), and IC-based systems such as SoCs. The IC represented in this work will be a 3-dimensional SoC.

According to Moore's Law, the number of transistors in a given IC area will roughly double every two years which means shrinking the process technology from time to time will take place. However, as 2D CMOS transistors get smaller, the leakage current gets higher. This is because the gate of the 2D transistor has gotten weaker in its ability to control electrons at a shrunk channel between the source and drain. This will lead to electron flow through silicon substrate which is far from the gate even when it is in 'off' state. Thinning the silicon channel and building the channel on top of insulator as in Figure 2.1.1 (a) will be an enhancement for the 2D planar transistor but there will be side effects such as heat sinking problem [3]. In 2011, Intel announced a major change to the transistor architecture from 2D planar transistor as shown in Figure 2.1.1 (b) to 3D FinFET Transistor as shown in Figure 2.1.1 (c).

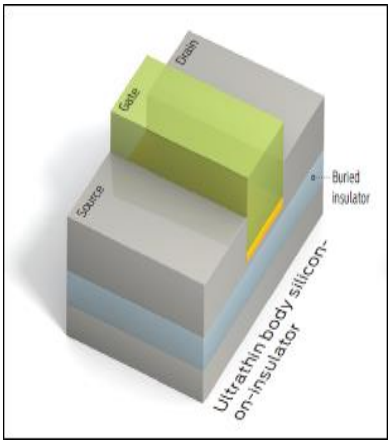

Figure 2.1.1 (a)

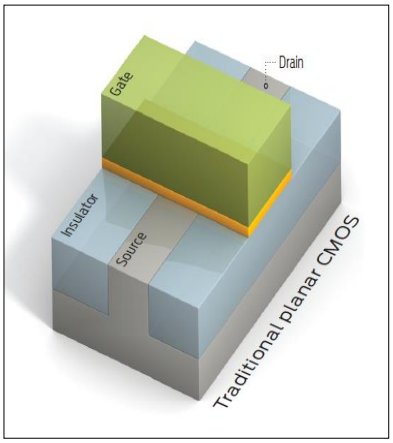

Figure 2.1.1 (b)

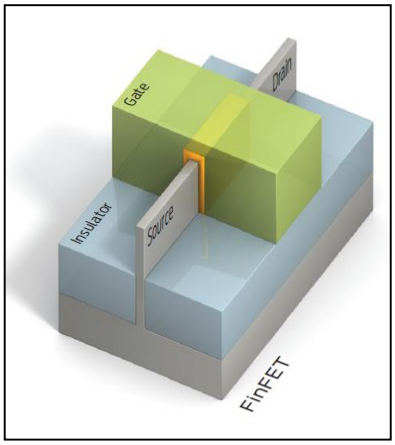

Figure 2.1.1 (c)

Figure 2.1.1(a): Ultrathin Body SOI [2]
Figure 2.1.1(b): 2D Planar CMOS [2]
Figure 2.1.1(c): 3D FinFET Transistor [2]

The 3D FinFET transistor has been designed to transform the thin silicon channel into 3D mode by creating the 'fin'. The 3D FinFET transistor's gate is shaped like an upside down U at the tip of the 'fin' and this will give perfect control to the channel carriers as shown in Figure 2.1 (c). Besides that, it also brings big gains in

terms of power consumption and faster transistor switching speed. However, the biggest challenge to the manufacturer will be huge investment for entirely a new set of manufacturing equipment, as narrow fins only allow for variations less than half a nanometer during process alignment, and compelled with the complexity of building the gate oxide [4]. As a result, FA activities on these newly developed components play an important role to drive for error fixing.

2.1.2 System-on-Chip (SoC)

Initial systems consist of just a few chips, memory and other discrete electronic components. However, cost, power dissipation, mobility, and programmability collectively become the limitations of a system with many components. Following this, components are being reduced and packed into a single chip. As a result, SoC is developed to accommodate billions of transistors on a single chip and at increasing levels of integration [5, 6]. As shown in Figure 2.1.2, integration of multiple chips and components like CPU, Display, Audio and USB module onto a single device could reduce the time to market as well as cost for the system design team. Due to significant reduction in interconnection, this will result in reduced switching capacitance and lesser power dissipation [7].

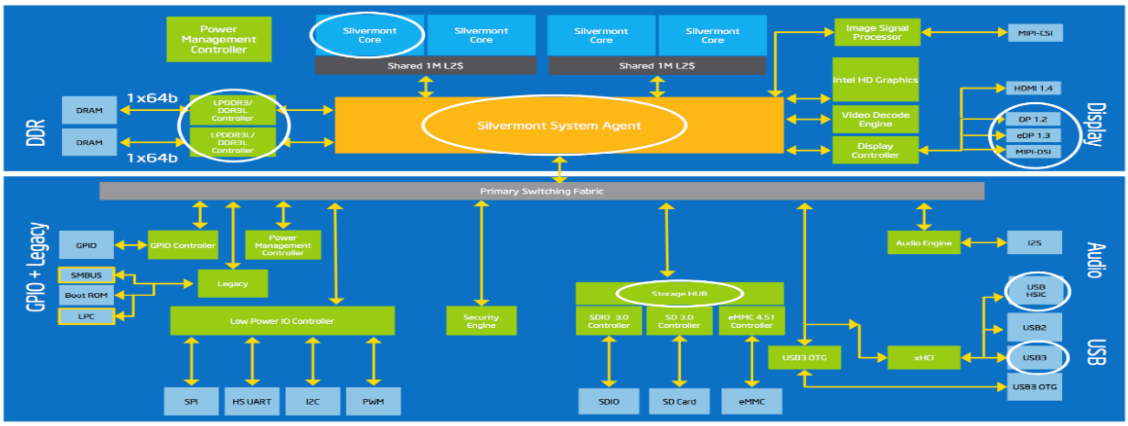

Figure 2.1.2: Intel System-on-Chip (SoC) Block Diagram [7]

Today's challenges in SoC design are the integration of complex digital and analog circuitry as well as RF components like WLAN and Bluetooth on the same chip. Integrated mixed-signal components include phase locked loop (PLL) blocks, high-speed I/O interfaces, analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) [8]. Furthermore, technology scaling is trending towards lower operating voltage and higher operating frequency. So, all of these issues have resulted in increased silicon failures or reduced yields for such mixed-signal devices. FA play an important role for the complex SoC manufacturer in order to improve the yield, reduce development cost and period by avoiding the additions of development & design stepping [9]. The FA being carried out on this study are on Power Management Controller (PMC) and Display components.

2.2 Front End Failure Analysis

Transistor count in an IC is increasing from thousands to billions until today. With this, the occurrence of failure inside ICs also increases proportionally due to narrow process margins and complexity. As a result, production in IC market will depend critically on FA to drive the time to market, yield and reliability learning,

experiment evaluation and technology qualification [10]. Generally, FA can be divided into a three step process of electrical test, failure localization and physical FA. During electrical testing, detailed info such as test area, different type of Shmoo diagram, transition waveform, data-log, as well as temperature effect will be captured. All of these detailed info will be used to narrow down the failing area of interest to minimize the effort during failure localization stage.

Failure localization can be done with the aid of logical fault diagnosis, internal circuit probing and optical analytical method. [11,12]. Logical fault diagnosis requires special dedicated design within the IC and is limited in capability and resolution as it uses data collected at the external pins of the IC to identify possible defective circuits internally. Internal probing is a difficult process that is tractable only on individual transistors that have already been identified. Today's fault isolation relies heavily on the last approach, optical analytical method which can gather information over a large area, in high speed and remotely. The analytical techniques most commonly used today are optical probing in the likes of laser voltage probing (LVP), infrared emission microscopy (IREM) and laser assisted device alteration (LADA) [13]. However, the limitation of LVP is that it requires simulation data. IREM is mainly targeted for the defect based failure and LADA is normally used for critical timing path or "speed path" debug. Besides that, LADA is mainly used with ICs which are free from manufacturing defects, need a fixed temperature, voltage and frequency at the pass-fail boundary region of an IC [14]. Due to the limitation of LADA usage in FA, this study will aim to develop the functionality of LADA which is not limited to speed path debug but also expand its usage on solid failure in an IC which can cover multiple voltage and frequency set point.

2.2.1 Laser-assisted Device Alteration (LADA)

Laser-assisted Device Alteration (LADA) can be defined as a laser-based analysis technique that can temporarily alter the transistors' operating characteristics and commonly used in FA of semiconductor devices or IC. The fundamental principle of LADA is precisely controlling the power of Neodymium-Yttrium Aluminum Garnet (Nd: YAG) continuous wave (CW) to produce near-infrared 1064nm wavelength beam to induce photocurrents inside a transistor device so that the 'normal' electrical characteristics of the device can be altered [15, 16].

The Thickness of silicon substrate of the flip chip 3D FinFET (Figure 2.2.1) would measure at around 1000 um so thinning process is needed to achieve a thickness of ~50um to avoid of the blockage of incident laser. A thin anti-reflective coating (ARC) also can be deposited onto the backside surface to minimize surface reflections as shown in Figure 2.2.1 [17].

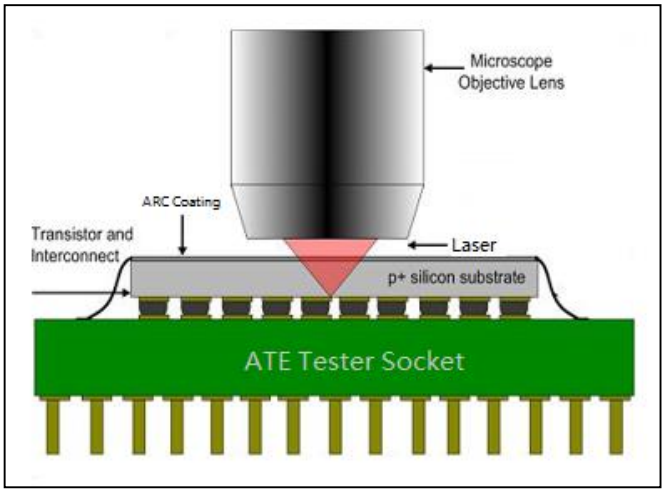

Figure 2.2.1: Flip Chip BGA with 90^{o} Laser Shinning

1064nm laser is introduced in a LADA system because energy bandgap, E_g for silicon is around 1.12 eV whereas 1064nm laser corresponds to a photon energy of ~1.17 eV, so that the laser power could be utilized as energy for electron to excite into the conduction band and cause the electron-hole (E-H) pair generation at typical silicon operating temperatures. The E_g of silicon can be calculated using equation (1) below, where $E_g(0)$ is energy needed to jump over conduction band at 0 K, α is 0.473 and β is 636 for material silicon.

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T+\beta} \text{ [18]} \qquad (1)$$

Photon to be induced inside transistor device will create electron-hole pairs as well as drift current in the reversed biased source-drain junction and the n and p substrate junction. The photo-generated currents will affect a node either directly by assisting in the charging or discharging of a load capacitance or indirectly through local modulation of electric potential thus changing the dc operating point of the transistor as shown in Figure 2.2.2.

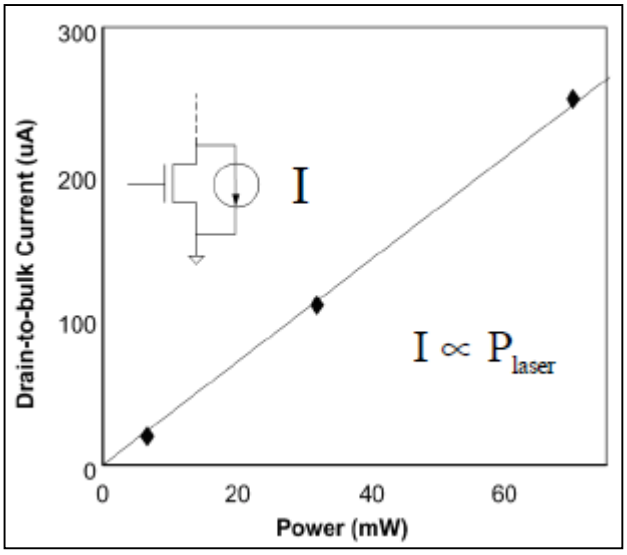

Figure 2.2.2: Drain junction photo current versus Laser Power [14]

LADA is not a standalone machine that can work together with the IC alone. It needs to be used together with an ATE which is equipped with test pattern and device under test (DUT). For them to work together, the LADA system has its own computer to connect to the laser equipment. The ATE is setup with triggering output pin, test patterns with looping capability and also DUT with stable failing signature. Inter-relations between all of the above equipment will be discussed in detail in the methodology part.

2.2.2 Front End Failure Analysis Equipment (ATE, Test Pattern and Shmoo)

To perform FA on an IC, automatic test equipment (ATE), ATE test pattern and Shmoo plotting are required. The normal approach to test an IC is to store the test stimuli onto the automatic test equipment (ATE), load the IC into ATE as device under test (DUT), test it and compare the results [19]. ATE system can be define as a system that has ability for test instruments composition, stimuli application and accurate measurement under the control of a computer console. It is usually in automated mode in electronic manufacturing industry when performing testing, measurement and evaluation of the test result [20]. ATE will produce test responses after running the IC test and the results will be compared to the expected test response, whereby if it matches it is considered to be a healthy IC, else it is considered as a faulty part. If there is a huge number of IC parts falling into the same category of faulty signature, FA will be the next step to recover and improve the situation.

However, based on ATE alone one could not define what to test and how to test for a specific partition in an IC. ATE test patterns are needed to control the ATE

on what to do and how to compare acquired results with the expected value. Generally, a test pattern is generated from outputs of a Register-Transfer Level (RTL) simulation model and converted into ATE specific vectors which consist of series of '0's and '1's as instruction and data which precisely describe the activity of each tester pin at bus clock resolution [21].

The Shmoo plot got its name based on plotting of PMOS's V_{dd} versus V_{ss} pass-fail data points in 1970s using early ATE systems. The principle of Shmoo plotting on ATE is to identify the MOSFET's basic characteristics in an IC's performance across different voltage and temperature range. As a whole, Shmoo plot plays an important role to characterize the transistor process condition and to ensure the IC works to customer's expected behavior prior to volume manufacturing [22]. Figure 2.2.3 represents a normal and healthy Shmoo plot where the test point is at the passing region. Figure 2.24 represents a marginal failure Shmoo plot where the test point is at the failing region but there are still other points which passed within the designed voltage and timing range. Figure 2.25, however, represents a solid failure Shmoo plot where all the points failed within the designed voltage and timing range.

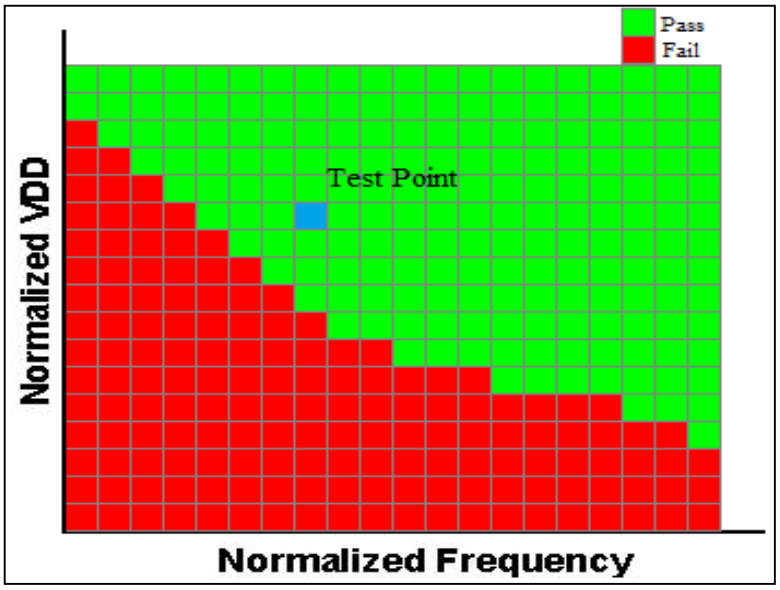

Figure 2.2.3: Normal Shmoo Plot

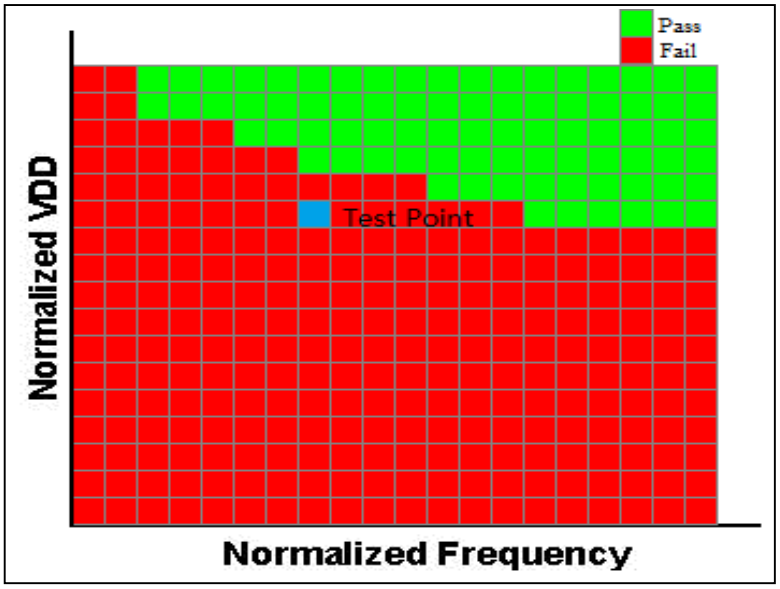

Figure 2.2.4: Marginal Failure Shmoo Plot

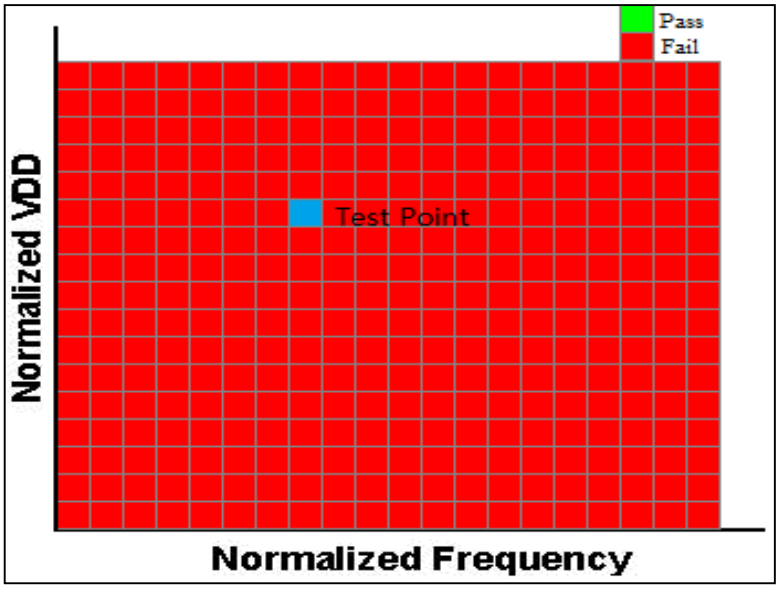

Figure 2.2.5: Solid Failure Shmoo Plot

The experiments of this project is performed on CMT ATE with structural SCAN ATPG and functional pattern in solid failure conditions.

2.3 Back End Part of Failure Analysis

Back end part of FA here would be defined as the stage after defect localization, whereby the FA engineer will have to prove his/her finding and result in the defect localization stage. Generally, failures in IC could be divided into 2 big categories which is design related failure and manufacturing defect related failure. However, there could be also a possibility of a mixture between the two or a design marginality issue due to process limitation. For design related issues, the back end part of FA will be silicon circuit edit with Focus Ion Beam (FIB) method. For defect related issue, defect inspection steps will be done using Scanning Electron Microscopy (SEM) or Transmission Electron Microscopy (TEM) when dealing with newer and smaller process technology.

2.3.1 Circuit edit with Focus Ion Beam

During FA, to screen for design errors, circuit edit is an important step to prove that it's indeed a design related issue and FIB will be the most appropriate tool to prove the success of a circuit edit before a new design is implemented [23]. Figure 2.3.1, describes the circuit edit process flow for backside chip. First step of circuit edit will start with thinning down of bulk silicon to about 100 microns, polishing for better IR image and coating with dielectric. Next will be followed by CAD navigation to find the alignment mark and trenching will be started once alignment mark is found. Main purpose of trenching will be to open a hole of a few hundred microns in size by FIB for circuit editing stage later. That will be followed by identifying the signal location of interest to be edited. Thinning and dielectric deposition will then be performed. At the end, circuit edit will be performed after matching with the CAD and the chip's IR image with fine navigation. The FIB edited IC will be tested again in ATE tester with the same test condition before edit and any changes or improvement of the IC will be observed and recorded for failure root cause purposes [24].

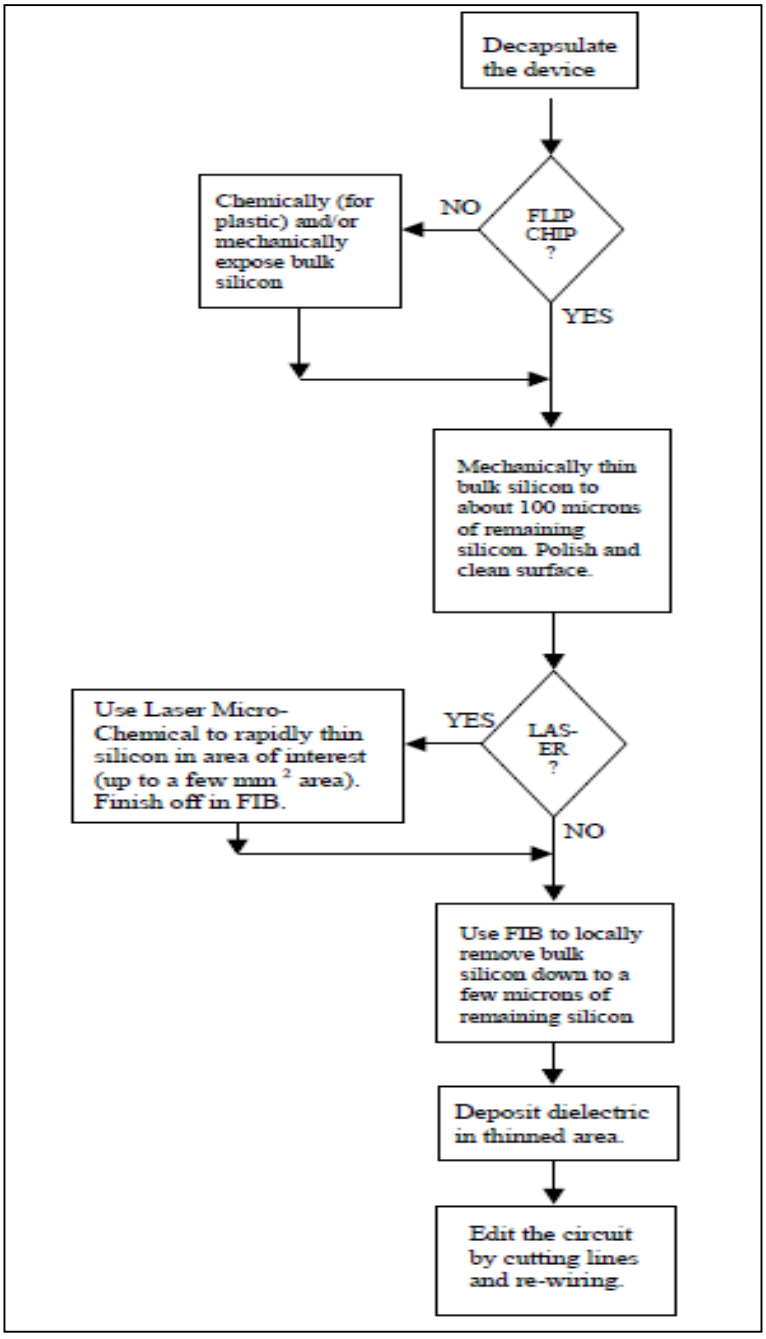

Figure 2.3.1: Circuit edit process flow for backside chip [24]

2.3.2 Defect Inspection with SEM and TEM

Besides the design related issue as discussed in section 2.3.1, defect related issue is also one of the bigger portion of IC failure analysis. Scanning Electron Microscopy (SEM) and Transmission Electron Microscopy (TEM) will be the tools

used for IC defect inspection after the defect localization stage. Usually, SEM will be the first inspection tool used as long as the SEM's resolution is good enough for inspection before proceeding to TEM analysis (with higher resolution). The SEM system includes a sample stage, electron column and also detectors as shown in the block diagram in Figure 2.3.2.

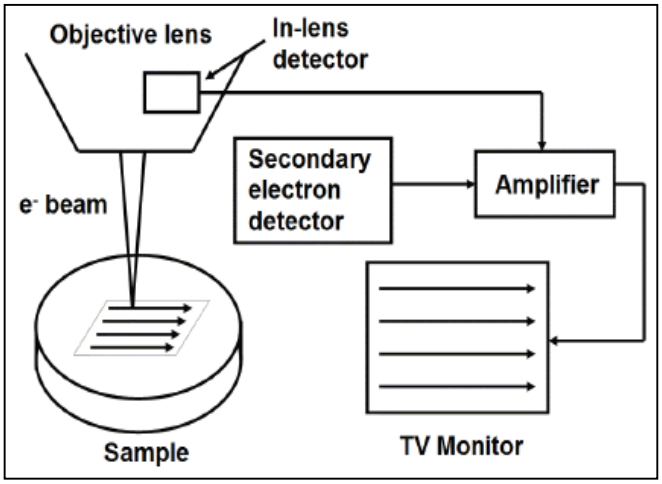

Figure 2.3.2: Block Diagram of SEM [24]

The operation of SEM is mainly the scanning of IC's surface with fine focused electron in a raster pattern. Then, then reflected electrons from the IC's surface will be collected, amplified and showed on a monitor display for viewing. SEM's electron detector acts as an electron counter to detect the number of reflected electrons [25]. Scanning each pixel of the of IC's surface will produce very life like, easily interpreted 3D image as in Figure 2.3.3.

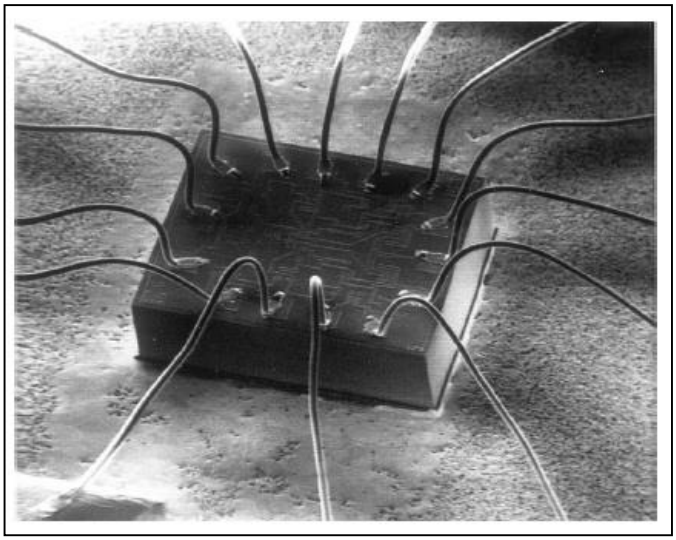

Figure 2.3.3: Low magnification SEM image of an integrated circuit [24]

Aggressive scaling in semiconductor industry that follow Moore's law has made defect inspection to be extremely challenging. Transmission electron microscopy (TEM) with excellent spatial resolution and elemental analysis capabilities will be one of the tool of choice to overcome the scaling challenge. Operation of TEM is to transmit a high energy (~1k to 3k keV) electron beam through the thinned region (~100 nm) of interest (ROI) on an IC [26]. Transmitted, elastic scattered, and inelastic scattered electrons are collected and used to form the image at the end as shown in Figure 2.3.4 [27]. Besides that, another feature of TEM is elemental analysis technique which utilizes X-ray photons in energy dispersive spectroscopy (EDS) [28].

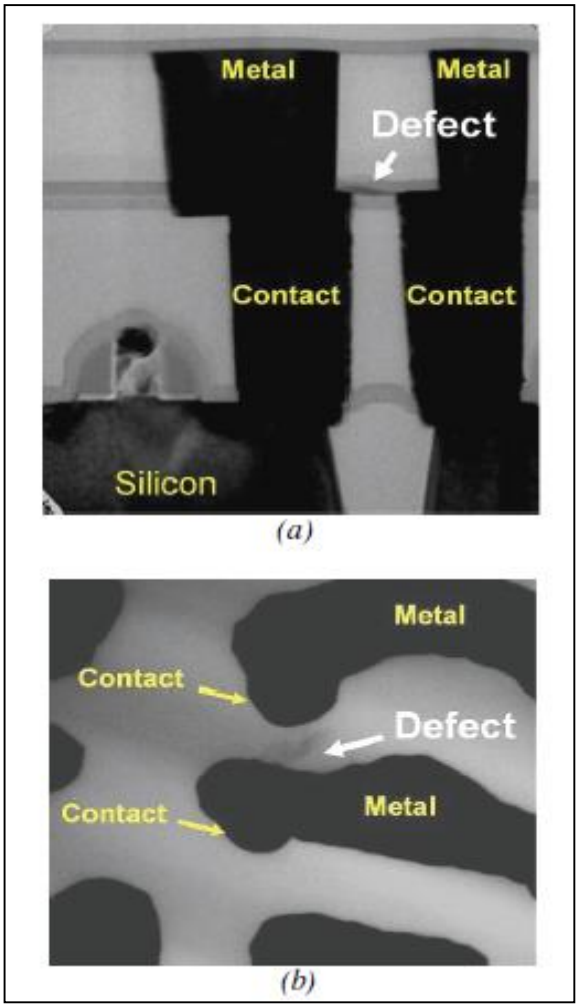

Figure 2.3.4: TEM images [26]

2.4 Summary of Literature Review

As a summary, 3D FinFET transistor SoC IC is the main component in this study in which all experiments were performed. FA activities on these newly developed component 3D FinFET SOC IC play an important role to drive for error fixing to improve the yield, reduce development cost and time by avoiding the additions of development & design stepping [9]. Besides that, production in IC market will depend critically on FA to drive the time to market, yield and reliability learning, experiment evaluation and technology qualification [10].

The front end FA analytical techniques most commonly used today are optical probing in the likes of laser voltage probing (LVP), infrared emission microscopy (IREM) and laser assisted device alteration (LADA). This study aims to develop the functionality of LADA which is not limited to speed path debug but also expand its usage on solid failure in an IC which can cover multiple voltage and frequency set point.

The back end part of FA here would be defined as the stage after defect localization, whereby the FA engineer will have to prove his/her finding and result in the defect localization stage. For design related issues, the back end part of FA will be silicon circuit edit with Focus Ion Beam (FIB) method. For defect related issue, defect inspection steps will be done using Scanning Electron Microscopy (SEM) or Transmission Electron Microscopy (TEM) when dealing with newer and smaller process technology.

CHAPTER 3

RESEARCH METHODOLOGY

The research methodology used in this work described in this chapter. Generally, the approach of how to conduct the experiment, limitation of normal FA flow, enhancement of weakness as well as the subsequent step to verify the data collected from the experiments are described. Besides that, the verification process for all stages are also explained.

3.1 Typical Failure Analysis Flow

Figure 3.1.1 shows the typical FA flow for solid failure case as well as marginal failure case. Firstly, a case which is requested for failure FA will be followed by failure reproduction. In detail, data collection at FA platform includes testing the area of interest, different types of Shmoo diagram, transition waveforms, data-log, as well as temperature effect. Next to follow is defect localization and this is typically divided into 2 groups which is solid failure case and marginal failure case. Marginal failure case will proceed with LADA experiment and solid failure case will proceed with IREM after fault isolation stage. The best isolation path for both types of cases is to locate sensitive device(s) for marginal cases and observe abnormal emission for solid failure cases. The sensitive device can be define as an IC's component that could make the test pass with the assist of laser power. This will be followed by back end FA and

lastly proceed with closure. This thesis will focus on those solid failure cases that could not observe abnormal emission under IREM and could not proceed further. This study will enable the LADA capability for solid failure cases to complete the entire FA flow.

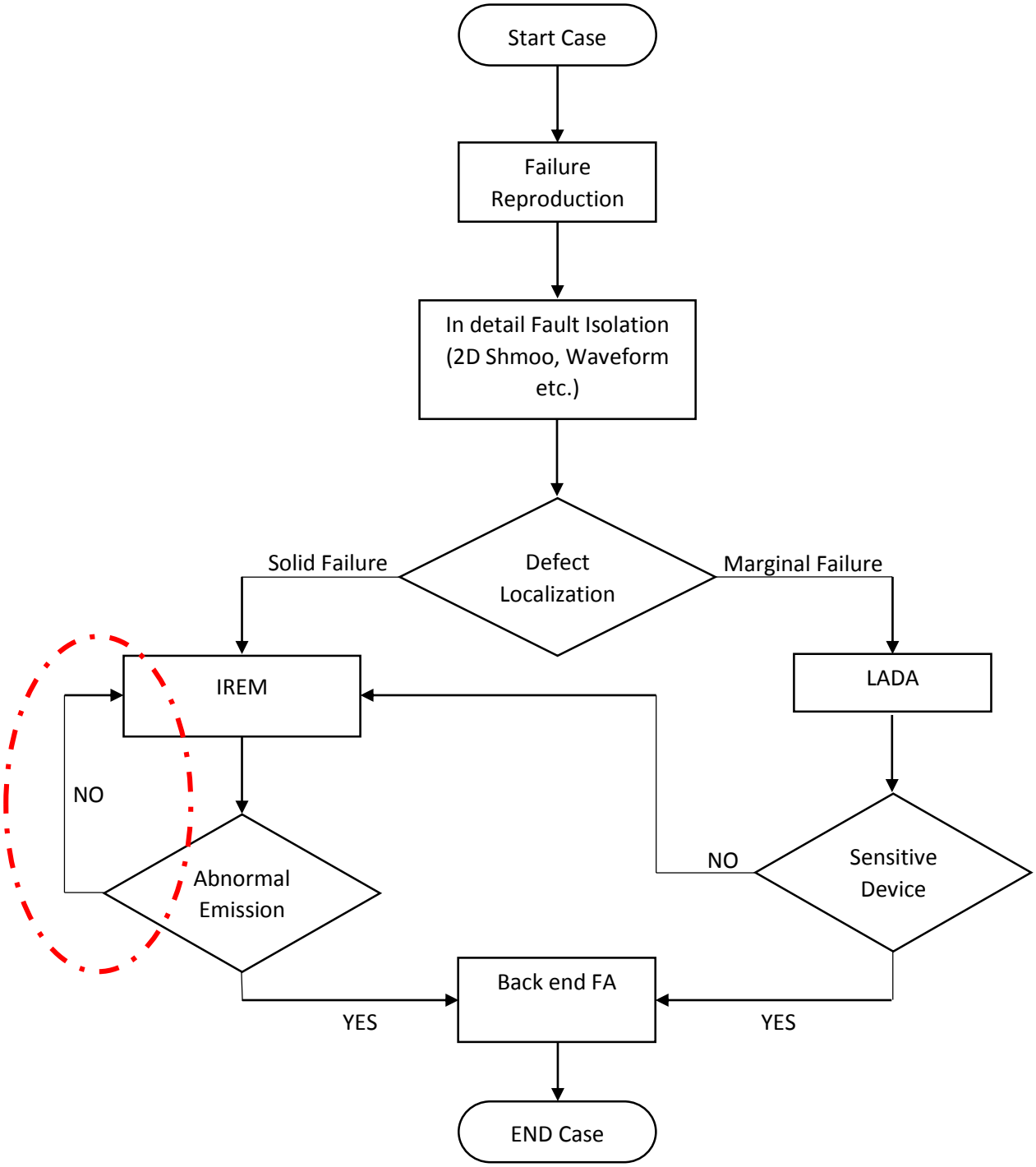

Figure 3.1.1: Normal Failure Analysis Flow

3.2 Script and Signal Triggering Validation Flow

Before LADA experiment is started, script and signal triggering validation is a mandatory process. This is because the script and signal triggering play an important role to pin point the device sensitive to laser. If the script and signal triggering is not correctly functioning, sensitive device found during LADA scanning might also be inaccurate. Script, signal triggering, test pattern and test program modification will be validated together and observed through an oscilloscope as shown in Figure 3.2.1 below.

First of all, test set point will be set at failing condition with reference to the Shmoo plot. A trigger pulse pattern will be inserted into the test's triggering pin. A trigger pulse can be in any pattern form like "0011", "0001" or "0101" for easy recognition purpose when observed under oscilloscope later. After that, a connection needs to be established between ATE's trigger pin and LADA equipment through an SMA cable. Besides that, the test program will need to be modified to infinite number of failing count to avoid any disruption to sustain looping mechanism. Next will be followed by starting of Perl script in ATE's API environment with the needed parameter link range of voltage and timing parameters. Perl script is needed to run at API environment because ATE's API function is needed to link the computer to the ATE's console, without this the Perl script could not make any changes to the ATE's functionalities.

SMA cable that is connected to LADA equipment will be connected first to oscilloscope for signal observation. If the pattern inserted to the running test's triggering pin can be observed under oscilloscope, means the setup is validated