EVALUATION OF 28NM 10 BIT ADC USING RAMP AND SINUSOIDAL HISTOGRAM METHODOLOGIES

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By

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF NOMENCLATURE

t	: Time
V	: Voltage
A	: Amplitude
n	: Number of bits
G	: Gain
Fs	: Sampling Frequency
Fi	: Frequency of Interest
M	: Number of cycles for input signal frequency
N	: Number of samples for sampling frequency
C	: Offset amplitude of sine wave

LIST OF ABBREVIATIONS

ADC : Analog to Digital Converter

DAC : Digital to Analog Converter

ATE : Automatic Test Equipment

DSP : Digital Signal Processing

AWG : Arbitrary Waveform Generator

OE : Offset Error

GE : Gain Error

FSE : Full Scale Error

FSR : Full Scale Range

DNL : Differential Non linearity

DLE : Differential Linearity Error

INL : Integral Non Linearity

ILE : Integral Linearity Error

LPF : Low Pass Filter

DUT : Device Under Test

THD : Total Harmonic Distortion

SNDR : Signal to Noise Distortion Ratio

SFDR : Spurious Free Dynamic Range

VREF : Reference Voltage

FFT : Fast Fourier Transform

MSE : Multi Site Efficiency

SOC : System on Chip

PDF : Probability Density Function

PENILAIAN 28NM 10 BIT ADC MENGGUNAKAN KAEDAH HISTOGRAM RAMP DAN SINUSOIDAL

ABSTRAK

Ujian pengeluaran ADC menjadi lebih mencabar disebabkan prosedur ujian yang lebih ketat dikenakan keatas ADC generasi baru. Trend harga silikon menurun manakala trend harga ujian semakin meningkat. Oleh sebab itu, mengurangkan kos ujian dan mengekalkan ketepatan ujian adalah penting untuk pengujian berkuantiti besar di sektor pengeluaran. Kajian ini dijalankan bagi ketepatan pengujian ADC menggunakan kaedah histogram. Kaedah histogram adalah prosedur ujian yang paling biasa digunakan dalam ujian pengeluaran berkuantiti besar. Pada masa yang lalu, banyak kajian yang dijalankan terhadap pengujian ADC tetapi tiada penekanan terhadap kepelbagaian kaedah histogram untuk pengujian berkuantiti besar. Objektif kajian ini adalah untuk membangunkan penyelesaian ujian bagi 28nm 10 bit ADC menggunakan kaedah histogram. Hasil daripada kajian ini jelas menunjukkan bahawa program ujian yang dibangunkan berupaya mengasingkan peranti yang lulus dan gagal. 98.18% peranti berupaya untuk lulus ujian ADC manakala selebihnya 1.82% peranti gagal ujian ADC. Telah didapati bahawa kaedah Ramp Histogram dan Sinusoidal Histogram telah mencapai objektif kajian ini kerana kedua-dua kaedah menunjukkan keputusan yang agak sama berdasarkan perbandingan yang telah dibuat. Telah diketahui bahawa ujian ADC yang tepat memerlukan saiz sampel yang besar. Kajian ini telah menemui bahawa pengujian berbilang tapak berupaya untuk mengimbangi kelemahan dalam kaedah histogram. Keputusan menunjukkan ujian berbilang tapak adalah 63.72% lebih cekap dari segi masa pengujian.

EVALUATION OF 28NM 10 BIT ADC USING RAMP AND SINUSOIDAL HISTOGRAM METHODOLOGIES

ABSTRACT

ADC production testing has become more challenging due to more stringent test procedure for new generation of ADC. The trend for silicon cost is going down while the cost of test is going up. Therefore, to reduce the cost of test and preserve the test accuracy is essential for high volume testing in production. This research is conducted for accurate ADC testing using histogram methodologies. Histogram methodology is the most common test procedure used in high volume production testing. In the past there were a lot of studies on testing the ADC but there were no emphasizing on various histogram methodologies for high volume testing. This research objective is to develop test solutions for 28nm 10 bit ADC using histogram methodologies. The outcome from this research has clearly shows that the test program that has been developed is able to segregate the good and bad devices. 98.18% of the devices are able to pass the ADC testing while remaining 1.82% fail the ADC test. It was found that Ramp Histogram and Sinusoidal Histogram method has achieved this research objective as both methodologies shows similar result based on comparison that has been made. It was known that accurate ADC testing requires large sample size. This research found that multi-site testing was able to compensate the drawback in histogram methodologies. The result shows that multi-site testing is 63.72% more efficient in term of ADC testing time.

CHAPTER ONE

INTRODUCTION

1.0 Background

At present, most part of the signal processing in areas like instrumentation, telecommunications, and control is carried out at the digital domain. Therefore, ADC plays an important role to convert analog signal to digital signal. The presence of the ADC macro cells embedded in complex system on chip requires correct evaluation and testing using production tester as known as Automatic Test Equipment (ATE).

As the new generations of ADC provide increase in resolution and speed, the test requirements become more stringent and resulting in more expensive test procedures. The test cost frequently reaches half price of the device itself and this would increase the cost of the device in the end user market and forcing electronic manufacturer to offer competitive price. Test cost control is becoming important in the semiconductor industry because testing cost is increasing while the cost of silicon is decreasing. ADC is a key component of mixed-signal SOCs, so their testing is important. For high-resolution, slow sampling rate ADCs (such as SAR ADCs embedded in micro-controller chips), their DC linearity testing is very important but very time consuming, and hence costly (Satoshi, et al., 2010). Figure 1.1 shows the trend for silicon cost going down while the test cost is going up. The cost for silicon is decreasing due to the cost per transistor is decreasing. Technology to produce silicon wafer keep improving year to year and silicon manufacturer can offer cheaper price for their silicon wafer because they can manufacturer the silicon wafer in large quantity. Furthermore, the silicon demand is increased due to the fast pace

technology nowadays attracts more silicon wafer manufacturer compete in the market. Oversupply of the silicon wafer will also contribute to the silicon cost decreasing in the market. Due to fast growing technology, more circuits need to be tested and this will increase the testing time utilization. Thus, the test cost is increased. As a result, ADC requires accurate test methodology and at the same time with faster testing time to improve test yield and test cost of the device. Test accuracy is essential in high volume production testing because accurate test methodology will prevent over reject in testing.

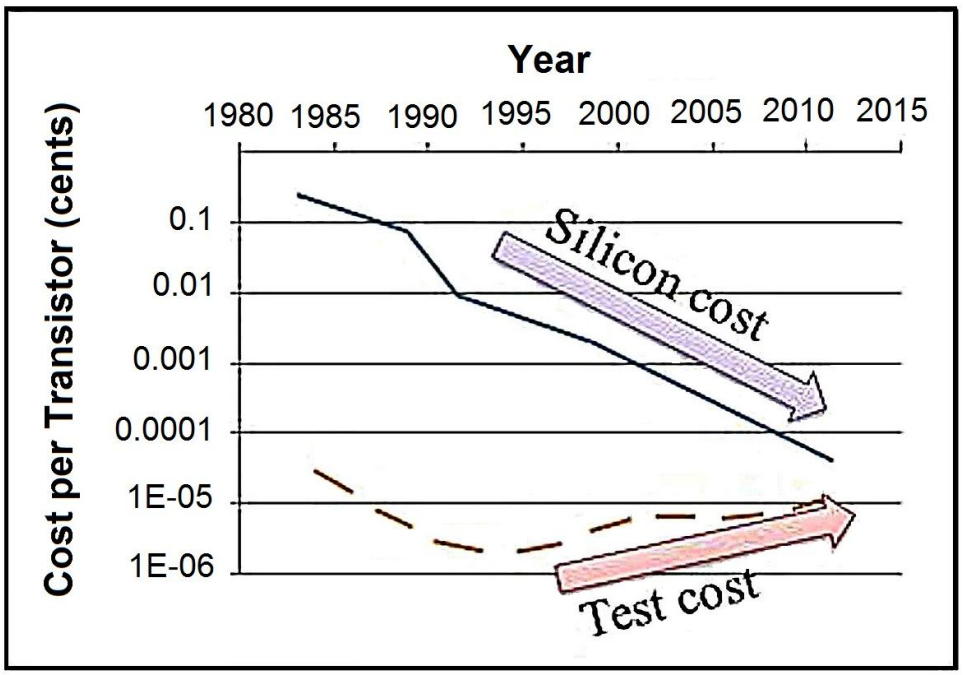

Figure 1.1. Silicon Cost and Production Test Cost Trends (Satoshi, et al., 2010)

This work is focusing on ADC test methodology. In ADC testing using Automatic Test Equipment (ATE), analog input stimulus is generated by an arbitrary waveform generator (AWG) which employs a Digital to Analog Converter (DAC) and output code for each analog voltage conversion is measured using digital capture. The input stimulus signal is created with mathematical method, and the measured signal is processed with mathematical algorithm, extracting various parameters such

as Differential non-Linearity Error (DNL), Integral non-Linearity (INL), Offset Error (OE) and Gain Error (GE). Test execution and hardware programming is controlled by the ATE test program. Figure 1.2 illustrated the block diagram for generic ATE test system to test the ADC embedded inside the DUT. ATE test system operation requires the test hardware to be used as interface card in between DUT and test system.

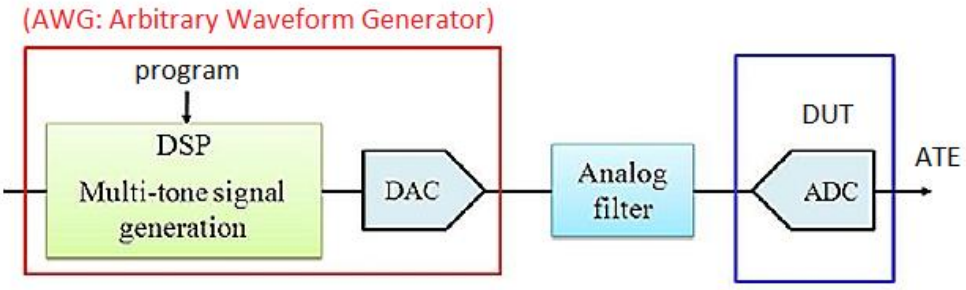

Figure 1.2. Test System to Generate Analog Input Stimulus (Satoshi, et al., 2010)

The most typical ADC output signal processing method is using Histogram analysis. Basically, there are two types of Histogram which is Ramp Histogram and Sinusoidal Histogram. Ramp Histogram method appears a flat line profile for linearity calculations. In Sinusoidal Histogram method, a very low distortion wave is required. It is relatively easy to generate such a low distortion sine wave because an appropriate low pass filter (LPF) can easily remove distortions. However, since ADC generate non-flat histogram distribution for Sine wave; post processing of the Sinusoidal Histogram for linearity calculation becomes much more complex than Ramp Histogram (Hideo, 2009). The sine wave based method is called “dynamic linearity” because high frequency sine waves are easier to generate and the method can be used to evaluate the linearity of the ADC during dynamic input conditions. Sometimes the term “DC linearity” is used to denote that the “linearity” is measured at a very low conversion rate, using a DC-like, slowly varying input (Turker, 1999).

When testing the ADC, there are two types of ADC data to determine the performance of ADC which is static and dynamic performance. Static performance such as Differential non-Linearity (DNL), Integral non-Linearity (INL), Offset Error (OE) and Gain Error (GE) are the typical measurement of ADC during high volume production testing. Dynamic performance of ADC involve the measurement of the parameter induced by the noise level such as Signal to Noise and Distortion Ratio (SNDR), Total Harmonics Distortion (THD) and Spurious Free Dynamic Range (SFDR). Usually, dynamic performance of ADC is measured to characterize the noise level of the DUT. The presence of noise could affect the quality of generated sine wave and sampling for ADC testing using histogram method. The noise could be generated from a few sources such as test equipment clock jitter, harmonics from test equipment, DUT's input circuitry, DUT's aperture jitter and DUT's nonlinear distortion (Fang, 1999). In this research the focus is only on the static parameter of ADC because the study of dynamic parameter is more suitable for high resolution ADC.

1.1 Problem Statement

The presence of the ADC macro cells embedded in complex system on chip requires correct evaluation and testing using production tester as known as Automatic Test Equipment (ATE). As the new generations of ADC provide increase in resolution and speed, the test requirements become more stringent and resulting in more expensive test procedures (Azaïs, et al., 2003). The test cost frequently reaches half price of the device itself and this would increase the cost of the device. According to prior research (Paolo, et al., 2002), the assurance and improvement of quality levels characterizing the performance of analog-to-digital converter (ADC)

require the careful selection of post-production device testing methods. In fact, considerations mainly based on economical reasons demand the tests to be quick, effective, easily reproducible, and simple. In practice, both static and dynamic information on the ADC behaviour is usually needed, as well as figures showing its performance both in the time and frequency domains. It is widely recognized that, among other parameters, ADC Integral non-Linearity (INL) and Differential non-Linearity (DNL) represent quantities of paramount importance for the description of the tested device quality under both static and dynamic conditions. To measure the ADC linearity parameters, the histogram test methodology is applied. This methodology is based on the use of a signal source exciting the ADC under test and the evaluation of the histogram analysis of the device output codes. Accordingly, the prior knowledge about the amplitude distribution of the converter input signal is employed. The linearity parameters are finally estimated by processing the ADC output code histogram. The most frequently used device input stimulus is the sinusoidal and ramp, even though Gaussian noise has been recently proposed as an alternative approach. Whichever the excitation signal type, if the information carried by the device output sequence is effectively processed, the time needed to obtain prescribed levels of estimation accuracy is minimized. Since the test costs are directly related to the test process duration, efficiently processing data helps in keeping test expenses at a minimum.

In the past, there were a lot of study on the various test methodology and test algorithms for ADC but there was no emphasize on the ADC production testing with high accuracy, minimizing yield loss and test cost. This research will expose more on the ADC test using histogram methodologies for high volume testing in production.

1.2 Aim

The aim of this research is to develop test solution for Analog to Digital Converter (ADC) in high volume production testing using histogram methodologies. This research will help Test Engineer to be better understanding the concept behind ADC testing and aware of the factor that could induce the test performance of ADC in DSP based testing. Outcome from this research would help to improve ADC test accuracy and yield as well as production test time. Organization could benefit from product test accuracy, reliable test solution, test cost saving and production cycle time to meet customer requirement.

1.3 Research Objective

The objective of this research is based on the ATE test methodology for ADC. ADC used in this research is 10-bit resolution ADC and it is designed using 28nm technology. There are three objectives in this research as follows:

i. To develop test solution for 28nm ADC 10-bit resolution under production test environment using ATE.
ii. To evaluate ADC test performance with different input stimulus (Ramp and Sinusoidal input).
iii. To perform ADC parallel testing and test time reduction with multi-site testing.

1.4 Scope and Limitations

ADC parametric testing for 10-bit ADC in 28nm SOC is a focus in this research. ADC device under test is the ADC macro cell embedded inside system on chip. This type of ADC has different internal reference voltage. It will need a

specific method to determine internal voltage reference. Test execution is controlled by ATE test program that has been developed using C++ programming language and ATE firmware instructions. Test methodology for ADC is DSP-based testing method call histogram method and it requires analog voltage as an input stimulus to ADC. The input supply to ADC is generated by Arbitrary Waveform Generator (AWG) inside analog sub-system called AV8. This analog voltage supply need a set of hardware configuration to ensure low distortion signal is generated out from AV8. Basically, there are two types of analog supply for ADC which is ramp input and sine wave input. This research will discuss both type of analog input and algorithms in formulating the linearity test. The output code from each ADC conversion will be processed using histogram analysis to determine the value for Differential non-Linearity (DNL) and Integral non-Linearity (INL).

Dynamic parameter measurement will not be covered in this research because it requires RF-subsystem to analyse the dynamic parameters of ADC especially in frequency domain. For high resolution ADC, it is essential to measure and study dynamic performance of ADC. Noise issue is always a challenge in high resolution ADC testing. In this research, parameters that we measure are static parameters of ADC consist of Offset Error, Gain Error, INL and DNL.

1.5 Thesis Structure

Chapter Two discusses the literature review of ATE test methodology in ADC testing using ramp histogram method and sinusoidal histogram method. Included in this chapter are algorithms and ADC output processing method proposed for ADC testing.

Chapter Three discusses the methodology of this research. The approach used is investigating on the ramp and sinusoidal histogram method with proposed histogram algorithm and ADC parameters calculation.

Chapter Four discusses the result from the proposed ramp and sinusoidal histogram method. The observations and conclusion on the results are also included in this chapter.

Chapter Five discusses the conclusion of this research and future work to enhance ADC production test methodology using ATE.

1.6 Research Contributions

This research main contribution is more towards the test solution for 28nm 10 bit ADC under high volume production environment. In previous research, there were a lot of studies done on ADC parametric testing but there was no emphasizing on various histogram methodologies using ATE. Besides that, this research contribute to the histogram methodologies comparison and some idea on ADC test parametric setting in term of sampling frequency, sampling size and optimized parameters in generating the ADC test solutions. Then, there will be some idea contributed by this research on compensating the test cost with the test accuracy using multi-site testing.

In general, this research also helps Test Engineer to get better idea and concept behind ADC testing in high volume production environment. With some study on various ADC histogram test methodologies, organization could take benefit

from production yield improvement and test cost reduction. In many products, mix signal intellectual properties (IP) or mix signal devices has common methodology to test and it is a good idea to grow the knowledge in this area. With the knowledge growth in ADC or mix signal testing, organization could benefit in providing more competitive workforce in semiconductor testing industry.

CHAPTER TWO

LITERATURE REVIEW

2.0 Introduction

In this chapter, the literature review used in this research is presented. First topic is on the introduction to ADC. Explanation on what the ADC is and testing parameters used to determine performance of ADC. The following sections will focus on ADC sampling theorem, discussion on ADC oversampling and undersampling. A brief discussion on histogram test methodology used in ADC testing is also presented in this chapter. Discussion is based on prior research done on ADC testing using histogram analysis. Then, this chapter will be discussing on multi-site testing on ADC using ATE and potential cost saving with ADC multi site testing.

2.1 Analog to Digital Converter

Analog to Digital Converters (ADC) is widely used in many application fields to employ digital systems which realize superior performances with respect to analog solutions. Various examples of ADC applications can be found in Data Acquisition Systems, Measurement Systems, or Digital Communication Systems. Such a widespread usage present significance to the testing activities, which nowadays largely contribute to the production costs of integrated circuit devices (Francisco, 2004). Analog-to-Digital Converter (ADC) is called mix signal device because it has both analog and digital functions. ADC can be considered simply to be the instrument or device that provides an output that digitally represents the input voltage or current level. Most ADCs convert an input voltage to a digital word, but the true definition of an ADC does include the possibility of an input current. An

ADC has an analog reference voltage or current against which the analog input is compared. The digital output word tells us what fraction of the reference voltage or current is the input voltage or current. Basically, the ADC is a divider and the IO transfer function is given by the formula indicated in equation 2.1. Output of ADC indicated input as what fraction of reference voltage.

$$Output = \frac{2^n \times G \times A_{IN}}{V_{REF}} \tag{2.1}$$

where

n = number of output bits (resolution)

G = gain factor (typically = 1)

A_{IN} = analog input voltage

V_{REF} = reference voltage

For a 3-bit ADC, there are 8 possible output codes. For example, if the input voltage is 5.5V and the reference voltage is 8V, then the output code is 101. More bits give better resolution and smaller steps. A lower reference voltage gives smaller steps, but it could be at expense of noise.

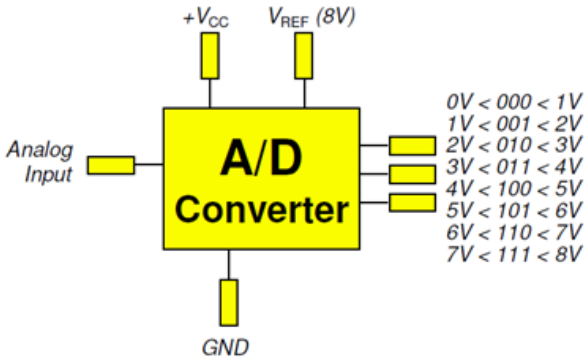

Figure 2.1. 3-bit Analog to digital converter (Nicholas, 2006)

Figure 2.1 shows the example of 3-bit analog to digital converter and it has 8 possible output codes. The difference between each output code is VREF / 2^3. Assuming for ideal case and the output response has no error; the output code will increase by one bit if the input voltage has increase by 1V. The least significant bit (LSB) represents 1 Volt, which is the smallest increment that this converter can resolve. For this reason, the resolution of this converter is 1.0V because voltages can be resolved as small as 1 Volt. Resolution could be presented in bits as well. If the reference voltage being reduced to 0.8V, the LSB would then represent 100mV and a smaller range of voltages (0 to 0.8V) can be measured with greater accuracy. The Resolution of an ADC is the number of output bits that the ADC has. Resolution could also be defined as the size of the LSB (Least Significant Bit) or one count. The Least and Most Significant Bits (LSB and MSB) are just what their name implies; those bits that have the least weight (LSB) and most weight (MSB) in a digital word. For an n-bit word, the MSB has a weight of $2^{(n-1)} = 2^n / 2$ where "n" is the total number of bits in the word. The LSB has a weight of 1.

Since one LSB is equal to VREF / 2^n, it stands to reason that better accuracy (lower error) can be achieved by using a higher resolution converter or smaller reference voltage. Higher cost is a concern in using higher resolution ADC. Also, the smaller LSB means it is difficult to find a really small signal as it becomes lost in the noise, reducing SNR performance of the converter. The problem with reducing the reference voltage is a loss of input dynamic range. A small signal in the noise also can be loss, causing a loss of SNR performance.

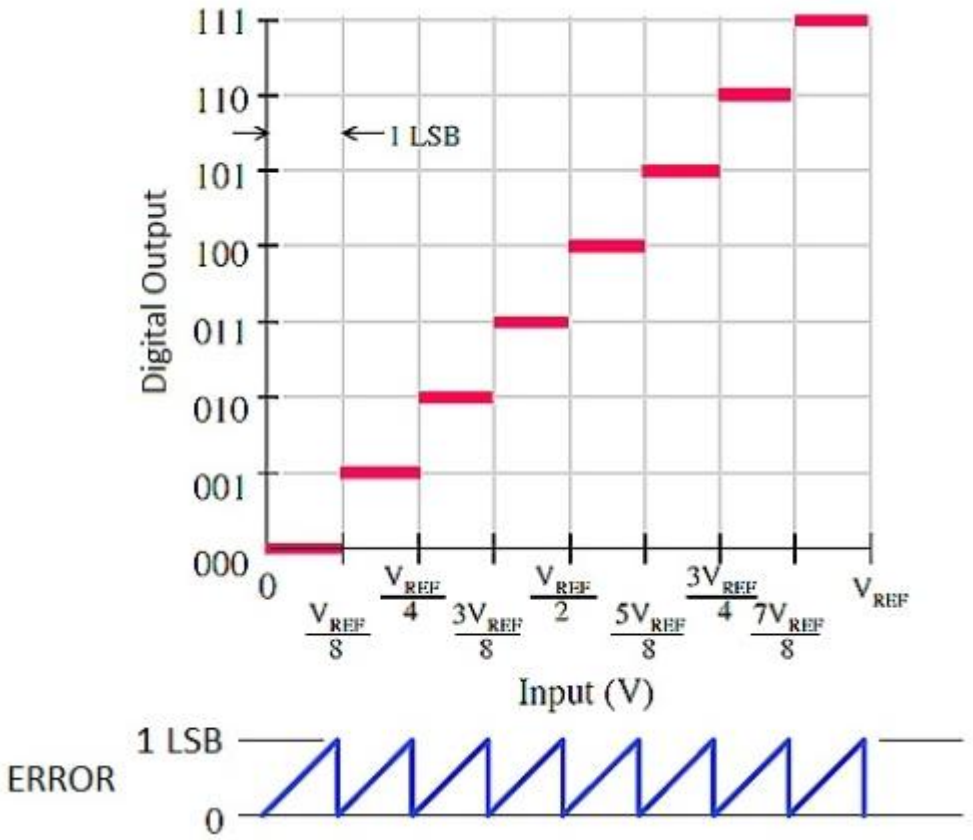

Figure 2.2. Quantization error (Nicholas, 2006)

For 3-bit ADC as an example, an ADC input of zero produces an output code of zero (000). As the input voltage increases towards VREF/8, the error also increases because the input is no longer zero, but the output code remains at zero because a range of input voltages is represented by a single output code. When the input reaches VREF/8, the output code changes from 000 to 001, where the output exactly represents the input voltage and the error reduces to zero. As the input voltage increases past VREF/8, the error again increases until the input voltage reaches VREF/4, where the error again drops to zero. This process continues through the entire input range and the error plot is a saw tooth, as shown in Figure 2.2. The maximum error we have here is 1 LSB. This 0 to 1 LSB range is known as the "quantization uncertainty" because there are a range of analog input values that could have caused any given code and uncertain on what the input voltage was that caused

a given code. The maximum quantization uncertainty is also known as the "quantization error" and this error results from the finite resolution of the ADC. ADC can only resolve the input into 2^n discrete values. Each output code represents a range of input values. This range of values is called quanta which typically assigned with symbol "q". The converter resolution is presented by 2^n. For example, an 8 Volt reference (with a unity gain factor), a 3-bit converter resolves the input into VREF/8 = 1 Volt steps.

2.1.1 Offset Error

For ideal ADC, an input voltage of q/2 will just barely cause an output code transition from zero to a count of one. Any deviation from this is called Zero Scale Error or Offset Error. This error is positive or negative when the first transition point is higher or lower than ideal, respectively. Offset error is a constant and can easily be factored or calibrated out.

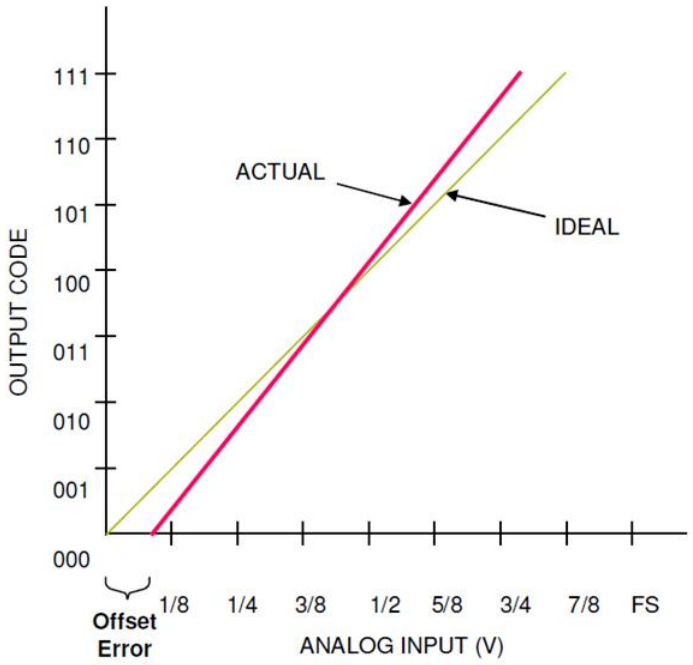

Figure 2.3. Offset error (Nicholas, 2006)

Offset error as illustrated in Figure 2.3 may be expressed in percent of full scale voltage or in LSB. Bottom Offset differs from Offset Error in that Bottom Offset is the input voltage required to cause a transition of the output code to the first count.

2.1.2 Full-Scale Error

For ideal ADC, the output code transition to full scale just barely occurs when the input voltage equals G*VREF*(2^n - 1.5) / 2^n, where "G" is the gain of the converter (typically, G =1). VREF is the ADC reference voltage and "n" is the resolution (number of output bits) of the ADC. In an actual ADC the full-scale analog input causing this transition may differ somewhat from this ideal value. Full Scale Error is the error in the actual full-scale output transition point from the ideal value. Part of this error will be due to offset voltage and the rest will be due to an error in the slope of the transfer function.

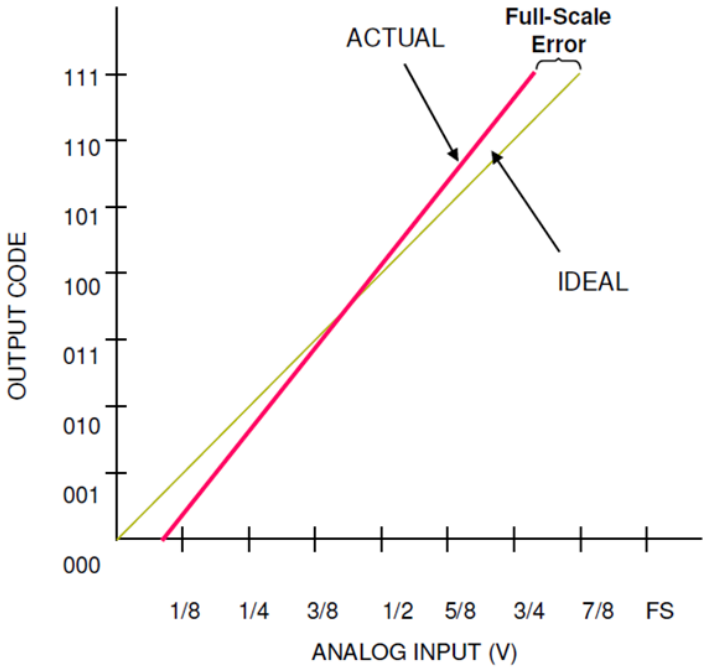

Figure 2.4. Full-Scale error (Nicholas, 2006)

Figure 2.4 shows Full Scale Error that is caused by the error in the slope of the transfer function. Full Scale Error may be expressed in LSB or as a percentage of the full-scale voltage.

2.1.3 Differential non-Linearity (DNL)

DNL and DLE are different terms used to describe the error in step size. Similarly, INL and ILE are different terms used to describe the maximum deviation from the ideal transfer function. DNL is the difference between the ideal and the actual input code width. The input code width is the range of input values that produces the same digital output code. For positive DNL we look at the widest input code range. For negative DNL we look at the narrowest code range. INL is the maximum deviation of the transfer function from a straight line between two points along the input-output transfer curve.

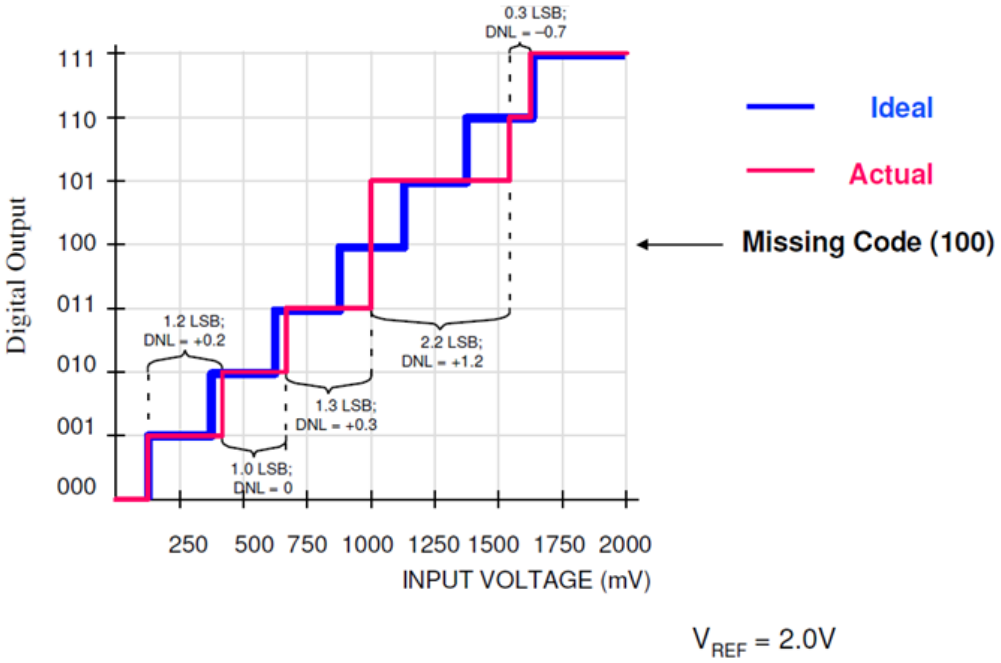

Figure 2.5. Differential non-linearity (DNL) (Nicholas, 2006)

For ideal ADC, the each code transition points are exactly 1 LSB apart. For example 8-bit ADC, these changes are separated from each other by 1 LSB or 1/256 of full scale. The difference between the ideal 1 LSB and the worst case actual input voltage change between output code transitions is called Differential Non-Linearity. DNL can be demonstrated using the transfer function of a three-bit ADC as shown in Figure 2.5. Each input step should be precisely 1/8 of full-scale. In Figure 2.5, the first code transition (from 000 to 001) is caused by an input change of FS / 8 (250mV for the 2 Volt VREF), where FS is the full-scale input. The second transition, from 001 to 010, has an input change that is 1.2 LSB, so is too large by 0.2 LSB. The input change for the third transition is exactly the right size. The digital output remains constant when the input voltage changes from 1000mV to beyond 1500mV and the code 101 can never appear at the output. This condition is called “missing code”. To avoid missing codes in the transfer function, DNL should be greater (more positive) than -1.0 LSB. DNL indicates the deviation from the ideal 1 LSB step size of the analog input signal corresponding to a code transition increment. DNL is a static specification and it relates to SNR which is a dynamic specification. However, noise performance can not be predicted from DNL performance, except to say that SNR tends to become worse as DNL departs from zero.

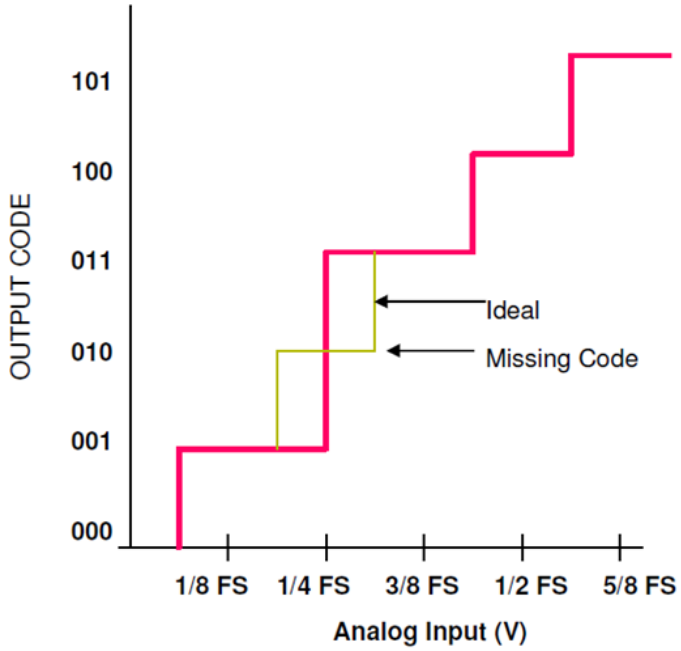

Figure 2.6. Missing code (Nicholas, 2006)

When there is no value of input voltage produces a given output code, such that the certain code never appears in the output, that code is missing from the transfer function and it is known as a missing code. Figure 2.6 shows a missing code example for a 3-bit ADC. The first code transition, from 000 to 001, takes place when the input voltage is 1/2 LSB, which is correct for an ADC. The second transition takes place when the input voltage reaches 1/4 FS, so the differential linearity error at that point is +1/2 LSB. The second transition has a differential linearity error of 1 LSB, causing the output code to jump from 001 to 011, and 010 is a Missing Code. Any time DNL is –1.0, there is a possibility of one or more missing codes. Many ADC data sheets specify “no missing codes” as this kind of specification could be critical in some applications such as in servo systems.

2.1.4 Integral non-Linearity (INL)

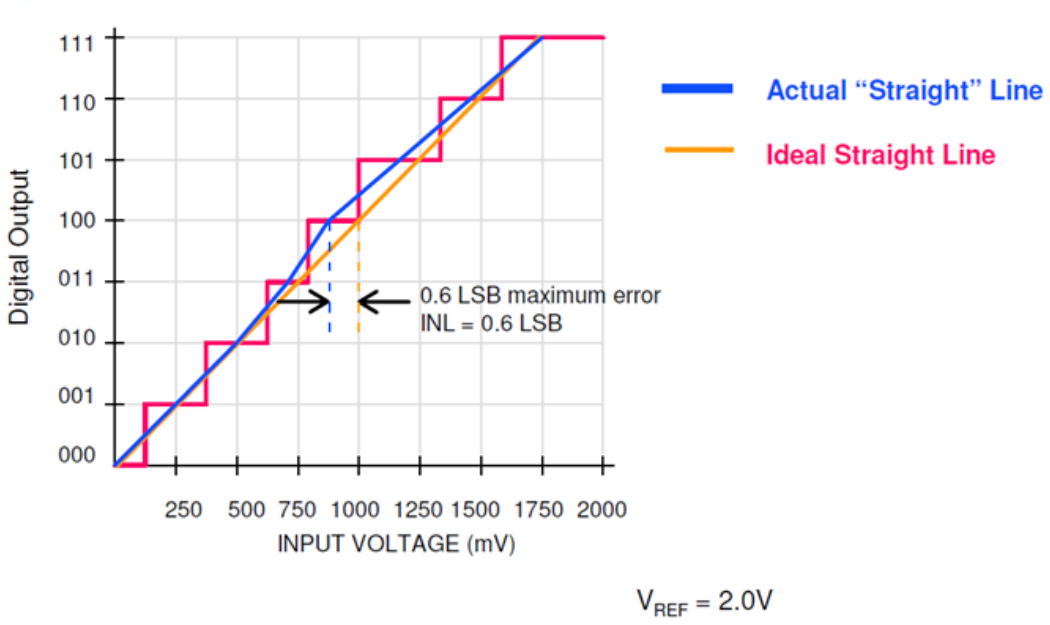

Figure 2.7. Integral non-linearity (INL) (Nicholas, 2006)

Integral non-Linearity (INL) or so called Integral Linearity Error (ILE) describes the departure from an ideal linear transfer curve for an ADC. INL does not include quantization errors, offset error, or gain error. It is a measure of the straightness of the transfer function and can be greater than the differential non-linearity. The size and distribution of the DNL errors will determine the integral linearity of the ADC. Sometimes ADC is described as being "x bits linear". For example, ADC with 10-bit resolution and 4 LSB non-linearity is sometimes described as an "8-bit linear" converter because 4 LSBs for a 10-bit device is equivalent to 1 LSB for an 8-bit device. INL is a static specification and relates to THD (total harmonic distortion). However, distortion performance can not be predicted from the INL specification, except to say that THD tends to become worse as INL departs from zero. Figure 2.7 illustrate INL for 3-bit ADC with VREF=2V.

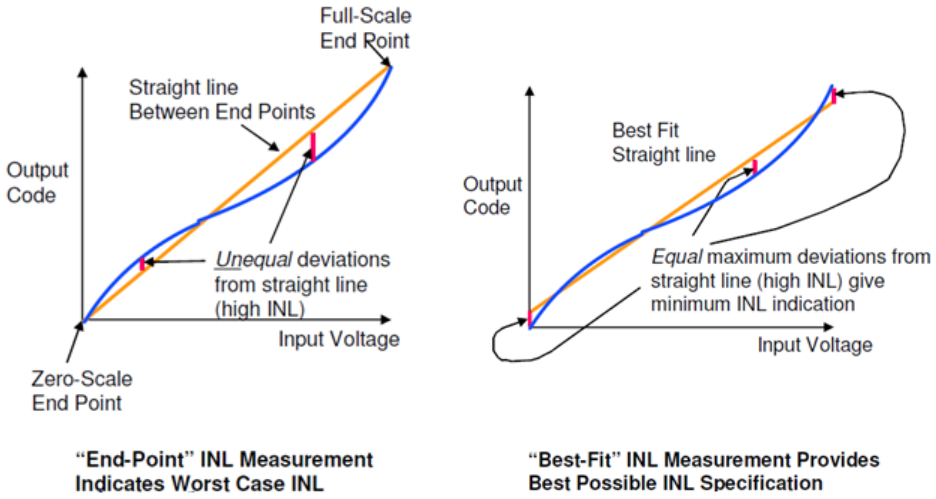

Figure 2.8. INL measurement; (a) End-Point INL; (b) Best-Fit INL (Nicholas, 2006)

Figure 2.8 (a) shows INL measurement using End-Point and Figure 2.8 (b) shows INL measurement using Best-Fit method. End-Point and Best-Fit method are two methods of measuring Integral Non-Linearity (INL). The Best-Fit measurement allows the ADC manufacturers to show better INL specifications than does the End-Point INL measurement method. With Best-Fit method, circuit could be adjusted to actually realize this low INL, achieving better performance. However, by doing circuit adjustment, each board must be adjusted for minimum INL for each individual ADC, which is time-consuming. Therefore, it is expensive and not considered desirable or practical by most ADC manufacturers. Best-Fit method is for dynamic applications only and says that these applications are not very concerned with offset and gain errors (which cause the End Point and Best-Fit INL methods to diverge). If offset and gain errors are very large, the Best-Fit method is more meaningful for these applications. This argument does indeed have some merit for dynamic applications, except they are meaningful only in that they are a better predictor of THD performance, which is usually specified anyway.

The End-Point method specifies worst case INL that could be expected if the adjustment is being made to two end points. Hence, the End-Point method is seen as

more practical by many. Comparing the INL of two competing devices is not reasonable when one device is measured using the end-point method and the other device uses the best-fit method because there is no correlation between the two methods. Generally, ADCs used in d.c. applications should be have INL specified with the End Point method. It does not really matter with which method INL is specified for ADCs used in dynamic applications.

2.2 ADC Sampling Theorem

The Sampling Theorem defines the conditions for signal reconstruction. The Sampling Theorem (Shannon, 1948) establishes the minimum sampling rate for a band-limited signal so that it is uniquely determined by its sampled values F = 2B. Where, Fs is the sampling rate and B is the signal bandwidth. If the Sampling Theorem is observed, the data between the samples can be reconstructed. Aliasing occurs if frequencies greater than Fs/2 are present. If the signal contains high frequency components, the sampling frequency must be at higher rate to avoid losing information in the signal. To be able to recreate a signal from its samples, it should be sampled at a rate higher than twice the highest frequency of interest (Fi). This condition is called Nyquist Theorem and it is always been used for sampling rate to ensure the information contain in the original signal is preserved. Equation 2.2 shows the Nyquist Theorem relationship between sampling frequency (Fs) and signal frequency of interest (Fi).

$$Fs \geq 2Fi \tag{2.2}$$

where

Fs = Sampling frequency

Fi = Signal frequency of interest

When the signal is converted back into a continuous time signal, it will exhibit a phenomenon called aliasing. Aliasing is the presence of unwanted components in the reconstructed signal. These components were not present when the original signal was sampled. Some of the frequencies in the original signal probably lost in the reconstructed signal. Aliasing occurs because signal frequencies can overlap if the sampling frequency is too low. Frequencies fold around half the sampling frequency (Nyquist frequency). Figure 2.9 illustrated aliasing in frequency spectrum when signal sampling frequency is too low.

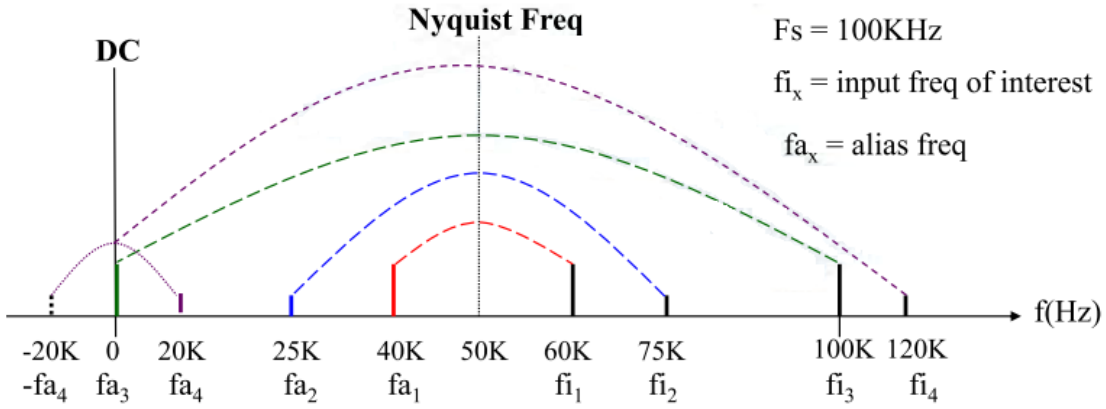

Figure 2.9. Aliasing illustrated in frequency domain

In order to minimize aliasing problem, frequency components greater than Fs/2 must be removed from the signal that is being digitalized. It is achievable by using anti-aliasing filter such as low pass filter. In this research, low pass filter is used inside analog module AV8 and the gain of low pass filter will be determined accordingly. Figure 2.10 shows how the low pass filter (LPF) used to remove signal frequencies greater than Fs/2.

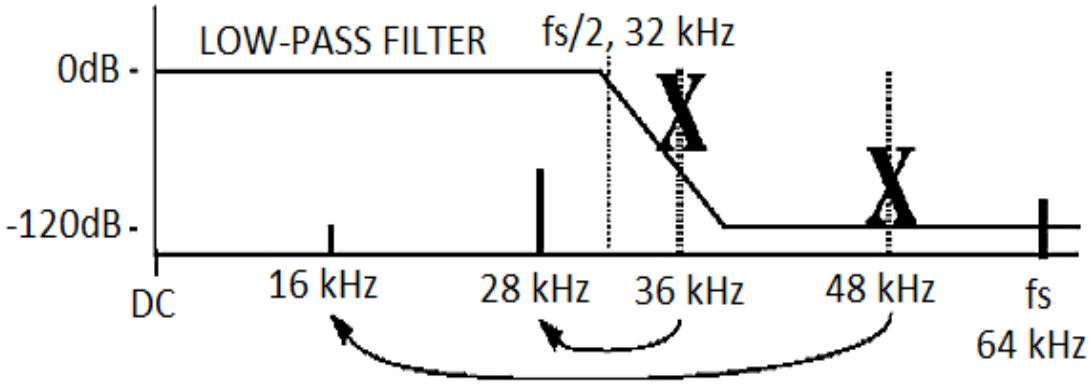

Figure 2.10. Low pass filter (LPF)

The IEEE standard for Terminology and Test Methods for Analog-to-Digital Converters (IEEE std. 1241, 2000) and IEEE standard for Digitizing Waveform Recorders (IEEE std. 1057, 2001) recommend the following five conditions to be satisfied to perform accurate spectral testing. The first condition is that the spectral purity of the input signal to the ADC under test should be about 3 to 4 bits more pure than the ADC. The second condition is to sample the input signal coherently. The third condition is to make sure that the input signal is slightly below the ADC input range. The fourth condition is to have very low jitter between the input signal and clock. Finally, the total data record length should be sufficiently large. It can be noticed that the first four conditions mentioned above are challenging to achieve as the resolution and speed of ADCs keep increasing. Over the decades, work is being done to relax some of the above conditions separately in order to decrease test cost (Siva, et al., 2013). However it is very challenging to work on test cost reduction while the test accuracy is another issue to be handled. This research is focusing on signal coherency condition to preserve the test accuracy. For test time reduction purpose, single tone signal is generated to be used as analog input. For single-tone test cases, the coherent sampling rule is rearranged and repeated to introduce the proposed approach as shown in equation 2.3 (Hari, et al., 2013). The new sampling

frequency, called coherent sampling frequency (Fs) here, is calculated for the desired input test tone (Fin) with predefined values of number of samples (N) and a chosen integer number of cycles of the input signal (M).

$$\frac{M}{N}=\frac{Fi}{Fs} \tag{2.3}$$

where

M = Number of cycles for input signal frequency over which samples are taken

N = Number of samples for sampling frequency

Fi = Frequency of interest

Fs = Sampling frequency

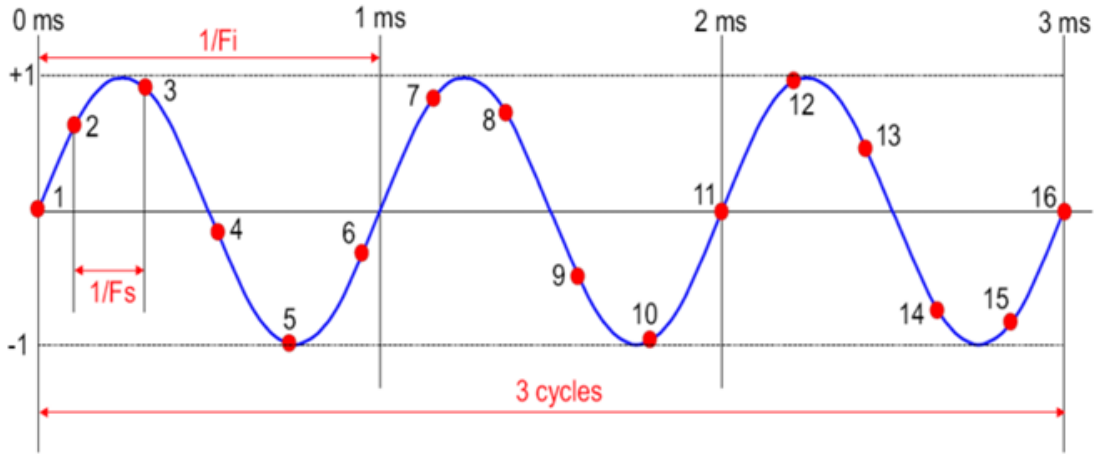

Figure 2.11. Coherent sampling example (Chris, 2011)

Figure 2.11 illustrate the example of input signal with frequency 1 kHz and 16 sampling are being taken over 3 cycles of input signal. Using equation 2.3, sampling frequency, Fs = 5.333 kHz to achieve coherent sampling. There are a few considerations in using equation 2.3 in the balanced ratio of Fi, Fs, M and N. Increasing M and/or N will increase accuracy and test time. M needs to be a whole number to have a coherent waveform (a whole number of cycles or complete full cycles. N has to be a whole number because there is no such thing as half a sample.