NEW CDC DESIGN TOOL FOR ANALOG LAYOUT WORKFLOW

BY

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LIST OF SYMBOLS AND ABBREVIATIONS

A	Cross-section area-dependent constant
ASICs	Application-Specific ICs
BKM	Best Known Method
CAD	Computer Aid Design
CDC	Cartoon Diagram Compiler
CLAMP	Gate Clamp
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
DFM	Design for Manufacturability
DLR	Device Level Router
DSPF	Standard Parasitic Format
DRC	Design Rule Check
E_a	Activation energy for Electromigration
ECO	Engineering Change Order
EDA	Electronic Design Automation
EM	Electromigration
GCN	Polygon
HDL	High-Level Hardware Description Language
IC	Integrated Circuits
ID	IDentification
IR	Voltage
J	Current Density
k	Boltzmann Constant
LCO	Layout Change Order

LVS	Layout versus Schematic
MTTF	Mean Time to Failure
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
N	Scaling Factor
NMOS	Negative channel Metal-Oxide Semiconductor
OTA	Operational Transconductance Amplifiers
PMOS	Positive channel Metal-Oxide Semiconductor
PLL	Phase Lock Loop
RC	Resistance and Capacitance
RF	Radio Frequency
RMS	Root-Mean Square
RTL	Register Transfer Level
RX	Receiver
SDF	Standard Delay Format
SEM	Scanning Electron Microscope
SM	Stress Migration
SPEF	Standard Parasitic Exchange Format
SoC	System on Chip
T	Temperature
TX	Transmitter
VCC	Voltage Collector-to-Collector (transistor)
VDD	Voltage Drain-to-Drain (transistor)
VSS	Voltage Source-to-Source (transistor)

PENYELESAIAN AUTOMASI BARU "CDC" UNTUK REKA BENTUK SUSUN ATUR ANALOG

ABSTRAK

Penempatan dan penghalaan reka bentuk susun atur analog peranti CMOS merupakan proses yang memakan masa dan rumit kerana jumlah penempatan peranti transistor yang banyak, kerja penyusunan peranti dan juga kekangan-kekangan kritikal terhadap susun atur jaringan. Usaha manual untuk melengkapkan reka bentuk susun atur analog mengambil masa beberapa minggu sehingga berbulan bergantung kepada kesukaran dalam kitaran projek yang telah dilakukan. Pada masa kini, pereka perlu menukar peranti daripada skema ke dalam susun atur dalam kanvas editor susun atur, dan kemudian menyusun peranti sewajarnya satu demi satu atau kumpulan dengan kumpulan dengan langkah teratur untuk menyiapkan penempatan peranti. Manakala bagi susun atur laluan jaringan, walaupun terdapat fungsi susun atur automatik dalam alat penyuntingan yang sedia ada, tetapi fungsi ini kebanyakannya dibangunkan untuk reka bentuk digital dan tidak dapat menyusun atur laluan yang tepat terutama apabila terdapat kekangan untuk penghalaan seperti keseimbangan peranti dan pelindungan terhadap medan. Kajian ini membentangkan penyelesaian automasi baru, “Cartoon Diagram Compiler” (CDC) yang membolehkan peningkatan produktiviti ketara dalam proses reka bentuk susun atur analog. Alat ini menyediakan keupayaan untuk meletak peranti transistor / sel contoh dari kanvas skematik kepada rajah kanvas susun atur dan juga berupaya untuk menempatkan secara automatik sel-sel yang tidak kritikal dan peranti dalam mod maya sebelum menukar ke dalam rajah susun atur yang sebenar. Selepas susun pelan lantai atau penempatan memenuhi keperluan reka bentuk, penjana topologi digunakan untuk imbasan segera pilihan susun atur dan sistem sokongan terhadap kekangan (perisai medan) dan kekangan jaringan susun atur. Penempatan peranti dan susun atur jaringan yang diperolehi adalah sepadan atau lebih baik lagi daripada teknik manual. Pretasi “CDC” telah diuji dan dibandingkan dalam reka bentuk susun atur analog projek dalaman syarikat Intel.

Dalam kajian, purata tempoh masa penyelesaian secara manual penempatan peranti dan susun atur jaringan analog memerlukan 640 minit dan 554 minit masing-masing melalui “CDC”, proses penempatan peranti dan susun atur jaringan mermelukan purata tempoh masa hanya 139 minit dan 112 minit atau pengurangan sebanyak 5.14x dan 6.31x masing-masing. Dengan penciptaan CDC, peningkatan produktiviti, pengurangan kerja dan juga masa dapat dijimatkan. Kesimpulannya, peralatan "CDC" meningkatkan produktiviti dengan membenarkan automatik sepenuhnya untuk penempatan dan susun atur laluan jaringan, reka bentuk tambahan dan penempatan pintar menjamin peraturan reka bentuk bebas dari kesalahan.

NEW CDC DESIGN TOOL FOR ANALOG LAYOUT WORKFLOW

ABSTRACT

The placement and routing on CMOS analog layout design had always been a time consuming and irritating process due to large amount of transistor devices placements, arrangements and a lot of critical nets routing constraint. Manual efforts to complete analog layout design took few weeks to months' time in previous project cycle according to the complexity of the circuit. In the meantime, designer needs to convert the devices from schematic into layout in canvas of layout editor, and then arrange the devices accordingly one by one or group by group by moving the devices in order to complete device placement. While for routing, even though there are different auto-routers in existing layout editing tool, but these routers are mostly developed for digital design and unable to route analog signals precisely especially when there are constraints for the routing like matching and shielding. This research presents a new automation solution, Cartoon Diagram Compiler (CDC) tool that enabling a significant productivity improvement on analog layout design. The automation tool provides capability to drag-and-drop the transistor devices/instance cells from schematics canvas to floor planning canvas and is able to auto-place non-critical cells and devices in a virtual mode before converting into real layout. After the floorplan/placement fulfill the design requirement, topologies generator can be used for quick preview of routing option and auto-router support for constrained (shield critical net) and un-constrained nets routing. The area and routing quality nearly matched with hand-drawn layout. The CDC tool has been compare and evaluated on Intel in-house analog layout design projects. In research evaluation, the average time to complete manual device placement and layout routing required 640 minutes and 554 minutes respectively. With device placement and layout routing process only required 139 minutes and 112 minutes or significant reduction in period of about 5.14x and 6.31x respectively. In conclusion, CDC tool increases the productivity by allowing fully

automatic derivation of placement and routing, incremental design updates and smart placement guaranteeing design rule free from violation.

CHAPTER 1

INTRODUCTION

1.0 Project overview

Currently, the analog and mix-signal design play important role on the SoC (system on chip) design. To develop an automated layout generation of advanced technologies for mix signal and analog circuit is still challenging. Though consuming only a small area on the layout, analog circuit involve significant amount of determination and design time. In the digital design, computer-aided design (CAD) tools are equitably well grow and commercially accessible to the design community. However, for mix signal layout design generally rely upon designers' proficiency to ease the influence from process variation beyond transistor level and to achieve outstanding performance [1].

An analog design is basically more difficult than digital layout due to the unique and necessary constraints obligatory on analog layouts. Example of the constraints are types of MOS transistor sizes, sensitivity to parasitic capacitance, crosstalk, device matching symmetry requirements, current density, temperature gradients, piezoelectric effects and electro migration [2] . Layout design of analog circuits is a fallible and time overriding process. In order to reduce the effect of parasitic mismatches, some devices need to be located in near proximity and proportionally with respect to an axis. Without the right placement of the layout, the overall performance of the circuit will be reduced.

Analog layouts routing are mostly routed by analog layout designers due to special constraints are requested from register transistor level (RTL). RTL is a high-level hardware description language (HDL) for defining digital circuits. Current automated routing tools still unable to fulfill this requirement [2]. This is a main disadvantage for mixed-signal designs, where the layout of the analog part can be a highly time-consuming assignment. This also negatively influence the time-to-market for SoC design and application-specific ICs (ASICs). In order to curtail the design effort from the human side, the exertion will advance in computer part by expending the automation involved in the design. The cost time and the time to marker will be reduced by using design automation which capable to reduce the design time spent by layout engineers.

Design automation reduces the design time spent by qualified engineers, thus reducing the cost and the time to market. Digital design has been almost completely automated since several decades. Analog design automation is far from being mature, on the other hand, and is still performed manually. Full-custom designs lead to long design-test cycles, therefore increasing the time to market and the cost [3].

1.1 Problem Statement

An analog layout design automation has a great potential to represent a significant role in the design process of the next generation of mixed-signal integrated circuits (ICs). As the development of worldwide semiconductors market shows a wild growth of integrated circuits, a huge number of analog and mixed-signal circuits are integrated with digital units to accomplish system-on-a-chip. Analog designs regularly requires more development time to implement analog blocks than digital because it required full examination to certify circuit performances. So analog circuits turn out to be blockage in the chip design flow due to the complications in analog layout designs and the lack of support by design automation tools. Although some studies or tools have been proposed for automation layout generation recently, however the degree of automation employ in analog design has never been close to the degree possess by digital design tools [4].

The layout designers converts the devices (transistors, capacitors, resistors, etc.) from the schematic into layout design. Then they have to continue by manual placement and routing based on the constraint requirement [5]. The procedure need to be recurring through verification until clean. After a clean layout has been fulfilled, the parasitic can then be obtained for re-simulation, and the whole cycle needs to be repeated until the simulation results show the required performance has been met. As a result that generating the layout can take days for a typically sized block. This whole flow is too recurrent and far too slow. With the considerations of time-to-market being ever more important, and new processes requiring higher-quality parasitic information as early as possible.

Nowadays designers are facing huge challenge to cut-off design time and time-to-market. In the digital world, automation is well established to enable turnaround of ever bigger designs in a reasonable schedule time. The designers can estimate parasitics premature in the design flow at RTL level by verifying the timing and power criteria [6]. Therefore design requirements are easily met because design changes can be restated relatively quickly in early stage before starting generation.

However the analog world is not same as the digital world, early estimation of parasitics has not been traditionally possible. Circuit simulation is not accurate in predicting performance if lacking of parasitics extracted from real layout[7]. For analog layout, it requires an expert analog layout engineer to take into account the matching of devices and the topologies in order to provide good performance, and they usually have only time to determine one layout topology [8]. So the circuit design and layout are iterative. Therefore layout-dependent effects are hard to estimate, the designer may has to delay days for the layout which is done manually before simulation can extract the actual parasitics once complete. This is obviously not an ideal situation.

1.2 Objectives

This research is to evaluate the time spent for generating the analog layout with employing a new layout design flow for analog custom IC design. The design flow has the following objectives:

1. To reduce analog layout design cycle by introducing automation process
2. To minimize re-spin and “over design” effort in analog design through visual aid
3. To reduce the development time for a good quality analog layout
4. To reduce Design Rule Check (DRC) / Layout Vs Schematic (LVS) violations

1.3 Scopes

This research project scope will focus on the new design flow that is more convenient, in which layout engineers can use to implement more optimum layouts with less iterations and fewer retries conventionally instigated by DRC/LVS violations. In addition, it can be used by circuit designers at an early stage to get earlier, more accurate simulation results from the draft layout which automation tools able to generate by himself and thus reduce iterations before pass to layout designers to generate the real layout. Besides that, it can be used by floor planner to achieve precise estimations of block dimensions and aspect ratios to increase top-level design speed.

This research will start with development of transistor placement automation in a visual aid called "cartoon diagram" before converting into real layout database which will be explained further in Chapter 3. Then, this will be followed by development of auto routing topologies with constraints.

1.4 Thesis outline

The following chapters in the research project thesis will be organized in details. These include introduction, literature review, methodology, result and discussion and conclusion. Chapter 1 is about the introduction of this project. This chapter describes on the project background, followed by problem statement, research objective, project scope and finally the outline of thesis.

Chapter 2 reviews the background of integrated circuit layout and the different between Digital and Analog layout. Besides that, analyses the mutual issues and challenges that confronted by the layout designer when producing high quality analog layout. This chapter would deliver knowledge of existing works of others and relevant fundamental background related to the project. Additionally explore and understand on various available analog layout methodologies.

Chapter 3 describes the methodology of this research project. It will introduce a new custom analog ICs design flow by adding a cartoon diagram compiler between layout process and schematic entry. The layout designers can perform manual or auto placing devices, instances, or arrays from the schematic into the cartoon diagram, the transistors and routing are presented in cartoon view. The designers can simply change the design without worrying about the design rules, connectivity or parameter value. After completing the diagram, the tool will convert into real layout. Lastly, the new CDC tool was evaluated with 17 custom layout cells/blocks by three layout designer.

Chapter 4 describes the results and discussion of this research. This chapter deliberate about the overall time consumed by the layout designer to accomplish an analog layout between new CDC tool and manual way. Comparison of performance of generating the analog layout with CDC tool and manual way have been made and discoursed in this chapter as well.

Lastly, Chapter 5 presents the conclusion of this research. This included the summary of the research and a reiteration of the results of the research. This chapter also contains the contributions and the future works to improve the CDC tool.

Furthermore, the information of analog blocks which used on the research experiment are included in the appendix section.

CHAPTER 2

LITERATURE REVIEW

2.0 Introduction

CMOS ICs are made using a tremendously complex process in which the end results are small transistors and wires being generated and connected on a silicon substrate. Integrated circuit layout, also known as IC layout, is the artwork of drawing these transistors and wires in which they will be appeared physically similar on silicon substrate. Therefore the layout can be assumed as the physical model of circuit. In other way, it also can be stated essentially as three-dimensional character of the elements and interconnections of an integrated circuit. By using computer-aided layout tool to place and route all the components that make up the chip by fulfill all the requirements, which are, density, size and manufacturability [9]. This practice is often partitioned among two main layout disciplines: Analog and Digital.

2.1 Analog and digital layout

There are a lot of similarities among analog and digital layout practices. When the digital systems get very fast in switching speed, it will behave like analog circuits. Besides, the relation between this two field, the use of power plane designs and bypass capacitors are mostly identical. Dissimilar will appear in switching noise and the positions of device on the board [10].

Analog signals enclosed intelligence in phase, amplitude, and frequency. While routing the signals, the layout designer has to be cautioned with nearby signals and structure that can affect the intelligence contained in the analog signal. Some of the signals possibly carry high density of current and travels through a thin metal wire. As the result the atoms of the metal wire migrate along the direction of the electron current, affecting short and open. This common critical issue is known as electro-migration (EM). In addition, analog design also suffer various types of problems. For instance, propagation delay, noise, capacitive coupling, induced signals, modulating currents and voltage drops [11].

On the other hand, digital signals comprise intelligence in the pulse edges which is used to start and stop digital events. However, no intelligence is transmitted in the amplitude or pulse frequency. The operation of the circuit will modify while the shape or position of the pulse edge is changes. The impedance of the circuit board trace develops significant effects to the higher frequency components. Therefore, impedance matching becomes important to avoid reflections of the higher frequency edge components. Other than that, the propagation time of high frequency pulse edges will be influenced by the dielectric resources of the circuit board. Besides that, high amplitude crosstalk in abutting traces or structures can be easily induced by the rate of current change (di/dt) of fast edges compare to analog signals. Since digital signals are well supply in frequency components, usually it have such high exchanging rates at the edges and have greater voltages than analog circuit board analog signals on the same board. Hence, the designers will avoid placing digital signals near the analog signals [10]. The intelligence in adjacent analog signals will falsify by the effects of digital signals.

However, in this day and age, mixed signal circuit (analog and digital signal) show a significant role in system on chip (SOC) industry. So, high current analog signals can also counteract digital signals on the same board. Power supply to the logic generating the edge to dip when an analog peak occurring at the same time as a pulse edge, which causes the digital signal to rise to a lower 'on' state. Besides that, the change in 'on' amplitude will be reflected as a shift in the slope of the pulse edge, which looks like a delay in the pulse edge. This is called 'pulse jitter' and distress timing in the digital circuitry. Thus with this all kind of issues to go through, towards developing a good quality of analog or digital layout is not an easy assignment.

2.2 Traditional manual analog layout flow

In the traditional flow as described in Figure 2-1 [12], the layout designers have to repeat over schematic entry, physical layout, parasitic extraction, and simulation. This flow process has been practiced for many years [13]. The schematic generally holds text notes for constraints. After that, all the constraints info are passed over to the layout engineer to start constructing the circuit. All the devices such as transistors and resistors are then generated in layout based on the schematic design. Next manual placement and routing are carried by conferring to the constraint records. This steps need to be recurrent through verification until clean design is achieved.

The parasitics can only be extracted for re-simulation after a clean layout has been accomplished. This full sequence needs to be repeated until the simulation achieve a good result. With the concerns of time-to-market becoming more significant, and new processes demanding higher-quality parasitic data as fast as possible, manual layout design can be a setback. This traditional design flow is too tedious and far too slow.

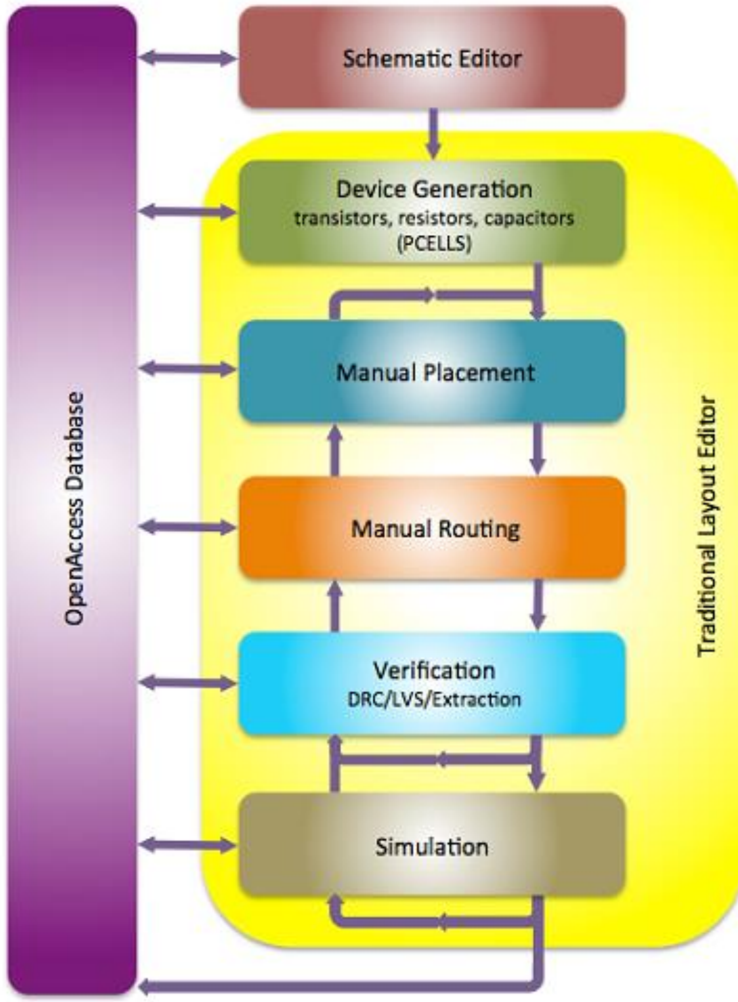

Figure 2- 1 Traditional manual analog design layout flow process [12].

2.3 Parasitic

In chip design, design netlist outlined the logic connectivity and cell instantiations. So for the real electrical connectivity are accomplished by metal wires after the cells are placed. However the current is affected by the resistance and capacitance from the cells and the wires while traveling through them. As a result, the signal propagation timing is affected by parasitic. In order to determine precisely how they impact on signal delay, the parasitic extraction procedure is performed by taking out the exact resistance and capacitance values involved with each metal segment [14].

The photo of real metal and vias formation in a chip is shown in Figure 2-2 [15]. These metal lines and vias consist of resistance and capacitance (RC). When analyzing timing, their effect on signal propagation delay must be taken into consideration. From Figure 2-3, it illustrates a small circuit with one inverter connecting another inverter with the wire interconnection layout. In the same figure, it also shows that the layout is consisted of various metal sections. The metal routings are symbolized by an RC network after the parasitic extraction procedure. In the past, the effect of parasitic resistance and capacitance were not as critical as nowadays due to the process geometry was much larger, meanwhile the signal traveling time was mainly overruled by the cells' delay. However, as chip size continually becomes narrow and more complex, this causes the parasitic delay has increasingly become a main issue [16]. Besides, executing parasitic extraction on full-chip level, it will be more computationally intensive and tedious.

After the parasitic extraction process is completed, the parasitic compression process will be continued in order to condense the information. It is due to the amount of parasitic components on large chips possibly will be massive and the extraction results are not appropriate for being directly used in simulation tools and timing analysis tools [17]. At the present time, the standard parasitic extraction methodology for most chip design is two-dimensional extraction. For more precise parasitic data, the high-performance circuits needed three-dimensional. Standard parasitic format (DSPF) or standard parasitic exchange format (SPEF) are the format for resultant RC network which generated by the parasitic extraction process, which can be converted easily between CAD tools [18].

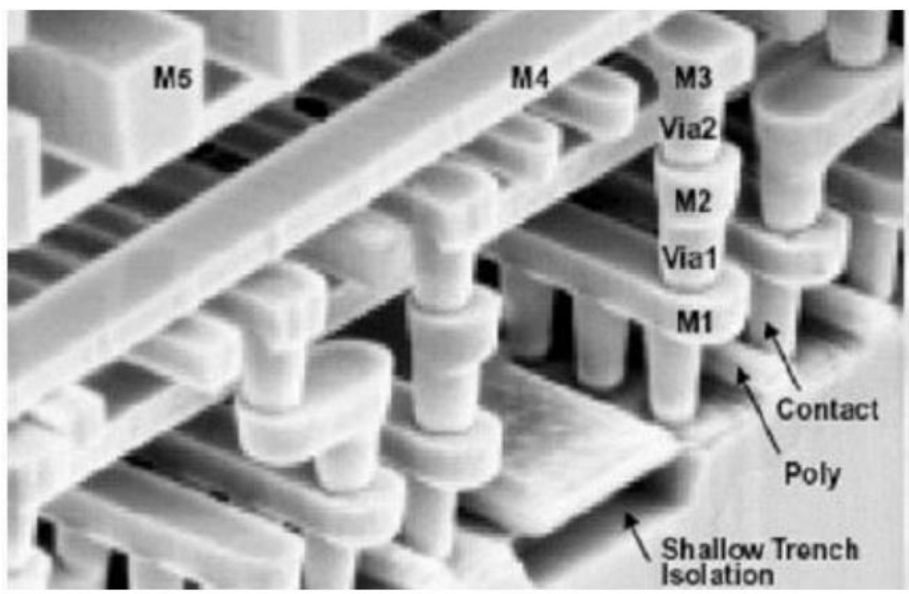

Figure 2- 2 SEM image of Metals and vias structures in a chip [14].

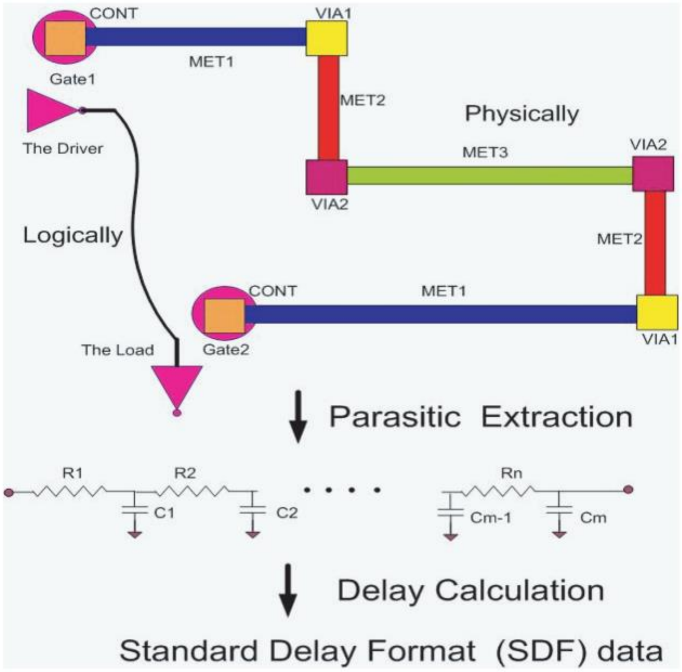

Figure 2- 3 The parasitic extraction process in metals and vias [14].

In order to reduce parasitic problem in early stage, there is a systematic method of optimizing an existing analog layout considering parasitics is introduced for technology migration and performance retargeting [19]. This method represents the locations of layout rectangle edges as variables and extracts circuit and layout integrity such as device symmetry, matching, and design rules as constraints as shown in Figure 2-4. The bounds of layout parasitics are determined initially to validate the required circuit performance. During retargeting existing high-quality layouts through technologies and specification sets, the layout geometries are constrain by the bounds. By combining a graph-based scheme with a nonlinear-optimization technique, effectively resolved the production of a target-layout subject to the entire set of constraints. This methodology has been employed in a parasitic-aware automatic layout optimization and retargeting tool (Intellectual Property Reuse-based Analog IC Layout). The tool successfully demonstrated that retargeting operational amplifiers with efficiency and effectiveness within 1 min of CPU time [19].

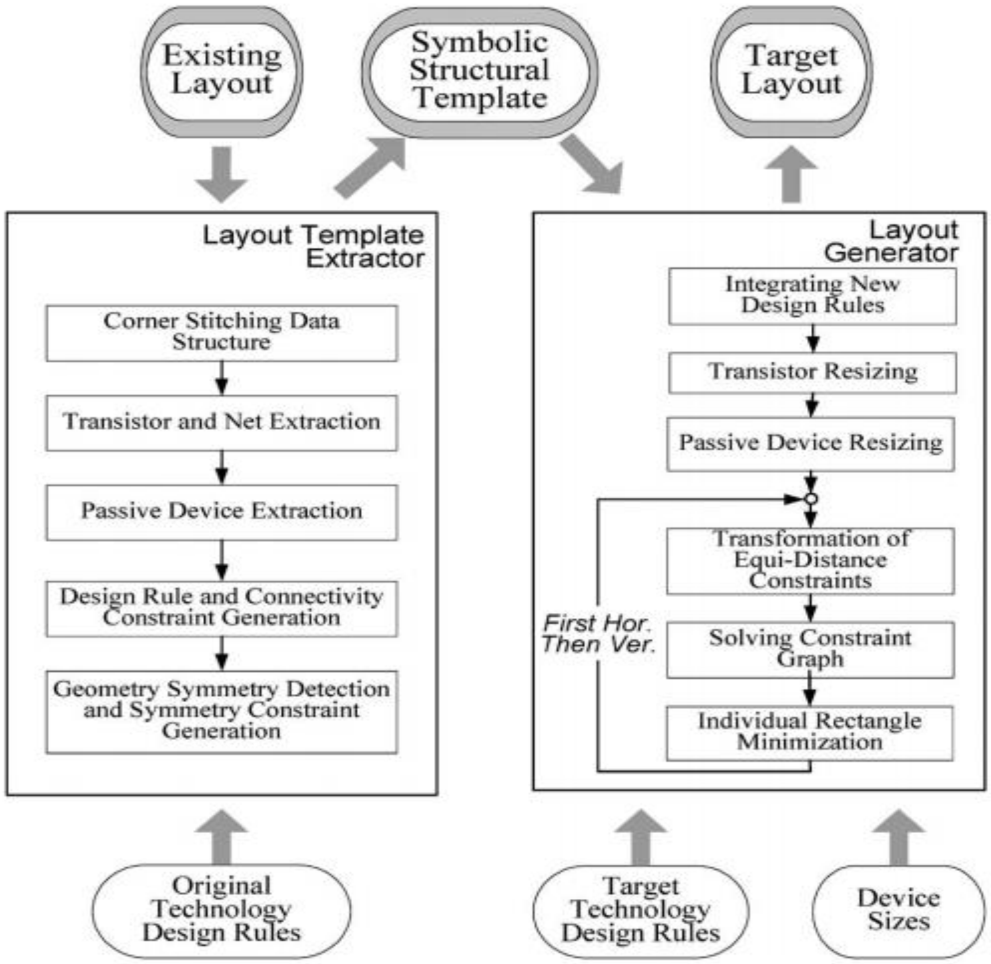

Figure 2- 4 Analog-layout-optimization/retargeting flow [18].

2.4 Voltage/IR (V=IR) Drop

When a current flows through a resistor of a fix resistance value and it cause a voltage drop, this event defines as IR drop. As mentioned in the last topic about parasitic, the routings among the cells are constructed by metal segments of copper or aluminum which are resistors. Therefore, the different electric voltage potentials due to ohm's law: V = IR, as shown in Figure 2.5 [15]. The chip performance will degrades from IR drop phenomena because its negative effect on the supply voltage that the cells obtain. As the current flows deeper and deeper into the chip, the voltages of the power supplies reduce slowly along the power network. Besides that, the sum of voltage deflation is over a certain limit at some locations inside the chip, the cells at those areas could suffer speed degeneration or stop operating completely [20].

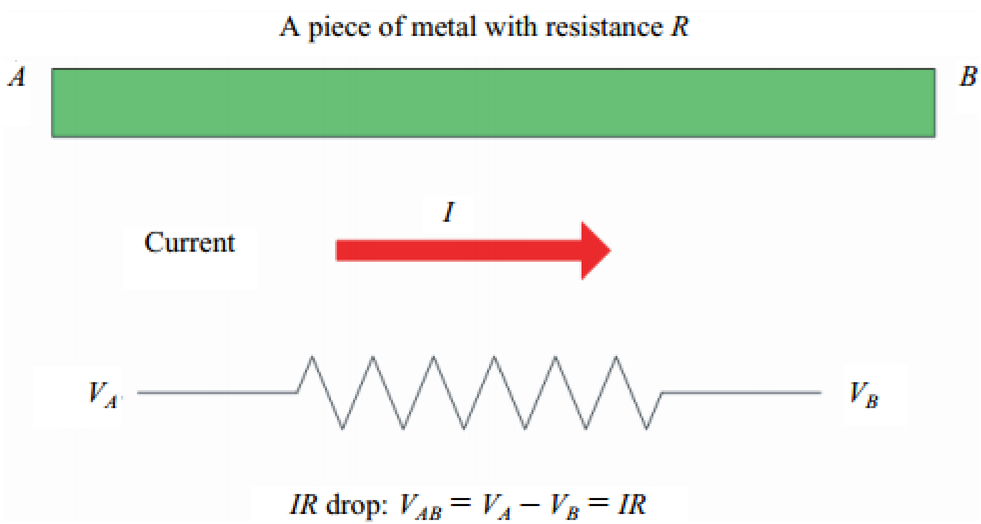

Figure 2- 5 The concept of IR drop in conductor [14].

An example of an IR drop plot in a circuit block is shown in Figure 2.6 [15]. The power supply voltage of this block is 1.1 V and is supplied through the power ports at block's boundary. At the boundary, the dark blue represented the supply voltage is 1.1 V. Then, the voltage level reduces correspondingly while slowly moving into the middle of the block. As shown in the figure, most voltage loss happens at the center of the block due to the IR drop of the VDD bus and it's roughly 5% of 1.1 V. An example of IR drop plot for a real chip is illustrate in Figure 2.7 [15]. Mostly at chip boundary is occupied by voltage and current source. The power pins allow the current flows into the chip that are situated at chip's I/O ring. The voltage potential drops lower and lower when the current slowly moves into the central region of the chip. This is characterized by the area of different color.

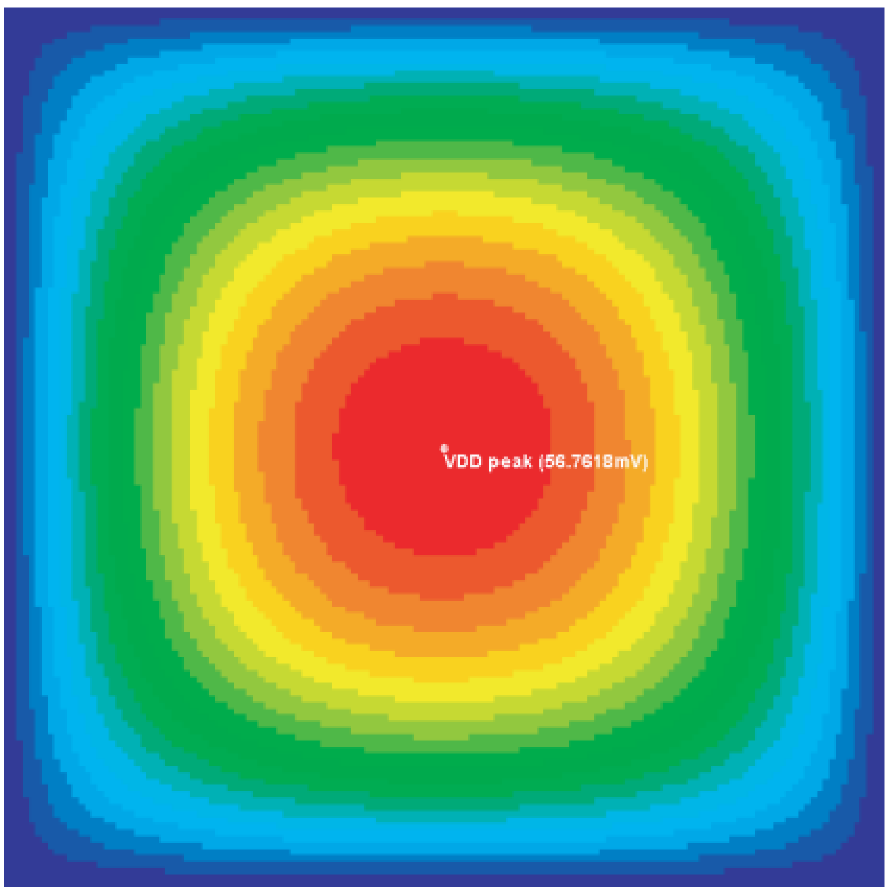

Figure 2- 6 An IR drop plot of a circuit block [14].

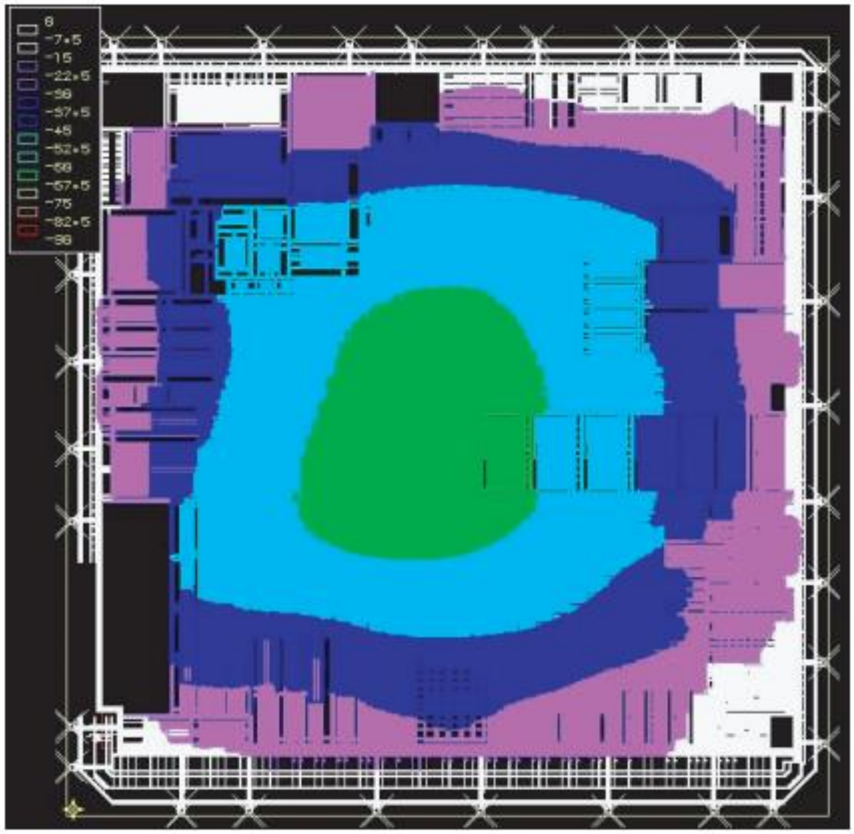

Figure 2- 7 An IR drop plot of a chip [14].

IR drop effect is not as bad problem for signal nets but is a critical issue for power nets [15]. The reason is the signal nets located at the gate terminals of transistors which hold great impendence for a CMOS circuit. So, the currents inside the signal nets are considered low magnitude and the IR drop is minor and can be ignored. However, for the power nets VDD and VSS have high volume of currents are present because of the connectivity at the source and drain terminals of transistors. Furthermore, power nets are on a global scale that links many cells (all of the cells in many cases) not like signal nets. Consequently the current inside the power net is high, and the IR drop issue must be taken into consideration during early design stage [18].

2.5 Electromigration (EM)

Nowadays, electromigration (EM) is a serious issue in ICs [21]. EM is the undesirable transport of material due to movement of ions in a conductor, affected by a transfer of momentum from electrons to these ions. In other words, EM is the regular dislocation of metal atoms in a semiconductor. During the time that the ions flow in irregularity manner, two forms of failures will happen. The first failure is because of a void during the outgoing ion flux surpasses the incoming ion flux, causing in an open circuit as shown in Figure 2-8 [22]. The second failure displays a hillock where the incoming ion flux exceeds the outgoing ion flux, resulting in a short circuit.

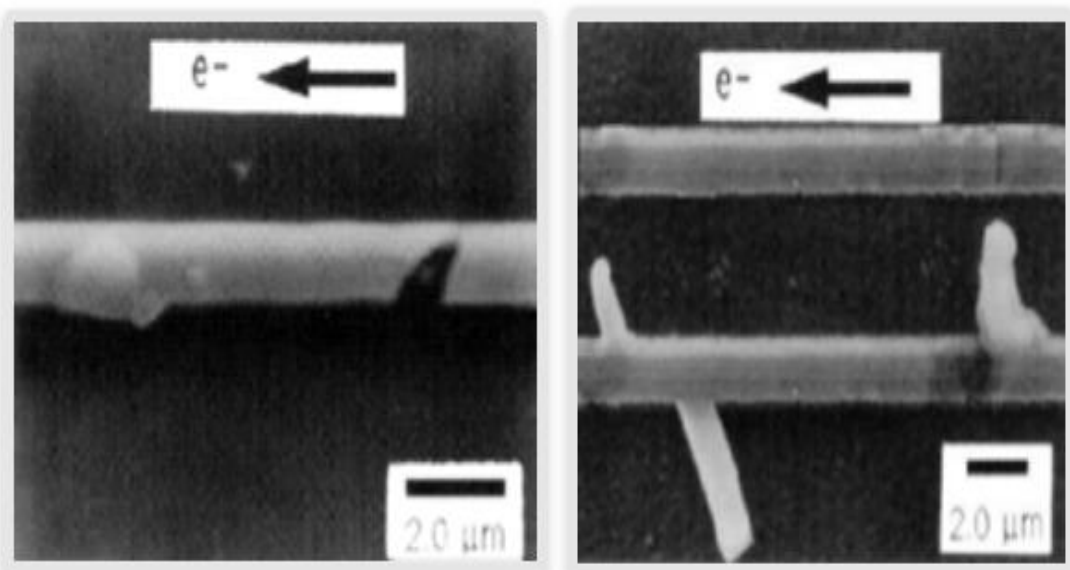

Figure 2- 8 SEM of void (open circuit) and hillock (short circuit) [21].

The EM incident was initially exposed by a French scientist called Gerardin during 1891. When the first commercial MOS IC introduced in 1964, it only became of practical attention. A lot of research events were started in the 1960s, one of the most significant engineering research was achieved by Jim Black at Motorola in 1969 [23]. An outcome of Black's determination was a calculation that is used to define the mean time to failure (MTTF) [24] of a metal wire when subjected to EM effects. MTTF of the interconnect under constant current stress and temperature, subjected to EM affects, is given by Black's equation as

$$MTTF = \frac{A}{J^N} \exp(\frac{E_a}{k.T}) \qquad (2\text{-}1)$$

Where the parameters of the equation are defined as:

A - Cross-section area-dependent constant

J - Current density

N - Scaling factor, usually set to 2

E_a - Activation energy for electromigration

k - Boltzmann constant

T – Temperature

Equation above shows that electromigration is reliant on temperature. Yet, there is a more menacing reliance on temperature that quickens failures due to voids. From Figure 2-9 illustrates a cyclical positive feedback loop that eventually ends in failure. The wire itself turn into narrower at location when a void starts to grow in a metal wire. So that the current density increases while a large current passes a thin metal wire. Consequently, the interconnect temperature rises because of Joule heating. Joule heating is a product of root-mean square (RMS) current. Thus when performing EM analysis, it is important to include RMS current into account. The growth of the void facilitate as the temperature of the wire rise and at the same time an open circuit happens.

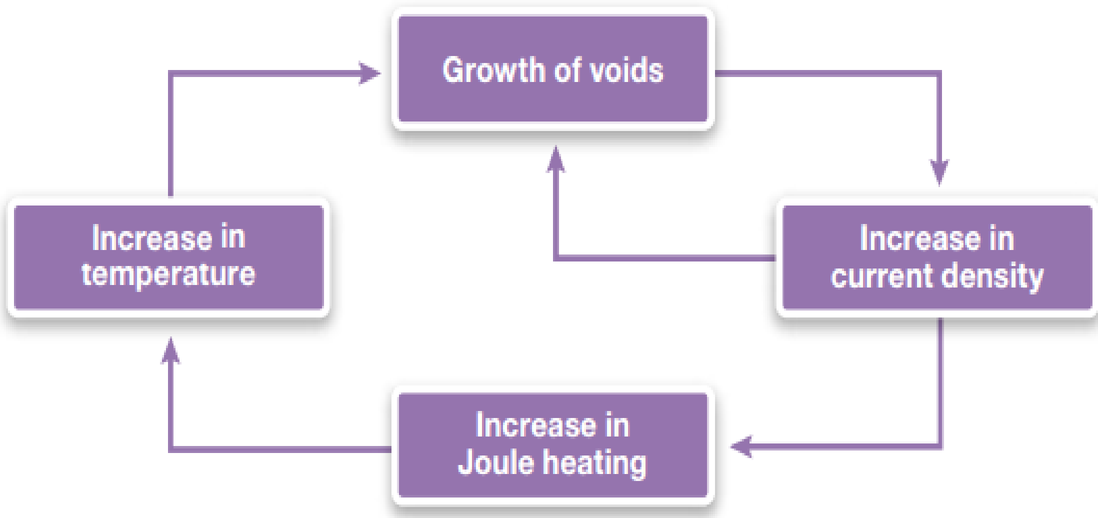

Figure 2- 9 Electromigration reliance on temperature.

Current density is the key factor inducing electromigration. In order to reduce this EM and current density, the wire width has to be increased. However, there is one condition is not applicable to this rule and that is when the wire width drops below the average grain size of the interconnect material. This condition is began by the position of the grain boundaries, which in such narrow wires lie vertical to the width of the whole wire. For the boundary diffusion factor is omitted, and material transport is consistently condensed because of the grain boundaries which also known as “bamboo pattern” are on right angles to the current [25].

Nevertheless, for signal lines of high density currents in analog circuits or for power supply lines with the maximum wire width, the likely for a bamboo pattern is generally too thin. In these conditions, slotted wires are regularly applied, whereby rectangular holes are engrave in the wires. So, the widths of the single metal arrange in between the slots lie within the area of a bamboo pattern, while the subsequent total width of all the metal structures fulfills power necessities.

There is a lower bound for the length of interconnect that will be exposed to the event of electromigration which is known as “Blech length” [26]. For any wire that has a length under this bound will not malfunction by electromigration. Currently, a mechanical stress growth produce a reversed migration process which decreases or constant balance the effective material flow towards the anode. Figure 2-10 [26] illustrated these alleged as “eternal” wires.

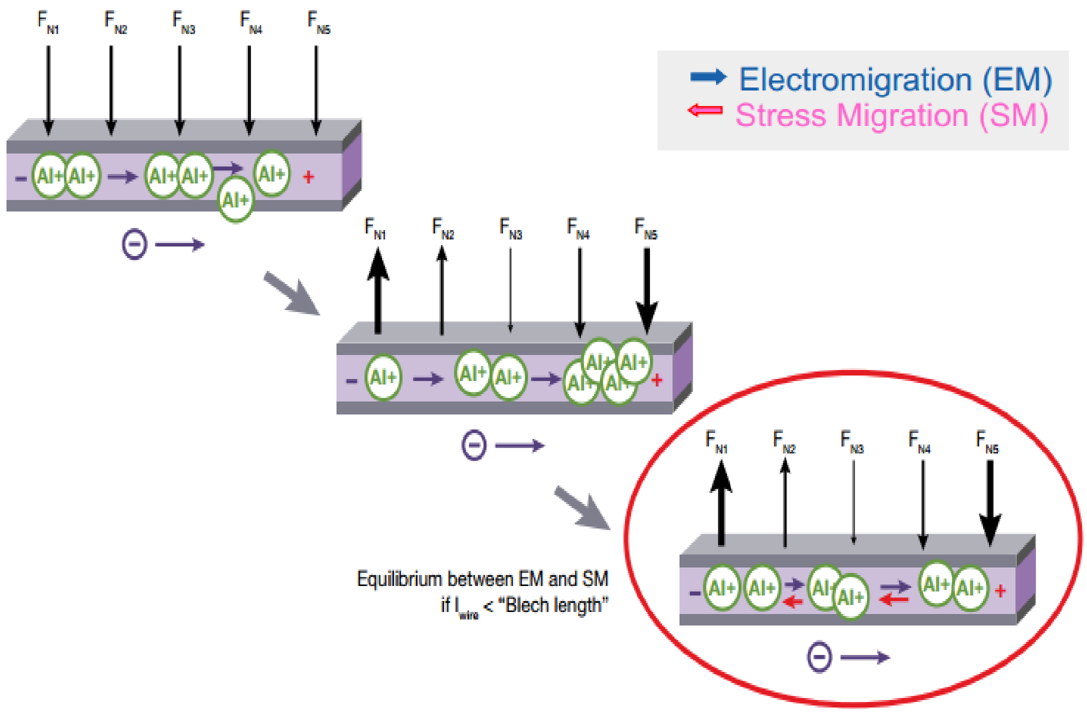

Figure 2- 10 An illustration of stress migration caused by the hillock area in a short wire. This reversed migration process essentially compensates the material flow due to electromigration. [25].

Interconnect layout has an effect on electromigration and current density. EM effect can be reduced by using specific layout strategies to obtain homogenous current flow [27] . From figure 2-11 [26] shows two different layout strategies to achieve homogenous current flow. The left-hand image show that 90° corners and rapid wire width reduction should be evaded. The current congestion and hurried growth in current density can cause serious EM issue. In order to archive homogenous current flow, via arrangement play a significant role in layout strategies as show at the right-hand image of Figure 2-11.

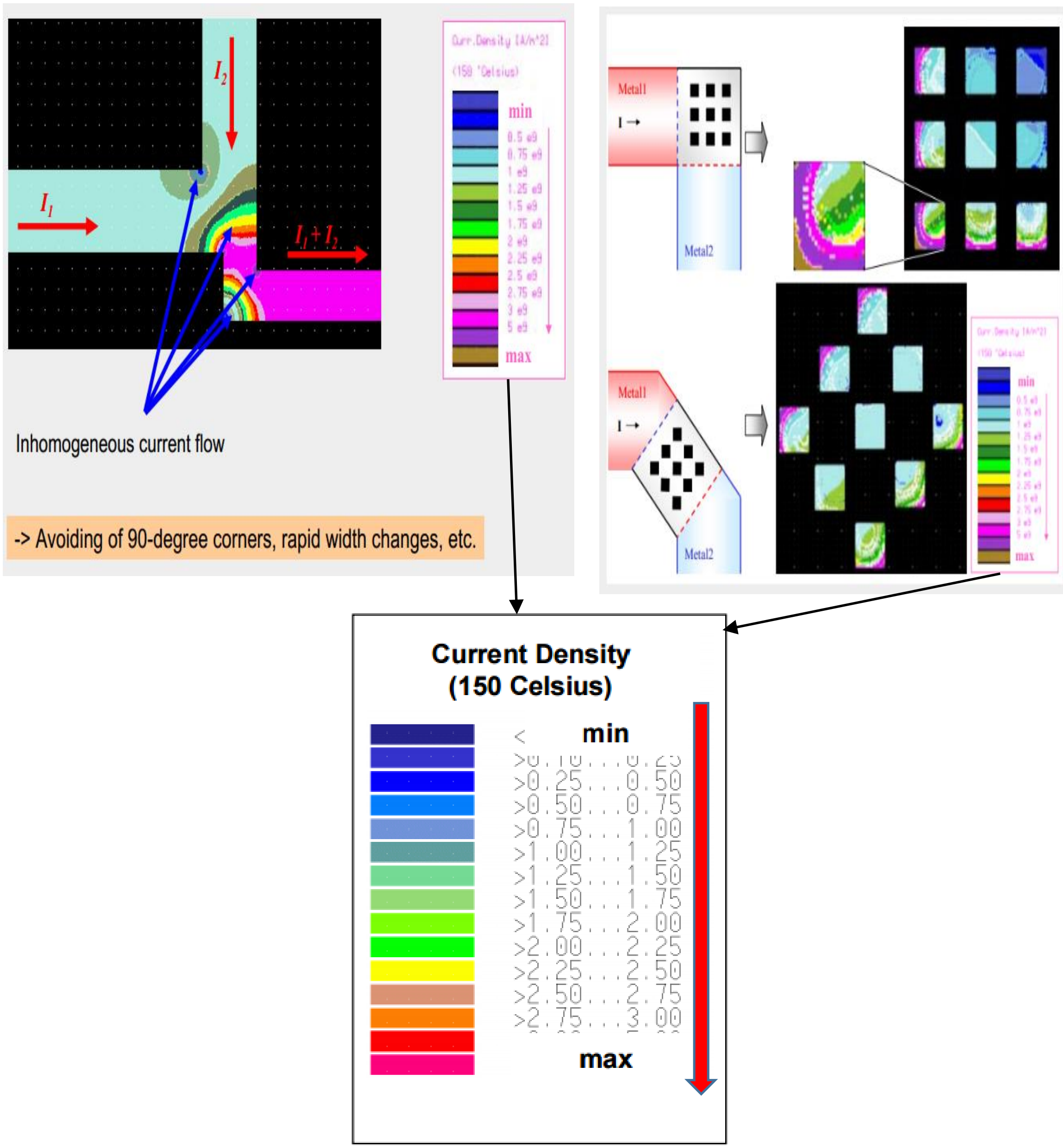

Figure 2- 11 Layout strategies to minimize EM. The left-hand image shown that 90° corners and rapid wire width reduction should be evaded. The vias arrangement played a significant role in layout strategies as shown at the right-hand image [26].

2.6 Eletromigration aware automation tools

As the layout complexity of analog ICs growths, layout designers have to spend more effort in handling with the routing problem to prevent electromigration phenomenon. In order to reduce the design timeline, multiple automation routing methodologies had been explored to aware an EM event [28]. However, there is a lot of constraints need to be taken into considerations while designing a good automation routing for analog design. For example as shown in figure 2-12 [29], the DRC (design rule checking) is violated when a widening wire which is fulfilled the maximum current density passes a narrow channel. But to pass the DRC, thinning the wire width suffers the current density violation.

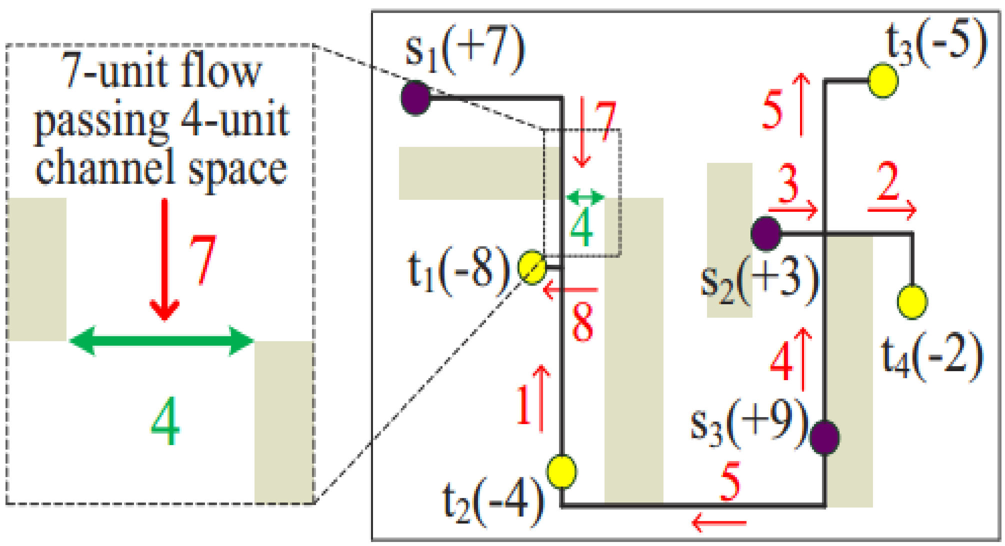

Figure 2- 12 Widening the wire width incurs DRC violation or thinning the wire width incurs the current density limit [28].

In order to avoid this circumstances, one of the method proposed by Yun-Chih et al. is to handle channel space between obstacles by automation routing algorithm [29]. This routing algorithm is able to locate a minimal routing solutions without having violations on DRC and the maximum current density limit. The routing algorithm contains four stages. For the first stage is to build modified spanning graph construction based on [30] with three changes. Next stage is edge encoding and channel space restriction. By encoding the edges of the modified spanning graph in two types: vertex-to-vertex encoding and vertex-to-terminal encoding. In order to support recording paths passing channel and prepare the beneficial info for advance operations. Channel space restriction defines as the space restraint of a channel between two obstacles or between obstacles and the chip boundaries, therefore wires routing through the channel cannot be expanded randomly. The channel space restriction has to be taken into account while routing through a narrow channel. This will prevent the current density increase by restricted wire width and serious electromigration issue or DRC will be violated by unrestricted wire width. So that two kinds of channel space restriction are recommended in their methodology: obstacle-to-obstacle and obstacle-to-boundary channel space restrictions. For third stage is path analyzing and reserved path finding. Path analyzing with channel space restrictions can be examined easily by using the edge encoding method from second stage. Finally, solution path with minimum wire area determination is the last stage of this methodology produced by linear programming to attain an ideal solution.

There are three constraints in the linear programing formulation [29]. The first constraints is to guarantee that each source node and target node satisfies Kirchhoff's current conservation law. Second constraint is to secure that the flow of a wire which routes through a channel cannot be greater than the maximum passing flow of the channel. Third constraint is to guarantees that the flow of each path cannot be greater than the capacity of the path itself. Their research successfully produced a productive automation routing for designing an analog circuits without current density violations and able to achieve optimum solution in practical runtime.