PARTIAL BINARY TREE NETWORK (PBTN):

A NEW DYNAMIC ELEMENT MATCHING (DEM) APPROACH TO CURRENT STEERING DIGITAL ANALOG CONVERTER (DAC)

By

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LIST OF ABBREVIATIONS

ADC	Analog Digital Converter
BTN	Binary Tree Network
CPU	Central Processing Unit
DAC	Digital Analog Converter
DEM	Dynamic Element Matching
DNL	Differential Nonlinearity
FRDEM	Full Random Dynamic Element Matching
GCN	Generalized Cube Network
INL	Integral Nonlinearity
LSB	Least Significant Bit
MSB	Most Significant Bit
PBTN	Partial Binary Tree Network
SFDR	Spurious Free Dynamic Range

ABSTRAK

Penukar Digital Analog (DAC) merupakan segmen penting yang sentiasa digunakan dalam kebanyakan sistem digital yang meyakinkan penukaran data yang tepat. Disebabkan faktor-faktor seperti penggunaan voltan yang semakin rendah, kesuntukan masa untuk kajian, serta keperluan lebar jalur yang meningkat, ini telah menyumbang kepada keperluan model DAC untuk bergantung terhadap komponen yang ditetapkan bagi melaksanakan penukaran data. Penghasilan komponen yang sempurna amatlah susah, kesilapan yang tidak sepadan masih senantiasa berlaku dan menyumbang kepada perbezaan di antara nilai komponen yang diingini dan sebenar.

Pemadanan Elemen Dinamik (DEM) ialah salah satu teknik yang biasa digunakan untuk mengurangkan ralat komponen. Teknik perawakan ini memilih nilai input digital secara rawak sebelum memasuki blok DAC. Ini dapat menyamakan purata masa untuk setiap komponen dan kesan perbezaan komponen dalam litar elektronik dapat dikurangkan. Kelemahan bagi penyelidikan yang sedia ada ialah DAC akan memerlukan perkakasan yang berlebihan dan pengekod yang rumit. Dengan ini, banyak get penghantaran akan diperlukan menyebabkan berlakunya gelinciran.

Dalam kajian ini, algoritma DEM baru yang ingin dicadangkan pada DAC adalah algoritma Rangkaian Pokok Sebahagian Perduaan (PBTN). Algoritma ini dapat menentang gelinciran dengan menggunakan litar elektronik yang tidak rumit. Analisis yang digunakan untuk menyemak pretasi DAC ialah gelinciran kawasan dedenyut, Kamiran Tak-linear (INL), Perbezaan Tak-linear (DNL) dan Penggunaan Kuasa. Kajian ini menunjukkan pretasi yang lebih kurang sama dengan kajian yang sedia ada tetapi mempunyai sekurang-kurangnya 56% lebih kurang perkakasan berbanding dengan kajian yang lain.

Perbandingan pencapaian simulasi untuk 3-bit dan 4-bit PBTN dengan 3-bit dan 4-bit konvensional Rangkaian Pokok Perduaan (BTN) menunjukkan bahawa kedua-dua algoritma telah menghasilkan DNL dan INL yang hampir sama, +/- 0.2 LSB. Lebih-lebih lagi, algoritma yang dicadangkan menggunakan kuasa yang jauh lebih rendah disebabkan jumlah get penghantaran yang digunakan jauh lebih kecil. Pencapaian simulasi bagi 8-bit PBTN dengan 1-bit perawakan ialah 1.5385 LSB dan DNL 0.2605 LSB. Di samping itu, algoritma PBTN menyediakan fleksibiliti untuk meningkatkan prestasi DAC dengan cara meningkatkan bilangan pelaksanaan perawakan pada MSB.

ABSTRACT

DACs are essential operations in many digital system which required high performance data converters. With shrinking of supply voltage, budget constraints of test times, and rising bandwidth requirement causing DAC architectures highly relying on matched components to perform data converters. However, components matched are nearly impossible to fabricate, there are always mismatch errors which caused the difference between the designed and actual component value.

Dynamic Element Matching (DEM) is one of the techniques that are commonly used to reduce component mismatch error. This technique is a randomization technique to select one of the appropriate codes for each of the digital input value before entering DAC block. With this technique, the time averages of the equivalent components at each of the component positions are equal or nearly equal to reduce the effects of component differences in electronic circuits. The drawback of existing works is DAC would suffer from excessive digital hardware complexity. A complicated encoding is usually necessary for conventional DEM encoders which will lead to a lot of switch transitions at the same time and it will bring glitches to the output signal.

In this research, a new DEM algorithm is proposed on Current-Steering DACs with Partial Binary Tree Network (PBTN) algorithm to overcome glitches transitions with low complexity. The analysis related to the performance of DAC such as glitch impulse areas, Integral Nonlinearity (INL), Differential Nonlinearity (DNL) and power consumption are shown to be equivalent and have at least 56% hardware efficient implementations compared to exiting DEM algorithm.

Simulation results for 3-bit and 4-bit PBTN compared with 3-bit and 4-bit conventional Binary Tree Network (BTN) show that both algorithms are equivalent in performance with DNL and INL errors of +/- 0.2 LSB and the proposed algorithm has even lower power consumption due to small amount of transmission gates used. Simulation results for 8-bit PBTN with 1MSB randomization achieved INL of 1.5385 LSB and DNL 0.2605 LSB with power consumption of 22.2 mW. Besides that, PBTN algorithm provides the flexibility to improve the DAC performance by increasing numbers of randomization implementation on MSB.

CHAPTER 1

INTRODUCTION

In real world, most of the analog signals such as temperature, pressure, sound, or images are converted to digital signals that can be easily processed in modern digital systems. In many systems, this digital information must be converted back to an analog form to perform some real-world function. The circuits that perform this step are digital-to-analog converters (DACs), and their outputs are used to drive a variety of devices such as loudspeakers, video displays, motors, mechanical servos, radio frequency (RF) transmitters, and temperature controls (Douglas, 2013). DACs are often incorporated into digital systems in which real-world signals are digitized by analog-to-digital converters (ADCs), further with processed, and then converted back to analog form by DACs as shown in Figure 1.

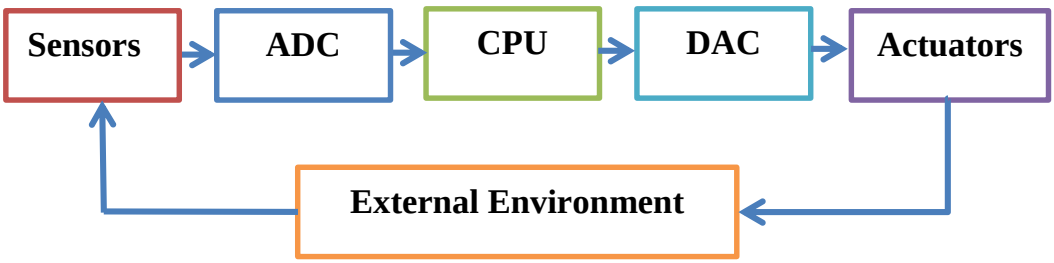

Figure 1-1: DACs in real world function

DAC are essential operations in many digital system which required high performance data converters. With shrinking of supply voltage, budget constraints of test times, and rising bandwidth requirement causing DAC architectures highly relying on matched components to perform data converters. However, components matched are nearly impossible to fabricate, there are always mismatch errors which caused the difference between the designed and actual component value.

Uncertainties in lithography and etching errors, contact resistance and process variation cause deviations of resistors ratio from the desired value (SHIGEO, 1982). Moreover, temperature gradients across the circuit, alignment error, component aging and component noise could cause component mismatch. One of the examples of

components mismatch is alignment error due to different amount of channels connected to C1 and C2 as shown in Figure 1-2. On Figure 1-2 top, fix dummy channels are added to C2 as a mirror design geometry to C1 which causes alignment errors in capacitances. By improving the circuit in Layout design perspective, after adding dummy valves S4 and S5, it reduces possible mismatch between C1 and C2 as shown in Figure 1-2 bottom. (F. Yu1, 2013).

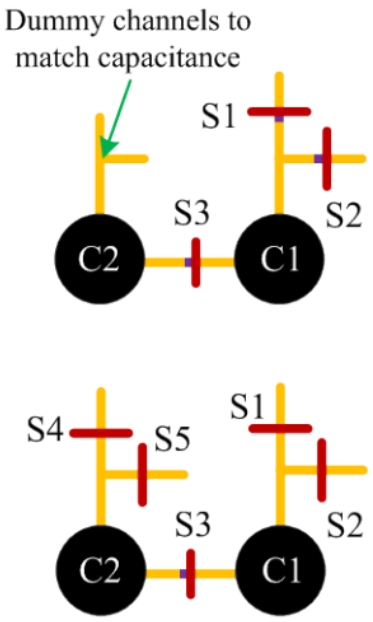

Figure 1-2 Channel mismatch on C1 and C2

Several techniques are introduced to reduce the effects of components mismatch errors. There are special VLSI layout techniques, laser trimming, self calibration, error cancellation and dynamic element matching. Technique introduced in this research is Dynamic Element Matching technique with new methodology which is Partial Binary Tree Network algorithm.

Dynamic Element Matching (DEM) would randomly select one of the appropriate codes for each of the digital input value before entering DAC block. The advantage of this technique is to reduce the effects of component differences in electronic circuits so that the time averages of the equivalent components at each of the component positions are equal or nearly equal (Bruce, 2000).

The connection of DEM with DAC is shown in Figure 1-3. 1-bit DACs of which the outputs are summed together to yield the desired analog output value. There will be several possible codes giving the same output value.

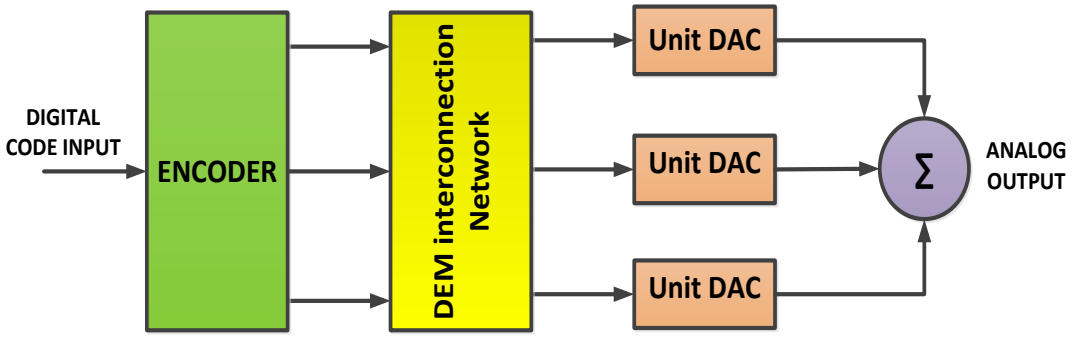

Figure 1-3 DEM Interconnection Network in DAC

There are a large variety of DEM DACs have been proposed and published with different methodology and application to further improve the performance of DACs. One of the papers proposed a 6-bit current steering DAC with Binary Tree Structure Random DEM Technique which shows that DAC with DEM is able to produce better (0.26 LSB) DNL and (0.45LSB) INL compared to DAC without DEM (Guangliang, 2012). Besides that, 8-bit DAC with Partial Randomization Dynamic Element Matching (Olga, 2012) had proven that DAC with DEM have average DNL% error 2 times reduced and average INL% error 3 times reduced from DAC without DEM.

1.1 Problem Statements

Many DAC architectures rely on matched components to perform their tasks. In practice, circuit's mismatches or imperfections elements are inevitably introduced during circuit fabrication, which are defined as the difference between the designed and actual component values. As a result, DAC can degrade a signal, so a DAC should be specified with insignificant errors in terms of the application.

As mentioned earlier, several techniques are introduced to reduce the effects of components mismatch errors. There are special VLSI layout techniques, laser trimming, self calibration, error cancellation and dynamic element matching. However, most of the techniques were either expensive in fabrication or large in size.

Special VLSI layout techniques can reduce resistor mismatch errors caused by high varying contact resistances. Over the years, great efforts have been made to the study of mismatch and layout strategies (Lovet, 1998; Chengming, et al., 2004). One of the techniques used to avoid these problems is that the resistors are interconnected without leaving the resistors layer to avoid current path contacts (Reimund, 1995). This kind of connection is insensitive to alignment tolerance of the contacts. However, the requirement of silicon area could be increased depending on the matching characteristic.

Laser trimming is another technique that can reduce the mismatch error in resistors. Trimming is a post-fabrication circuit adjustment aimed at correcting the process-induced offsets of various components. Resistor values can be changed by removing resistor material with a highly focused laser beam at the wafer stage. Although with laser trimming the physical dimensions of a resistor string after fabrication can reduce mismatch errors, the procedure is expensive (Vishal, 2006).

Another technique that is commonly used to reduce the mismatch error is Dynamic Element Matching (DEM). This technique allows many possible input codes that introduce error with randomization technique to select one of the appropriate codes for each of the digital input value before entering DAC block. With this technique, the time averages of the equivalent components at each of the component positions are equal or nearly equal to reduce the effects of component differences in electronic circuits (Bruce, 2000).

Interconnection networks are commonly used for DEM algorithm in DACs. A large variety of DEM DACs have been published with different properties and applications and the circuits proposed in the literature are shown to be equivalent and have hardware efficiently implemented based on multistage interconnection networks (Bruce, 2000; Rombouts, 1998; Chan, 2008; Olga, 2012).

However, the drawback is DAC would suffer from excessive digital hardware complexity. A complicated encoding is usually necessary for conventional DEM encoders, which will lead to a lot of switch transitions at the same moment in high-speed applications (Wei Su, 2011) and it will bring glitches to the output signal of the converter like full random DEM encoder (Henrik,1998).

In this research, DAC architecture that was considered is Current Steering DAC which is the most commonly used architecture for high speed application. Besides that, a new DEM algorithm is proposed on Current-Steering DACs with Partial Binary Tree Network (PBTN) to overcome glitches transitions with low complexity compared to full random DEM and conventional DEM encoders. The analysis was on the performance criteria of DAC such as glitch impulse areas, Integral Nonlinearity (INL), Differential Nonlinearity (DNL) and power consumption which are shown to be equivalent and have hardware efficient implementations based on well understood multistage interconnection networks.

This approach will only increase or decrease the selected number of current sources unit randomly at the same time in order to minimize the switch transitions.

1.2 Objectives

The main objectives for this research are:

- To design less complexity DACs using current steering methodology to generate high-frequency signals.
- To improve dynamic performance of DACs with PBTN DEM algorithm to overcome glitches transitions which minimize the switch transitions.
- To evaluate the proposed method with DNL, INL and power consumption value by comparing with conventional DEM methods.

1.3 Scope of research

The scope of research covered the design, implementation and evaluation of a DAC. A new algorithm of PBTM DEM is established in this phase. The proposed methodology was designed using Cadence Virtuoso. 4-bit PBTN DEM DACs and 4-bit conventional BTN DEM DACs were designed for comparison. 8-bit PBTN DEM DACs were designed to further identify the performance of PBTN in higher resolution DACs. Simulation using Cadence Virtuoso was undertaken to compare DNL and INL performance between 4-bit PBTN DEM DAC and 4-bit BTN DEM DAC. Besides that, the performance and effectiveness of 8-bit PBTN DEM DACs were also evaluated.

1.4 Summary

This chapter is an overview of the research which includes the introduction of the research to understand the background of the research, highlighted the problem statement of mismatch component impacted on the performance of DACs, the objective of the research to come out with a new algorithm and the scope of research to give an overall flow of the research.

Chapter 2 is Literature Review where different types of DACs are introduced to identify the suitable DACs to be chosen to meet the design requirement. Besides that, the architectures of DEM are reviewed and the needs of DEM interconnected with DACs are identified. Measurement metrics for DACs performance are introduced in chapter to verify the methodology to evaluate the performance of DACs. Based on the literature review survey, the requirement of the research is established.

Chapter 3 is Methodology which discussed the design of 4-bit PBTN DEM DACs and 4-bit conventional BTN DEM DACs as a comparison. 8-bit PBTN DEM DACs are designed to further identify the performance of PBTN even for higher resolution DACs.

Chapter 4 is Result and Simulation. The performance of 4-bit PBTN DEM DAC and 4-bit BTN DEM DAC in terms of DNL, INL, power consumption and glitch impulse area are discussed. Besides that, the performance and effectiveness of 8-bit PBTN DEM DACs is evaluated in this chapter.

Chapter 5 is Conclusion to summarize and evaluate the result achieved in this research. Besides, future work to further improve the proposed method is discussed.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Digital to Analog Converters (DACs) are interface circuits between analog and digital domains. DACs are used to drive a variety of devices such as loudspeakers, video displays, motors, mechanical servos, radio frequency (RF) transmitters, and temperature controls. However, digital-to-analog conversion can degrade a signal, so a DAC specified should be insignificant errors in terms of the application. To eliminate pulse shape, timing and amplitude errors arising from component mismatches as sources of nonlinear distortion in high resolution DACs, Dynamic Element Matching (DEM) as a randomized technique is implemented in this research. DACs performance metrics to be observed are Differential Nonlinearity (DNL), Integral Nonlinearity (INL), and glitches impulse area and power consumption of the whole circuit. This chapter is an introduction to provide relevant background information.

2.2 Digital to Analog Converter (DACs) Architecture

DAC produces a discrete step analog output in response to a binary digital input code. Example of a 3-bit DAC is shown in Figure 2-1. There is a variety existing DAC architectures exist, ranging from simple to complex. The digital input may be in any one of a number of codes: binary, BCD, thermometer code, Gray code, sign-magnitude, two's complement, offset binary and so on as shown in Table 2-1 (Jacob, 2010). To generate the output, a reference quantity either a voltage division or current steering is divided into binary and/or linear fractions. Then the digital input drives switches that combine an appropriate number of these fractions to produce the output. The number and size of the fractions reflect the number of possible digital input codes, which is a function of converter resolution or the number of bits (N) in the input code. For N bits, there are 2^N possible codes. The analog output of the DAC output is the digital fraction represented as the ratio of the digital input code divided by 2^N times the analog reference value,

$$A_O = \frac{D_i}{2^N} \; x \; R_{ref}$$

Where,

A_O is the analog output

D_i is the digital input code

N is the number of digital input bits (resolution)

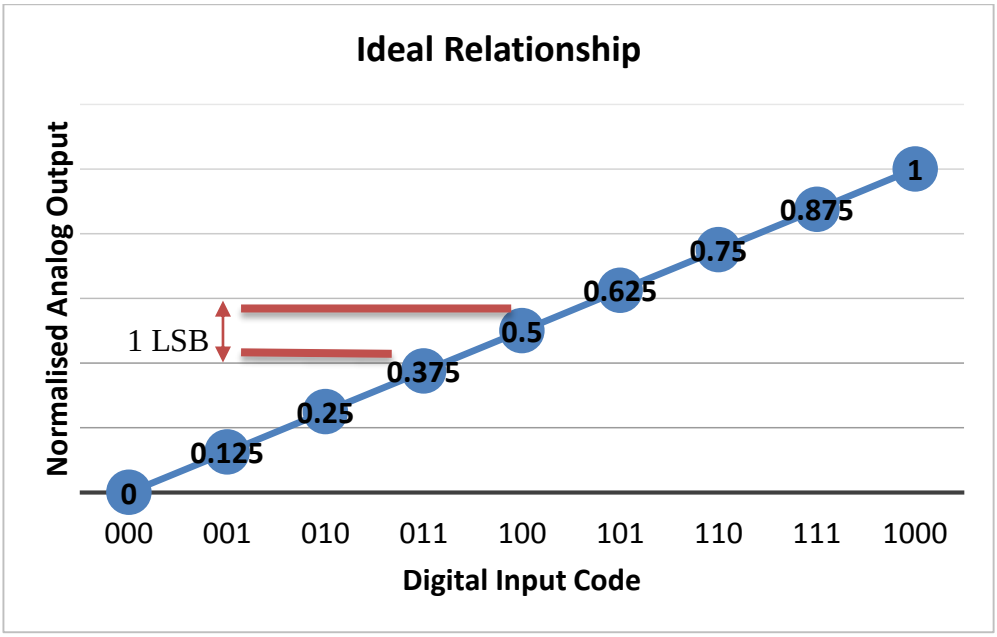

Figure 2-1: Ideal relationship between Digital input code and Fractional Value for 3-bit DAC

Table 2-1: Comparison of digital input codes

Decimal	Binary	Thermometer	Gray	2' Complement
0	000	0000000	000	000
1	001	0000001	001	111
2	010	0000011	011	110
3	011	0000111	010	101
4	100	0001111	110	100
5	101	0011111	111	011
6	110	0111111	101	010
7	111	1111111	100	001

2.2.1 Resistor string DACs

There are many types of DACs available, to name a few, they are Resistor String DAC, R-2R Ladder DACs, Current Steering DAC, thermometer-coded DAC, and hybrid DAC.

One of the most basic DAC is resistor string DAC also called Binary Weighted DAC which composed of resistor string of 2^N resistors connected in series and switches as shown in Figure 2-2. The analog output is the voltage division of the resistors at the selected tap. This implementation is easy to design and implemented but for only small digital input. Therefore this type of DAC usually limited to 8-bit resolution or less Below listed 3 main disadvantages of resistor string DACs for higher resolution:

i. Digital to analog conversion rate is slower due to the existence of large parasitic capacitance.

ii. A large chip area is needed to accommodate large resistor value and large number of passive components needed.

iii. Accuracy of the resistors become a concern as well due to higher tolerance when big resistor value is used which affect the output linearity.

2.2.2 R-2R Ladder DACs

R-2R Ladder DAC is an improvement of resistor string DAC as shown in Figure 2-3 which creates each value with a repeating structure of 2 resistor values, R and 2R. This improves DAC precision due to the ease of producing many equal matched values of resistors or current sources. However, the speed of conversion is slower due to the parasitic capacitance as well.

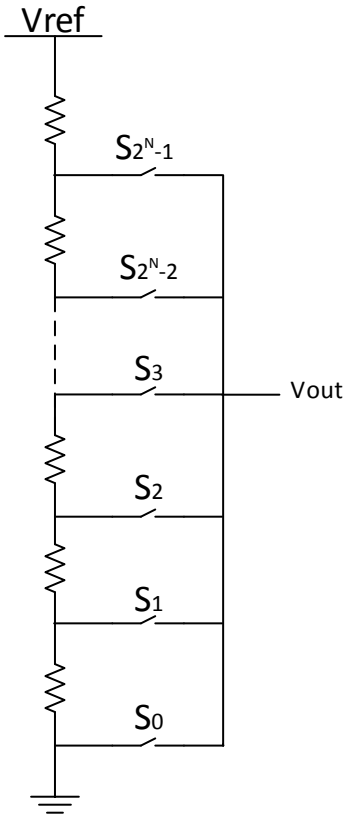

Figure 2-2: Simple Resistor String DAC

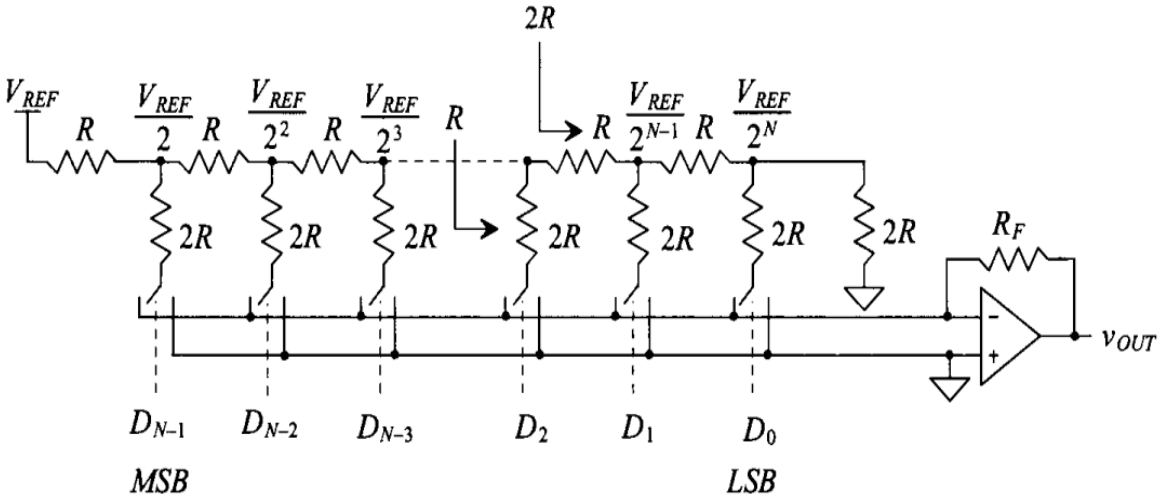

Figure 2-3: R-2R Ladder DAC

2.2.3 Current Steering DACs

Current steering digital-to-analog converters (DACs) composed of current sources which use current throughout the conversion. Each of the sources is connected with a switch controlled by the input digital codes. Current steering DACs is commonly used for generating high-frequency signals as it can achieve high sampling rate compared to voltage switches method because a reference current is not interrupted and only a significant voltage appears at the output but not across the switches (AB-AZIZ, 2009; Hnatek, 1967; Wei-Hsin, 2011) Hence, this architecture is frequently used for wideband communication applications.

A generic current steering DAC shown in Figure 2-4. This method shows there are $(2^n - 1)$ current sources needed and the input digital code is in the form of thermometer code. This architecture is the fastest and highest precision architecture DAC which improve INL and DNL. The drawback is large hardware is needed for decoder and if there are higher bits of DAC was designed, there would be a significant amount of current sources would be needed.

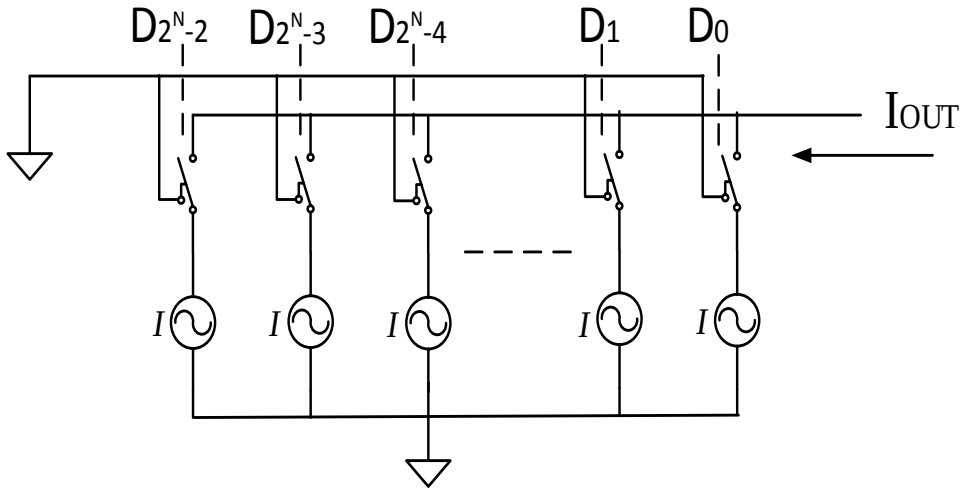

Figure 2-4: Generic Current Steering DAC

There is another type of current steering architecture using binary weighted current source shown in Figure 2-5. Binary weighted current steering is smaller in size due to thermometer encoder is not needed for this architecture. However, the ability of current

sources design can be matched to binary weighted is critical to determine the resolution of DAC.

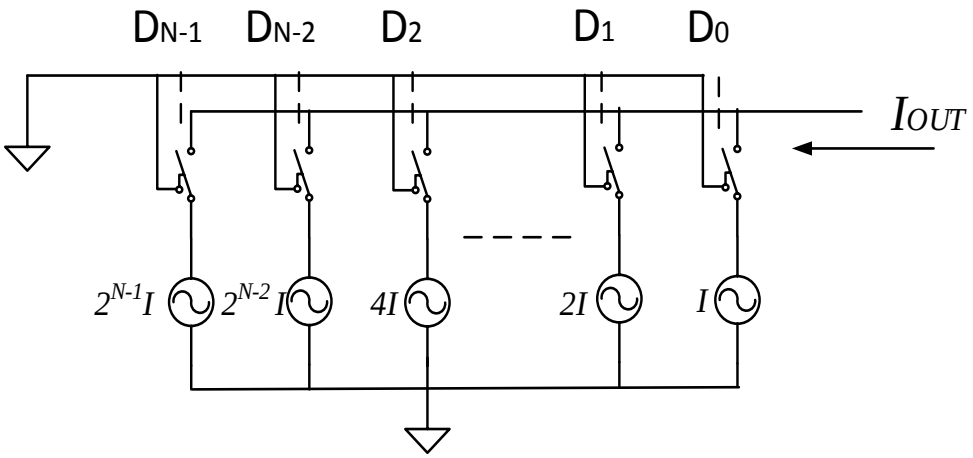

Figure 2-5: Current Steering DAC using binary weighted current source

2.2.4 Pulse Width Modulator DACs

Pulse-width modulator (PWM) DAC is the simplest and powerful DAC in micro-controller. It generates a DC voltage with reasonable ripple after passing through a RC low-pass filter as shown in Figure 2-6. This type of DAC usually used in electronic motor speed control that contained a stable current or voltage.

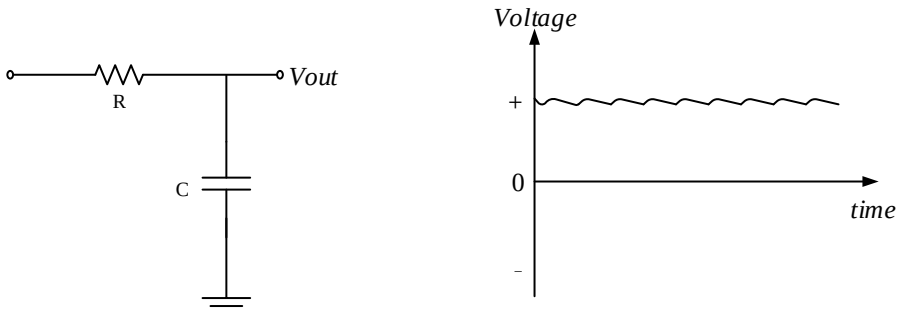

Figure 2-6: Pulse Width Modulation (PWM)