MODELING OF VERTICAL SIDE CHIP INTERCONNECT TECHNOLOGY FOR 3-DIMENSIONAL PACKAGING

by

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LIST OF ABBREVIATION

IC	Integrated circuit
Si	Silicon
SoC	System-on-Chip
3D	3-dimensional
VSCI	Vertical side-chip interconnection
SAB	Surface activated bonding
TSV	Through silicon via
MID	Mobile internet devices
Gbps	Gigabit per second
VLSI	Very large scale integration
HFSS	High frequency structure simulator
CMOS	Complementary metal oxide semiconductor
2D	2-dimensional
PCB	Printed circuit board
IO	Input/output
UBM	Under bump metallization

PEMODELAN TEKNOLOGI SALING HUBUNG TEGAK SISI UNTUK PEMBUNGKUSAN 3 DIMENSI

ABSTRAK

Pada era pengecilan ini, teknik pengecutan nod teknologi digunakan untuk meningkatkan prestasi peranti. Walaupun begitu, kaedah ini menjadi semakin rumit disebabkan oleh had saiz atom Silikon di dalam teknologi pengecilan rekabentuk litar bersepadu. Tambahan lagi, teknik isyarat juga memainkan peranan yang penting untuk menentukan keseluruhan prestasi sesuatu peranti. Oleh itu, kajian ini meneroka konsep yang berinovatif, iaitu teknologi Saling Hubung Tegak Sisi (VSCI) untuk pembungkusan 3 dimensi (3D) di dalam meningkatkan prestasi litar bersepadu. Ciri-ciri elektrik seperti galangan tidak sepadan, perlindungan gangguan, kehilangan isyarat elektrik telah dikaji bagi mendapatkan struktur optimum VSCI. Struktur optimum dari segi lapisan susunan cip telah dibincangkan dengan memberi trend orientasi isyarat TSV, nisbah isyarat TSV dengan bumi, dan kesan kedudukan isyarat kepada keseluruhan kualiti isyarat. Juga kajian tentang kepekaan saluran penamatan pada teknologi VSCI telah dilakukan. Perbandingan dengan teknologi tradisional litar bersepadu 3D seperti teknologi pateri benjolan dan aktifan ikatan permukaan juga telah dikaji. Trend pembukaan tinggi mata; salah satu parameter isyarat yang penting telah dianalisis berdasarkan panjang saluran penghantaran, masa naik kemasukan isyarat, kemuatan pada peranti penerima dan factor rintangan penamatan. Data diperolehi menunjukkan kebolehlaksanaan teknologi Saling Hubung Tegak Sisi sebagai salah satu kaedah alternatif untuk mencapai prestasi elektrik yang setimpal dengan model pateri benjolan dan aktifan ikatan permukaan

pada kadar pemindahan 100Gbps. Keputusan simulasi juga menunjukkan potensi penyelesaian teknologi Saling Hubung Tegak Sisi untuk penamatan penerima yang lemah untuk mencapai pembukaan tinggi mata melebih 350mV (berdasarkan 1V punca voltan) pada 30Gbps.

MODELING OF VERTICAL SIDE CHIP INTERCONNECT TECHNOLOGY FOR 3-DIMENSIONAL PACKAGING

ABSTRACT

In this miniaturization era, previously, shrinking the technology node was used in order to maintain and improve the electrical performance of a device. However, this method is getting difficult due to the limitation of Silicon (Si) atomic size of the material in designing the integrated circuit (IC). Moreover, the signaling techniques play a crucial role in determining the overall performance of a device. Thus, this thesis explores an innovative concept of vertical side-chip interconnection (VSCI) for 3 dimension (3D) packaging to improve the performance of IC. The electrical performance of the proposed vertical side-chip stacked package is discussed in order to optimize the structure of VSCI. Optimization of VSCI structure is based on stacked die package application with the trending of through silicon via (TSV) signal orientation, TSV signal to ground ratio and TSV signal pitch impact to the overall signal integrity performance. Then, this thesis had underscored the electrical performance of the aforementioned stacked die packages from signal integrity perspective in terms of impedance matching, noise shielding and electrical losses. Then, the sensitivity study of channel termination on vertical side-chip interconnection (VSCI) was carried out. The conventional 3D integrated system with solder bump and surface activated bonding (SAB) technology also was investigated as comparison with VSCI. The trends of eye height opening and one of the critical signaling parameters were analyzed based on transmission channel length, input rise time, receiver device capacitance and termination resistance

factors. Finally, full wave simulation using 3D electromagnetic field solvers and transient analysis results showed the feasibility of VSCI as alternative method to achieve comparable electrical performance with the conventional solder bump and SAB interconnection models at 100Gbps transfer rate. The simulation results showed potential solution space of VSCI for weak receiver termination to achieve more 350mV eye height opening (based on 1V supply voltage) at 30Gbps.

CHAPTER 1

INTRODUCTION

1.0 Introduction

In the late of 1965, the most widespread term “Moore’s Law” which coined by Caltech professor, Very Large Scale Integration (VLSI) pioneer in reference to a statement by Gordon E. Moore was the sequel of the collaborative interaction between quantum physic, electrical engineering and materials science. Generally, Moore’s Law describes the number of transistor which can be inexpensively placed in an IC are roughly doubles every 18 months. Every aspect of human life which covered from communication, transportation, publication, and entertainment are immensely improved either directly or benefited from the effect of its influences.

However, shrinking the technology node which had been applied for over few decades in accordance to Moore’s Law is getting more difficult for conventional planar IC to keep track on improving the device’s electrical performance. A complete digital system is composed by three main components: driver, interconnect, and receiver as shown in Figure 1.1. Performance of a given device or system is determined by how well the signal had been transmitted and the received signal quality at the receiver part. Generally, device (transistor) delay which is mainly occurred at the both driver and receiver part, and interconnect delay which is contributed by the whole interconnect

data path were the key factors to determine the overall performance of a device. The scaling technology which had been used was to boost up the device performance by reducing transistor delay. However, few difficulties were faced like complexity of the design and limitation on physical structure of the material which believed will hit the atomic size of silicon (Si) by keep applying this scaling technique. Moreover, Amdahl's Law stated that overall performance of the system is determined by the slowest unit in the system (K. C. Chillara et al, 2011). Undeniable, interconnect delay is higher compared to device delay at Deep Submicron Technology (DSM) nodes because of drastically increased in integration density while keep reduce the device area. Higher integration density had loaded the global interconnect delay compared to the device delay. Global interconnect delay which included related issues like power consumption and signal integrity are more pronounced in scaling technology and device delay like intrinsic gate delay is considerable decrease through faster and smaller area of devices (V. F. Pavlidiset al, 2005). The scaling technology focuses on reduce the device delay by developing techniques like tapered buffer, repeater insertion, wire sizing, and guard shielding at both circuit level and layout design (R. Chandel, et al 2005). Abovementioned techniques were increasing the silicon area and power consumption though device delay was improved.

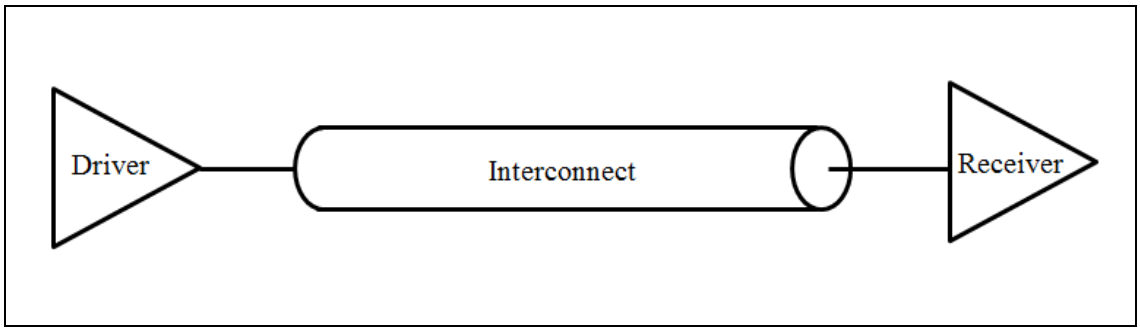

Figure 1.1: A complete Transmission Line Model for a digital system.

Consequently, the three-dimensional (3D) package technology, an alternate way for the multi-gigabits devices solution is introduced and continuously gaining much momentum due to the high demand on advanced digital devices like smart-phone, PC tablet, digital camera and mobile internet devices (MID) in terms of their functionality, performance and affordable costs of ownership. The 3-dimensional (3D) packaging technologies exploit the third or Z height dimension to provide a volumetric packaging solution for higher integration and performance.Moreover, the flexibility on interconnect and die stacking of the structure had offer significant reductions in interconnection length and lead to decrease of global interconnect delay. Thus, it became as an enabling technology option for high bandwidth device applications.

1.1 Problem Statements

In this miniaturization era, device's sizing is as emphasized as the overall device's performance and functionality. Previously, shrinking the technology node was used in order to maintain and improve the electrical performance of a device. However,

this method is getting difficult due to the limitation of the integrated circuit (IC) physical size and atomic size of the material. Furthermore, the design bottleneck of a high speed device was fall at the interconnect delay part rather than the intrinsic gate delay which can be improved through node shrinking technology. An alternate solution,3-dimensional packaging conceptwas introducedin order to cater the problems while miniaturize the physical size of a device. The 3-dimensional (3D) packaging conceptcovers the development of System in Package (SiP), Package on Package (PoP), and Through Silicon Via (TSV) technology.Numerous studies were carried out to study the signal integrity (SI) of 3D package technology through the years. (Pulici et al, 2009) showed the design flexibilities of System in Package (SiP) and the challenges of 3-dimensional package technology was described in (Corbalan, M.Met al, 2013). Although the 3D packaging technology aimed to reduce the size and weight of a device which enables higher degree of design freedom and improve electrical performance through shorter interconnect delay, it still limited to the number of stacked die that directly proportional to the density of the device (Matsuura et al, 2006). With the increase number of die that stacked vertically upward, it will increase the z-height of the device and lead to longer interconnect length and delay.

A finer technology, Vertical Side Chip Interconnect was proposed where the die was stacked vertically and extended laterally by utilizing the four surface sides of current 3 dimensional package technologies. The current research aims to reduce the z-height of a device and improve the global interconnect delay that enabled to the higher electrical performance. The principle of the design was extra dies were connected

laterally through the four surface sides of the main block to create a highly form factor 3-dimensional package. By employing this technology, the total z-height and global interconnect length of a stacked die design can be reduced by half while maintaining the comparable electrical performance (B. E. Cheah et al, 2011).

1.2 The Research Objectives

The signal integrity of 3-dimensional package technology was limited to the number of stacked dies that affecting the density of a design. Thus, this research is to achieve the following objectives:

i- To study the electrical performance comparison between solder bump interconnection model, surface activated bonding interconnection model, and vertical side-chip interconnection model.

ii- To investigate the electrical performances of the proposed vertical side-chip interconnection model by analyze the optimization effort and sensitivity of the termination on signal channel.

1.3 Project Contributions

This research was expected to address an alternate solution for high speed design by fully adopt the 3D packaging and integration technology. The proposed

model, VSCI exhibited comparable electrical performance with the current package technology models.

1.4 Scope of Project

The aim of this research is to study the electrical performance of newly proposed Vertical Side Chip Interconnect technology. The scope of this study was adopted from the following four major techniques:

i- Result and solution was performed based on electronic design automation (EDA) tools.

ii- Relation electrical performance study of the eight stacked dies with solder bump interconnection, surface activated bonding (SAB), and VSCI technology.

iii- Optimization effort on VSCI technology by assessing the different signal to ground ratio, pitch, and orientation.

iv- Sensitivity of channel termination on VSCI technology.

1.5 Structure of Thesis

This thesis is organized into 5 chapters and it begins with the research introduction and followed by research background that consists of problem statement,

research objectives, and the scope of this research. The rest of the chapters were discussed briefly as follows:

i- Chapter 2 (Literature Review) introduced the basic concept of 3D packaging and integration which covered the TSV technology. Moreover, signal integrity on high speed links which employed in this work were discussed in detail.

ii- Chapter 3 (Methodology and Implementation) illustrated the approaches to get the final output result began from the modeling method until the simulation setup.

iii- Chapter 4 (Results and Discussion) contained the overall results, starting from the signal integrity evaluation, optimization effort, and followed by the sensitivity of channel termination of VSCI technology.

iv- Chapter 5 (Conclusions and Future Works) summarized the findings and data as presented in previous chapter especially on the VSCI technology and pinpoint a few of suggestions for future work.

CHAPTER 2

LITERATURE REVIEW

2.0 Introduction

The chapter introduced the basic concept of 3D packaging and integration which covered the TSV technology. Moreover, signal integrity on high speed links which employed in this work were discussed in detail.

2.1 Basic Concept of 3-Dimensional Packaging and Integration Technology

3D integration and packaging technology is without question the hottest topic in microelectronics today. An effective solution for integrating similar or dissimilar chip had been released by employing this technology. At the same time, it was an emerging technology that can form highly integrated systems by vertically stacking and connecting various materials, technologies and functional components together (J.Q. Lu et al, 2007).

Traditionally, CMOS technology was designed based on 2-dimensional (2D) planar architecture and integrated into a single layer of die. Each die is individual assembled and placed on a planar interconnect substrate, mainly printed circuit board (PCB) to form a complete system (E. Beyne, 2006). Moreover, it also provides a

mechanical support and interconnection between different dies and components. However, this technology is suffered on the system size, input/output (IO) density, and interconnects of the channel length due to the limitation of its physical structure. By using this 2D technology, the area-package efficiency (die to package ratio) is typically low (P. Asimakopoulos, 2011). Besides that, the signal is easily distorted when it travel through the long interconnect channel length which is lossy in nature. This is because the long interconnect channel length will lead to higher wire parasitic and propagation delay.

Unlike 2D planar architecture, 3D integration provides more motivation and benefits in order to meet the end user demands which included high functionality, small form factor and high performance. A 3D integration of integrated circuit is defined as multiple dies are stacked, vertically interconnected and integrated on a share common package (J. U. Knickerbocker, P. S. Andry, B. Dang, et al., 2008). The signal and power of the stacked dies are travelled vertically to device strata through short interconnect like flip chip, and TSVs. The innovation of the third dimension is using multiple layers of silicon substrate to arrange in a stacked configuration in which each layer containing transistors with different functionality. Similar to the conventional chips, the interconnect routing covered the planar surface of the each substrate, but also tunnel directly through layers in a vertical as shown in Figure 2.1.

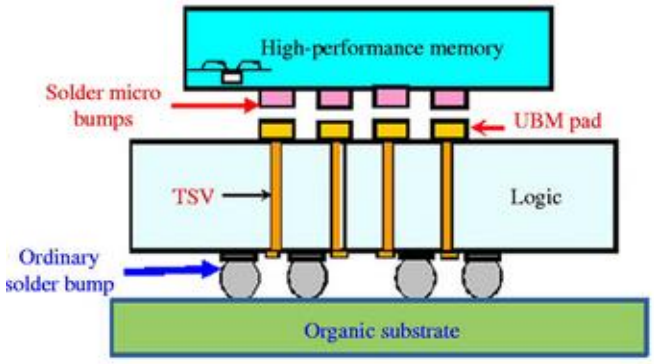

Figure 2.1: General view and outlook of through silicon via (TSV) and 3D integration (E. Beyne, 2006).

The significant advantages of 3D integration compared to 2D planar architecture are providing power efficiency, increased bandwidth interconnection and reduced latency operation (J. U. Knickerbocker et al, 2008). Generally, the length of the interconnect channel or wire is directly proportional to the global interconnect delay and power dissipation. Figure 2.2 shows 3D integration provides shorter interconnect channel length compared to 2D integration due to the flexibility of its stacked configuration. Instead of make a long route in 2D planar circuit, 3D integration provide shorter channel length by vertically connect 2 different dies. Hence, the total interconnect channel length is reduced and lead to the improvement of interconnect delay and power dissipation of the device.

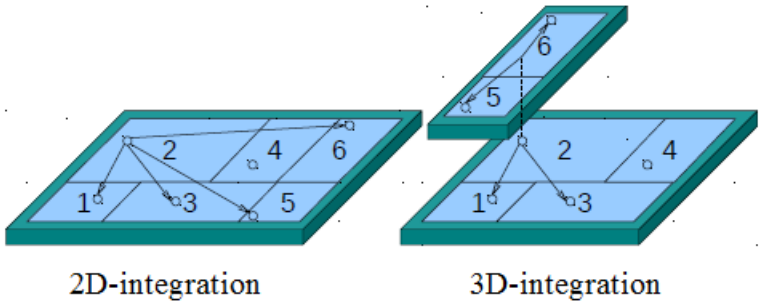

Figure 2.2: Channel length interconnection comparison between 2D integration and 3D integration (P. Asimakopoulos, 2011).

In general, there were three major types of 3D stack technology were emerged, wire-bonded chip stacks, package on package, and package in package. Although these approaches offer flexibility on known good dies testing, it caused long interconnection length and limitation on the interconnection among chips. There were few under development approaches for the chip stacking technology, chip to chip stacking, chip to wafer stacking and wafer to wafer stacking. Each of the approaches has their own benefits and limitations. High precision flip chip bonding is the common way to perform chip to chip and chip to wafer integration. Often, the die sizes will be different and heavily depend on their functionality and the density. For example, die sizes of a high density flash memory is different sizing with a low density flash memory or a normal microcontroller. Thus, these approaches are suitable to stack multiple known good dies in layers (C. Scheiring et al, 2004). However, these approaches are time consuming especially when the chips are bonded as arrays on a wafer. This is because the process has to be repeated as many times as the number of laminated chips in the array and if precise alignment accuracy is required, the process time for stacking each

layer increases further (T. Fukushima et al, 2007). As a result, these approaches will lead to higher cost due to the low throughput at the fabrication side. In another said, these technologies can be used when high yield or dies of different sizes are needed for 3D integration (K. Sakuma et al, 2008).

In the other hand, wafer-to-wafer integration technology may provide an ultimate solution for the highest manufacturing throughput if high yield and a minimal loss of good dies and wafers can be realized (R. J. Gutmann et al, 2004). By applying this technology, it had to rise up the current production yield as much as possible. Moreover, it required a strict control on the diameter size of the wafer so that each layers can be aligned with minimal tolerance. As a result, this causes the material and geometries become complex to handle due to the mismatches of thermal gradients between stacked wafers that lead to the displacement during their bonding process. The total yield of 3D integration using wafer to wafer technology is determined by multiplying the yield of each wafer in the stack (E. Beyne, 2006). Therefore, when the number of stacked layers increases, the compound chip yield will decrease exponentially. However, this technology could be applied with the high yield of known good dies per wafer.

2.1.1 Solder Bump Interconnection

Solder bumps are small spheres of solder (solder balls) that are bonded to contact areas or pads of semiconductor devices and that are subsequently used for face-down bonding. The length of the electrical connections between the chip and the substrate can be minimized by (a) placing solder bumps on the die, (b) flipping the die over, (c) aligning the solder bumps with the contact pads on the substrate, and (d)re-flowing the solder balls in a furnace to establish the bonding between the die and the substrate. This method provides electrical connections with minute parasitic inductances and capacitances. In addition, the contact pads are distributed over the entire chip surface rather than being confined to the periphery. As a result, the silicon area is used more efficiently, the maximum number of interconnects is increased, and signal interconnections are shortened. (Zheng Xu et al, 2009) shows the magnitude and phase of S11 and S21 using the inherent adaptive solving approach of Momentum for the solder bump interconnection model. The performance degrades as the frequency increases: reflection noises increases and signal gain reduces. At frequencies of 15 GHz, 20 GHz, 25 GHz and 30 GHz, the S11 are -31.02dB, -21.17dB, -14.82dB, -9.01dB respectively. On the other hand, the S21 are 0.34dB, -0.49dB, -0.73dB, and -1.51dB for the frequency of 15 GHz, 20 GHz, 25 GHz and 30 GHz respectively. By using the de-embedding and extrapolation method, the de-embedded results for both S11 and S21 on this technology are -6.13dB and -1.92dB for operating frequency at 45GHz.

2.1.2 Surface Activated Bonding Interconnection

Surface activated bonding (SAB) was a recently developed high density interconnection method for advanced microelectronic system. SAB bonding was proposed based on the simple principle that two surface activated materials could be easily bonded together at the room temperature or low temperature. The surfaces were activated by fast atom beam or plasma irradiation source which has been proved helpful to remove the oxide and organic layer covering on the material surface (Zhonghua Xu, 2005). As bonding is carried out at the room temperature or low temperature and the material is surface activated before, no intermediate layer or impurity particle will exist at the as-bonded interface. That, for the SAB bonded Au-Al sample, a homogeneous intermetallic compound layer was finally grown and formed at the Au-Al interface (Au-Al) without any voids after 500hours thermal aging at 423K in air, which was completely different from the performance of Au-Al interface constructed by other interconnection techniques such as wire bonding or soldering flip chip method (Zhonghua Xu, 2005). (Chi-Tsung Chiu et al, 2002) shows the S11 and S21 are -12.78dB and -1.24dB respectively at 25GHz operating frequency. At 45GHz, the de-embedded result for S11 is -8.36dB and S21 is -1.35dB.

2.1.3 Through Silicon Via (TSV) Interconnection

As abovementioned (2.1), there were some limitations on the current emerged 3D stack technology. Thus, in order to overcome these problems, 3D chip-stacking

technology using through silicon vias (TSVs) is investigated because it offers a way to solve interconnection problems by replacing the wire-bonded technology while also offering integrated functions for higher performance (M. Koyanagi et al, 1998). Besides that, it allows the formation of high signal bandwidth, fine pitch, and short-distance interconnections in stacked dies (K. Sakuma et al, 2008).

3D integration TSV technology describes the process of vertically connecting several chips to achieve high functionality-to-volume ratio. In this technology, two or more vertically stacked chips are joined together by vertical interconnects running through the stack and functioning as components of the integrated circuit using established silicon technology (S. W. Yoon et al, 2009). The process sequence is different in TSV application, depending on either via first or via last formation approach is applied. However, the general process steps of TSV technology are bonding, thinning, wafer processing on bonded/thinned wafers, and subsequent de-bonding. The only different between these 2 process is via are etched during front-end-of-line for via first and back-end-of-line for via last. Via first process is favored by logic supplier and this is the most challenging process by far. The smallest via diameters for via-first schemes tend to be 5 to 10μm; aspect ratios are higher (10:1), posing challenges for liner and barrier step coverage, and for the quality of copper fill. On the other hand, via last approach is used in image sensors and stacked DRAM. CMOS image sensors have via diameters exceeding 40μm with aspect ratios of 2:1. In other devices, the vias range from 10 to 25μm with aspect ratios of 5:1. With a lower aspect ratio, the difficultly on via creation and process complexity is reduced.

Anyhow, the vias must be void free to offer a high reliability and low resistance contact. Thus, a variety of structures and processes have been demonstrated using copper, tungsten, and other materials. Each process flow in the fabrication of TSVs has its own challenges, and the structure as well as the choice of materials for filling the via depend on the specific application of the 3D integration (C. S. Patel et al, 2005). By looking at the S-parameter result, (F. Liu et al, 2010) shows the S11 and S21 are -21.78dB and -0.94dB respectively at 25GHz operating frequency. At 45GHz, the de-embedded result for S11 is -17.36dB and S21 is -1.15dB.

2.2 Signal Integrity on High Speed Channel

For today's high-speed boards and ICs, signal-integrity performance is as important to specify as digital functionality or clock speed due to the bus cycle is up to Gigahertz rate. Signal integrity problems, including delays, ringing, crosstalk, and EMI, can be identified through careful use of simulation (L. Green, 1999). Once the potential signal integrity problems are identified, design improvement like include different termination scheme, control the characteristic impedance of signal trace and change the package stack-up configuration can be done at the package layout stage. By addressing signal-integrity problems early in the package layout design stage, a high-performance product can be produced with higher reliability and lower cost.

2.2.1 Transmission Line Model and Signal Attenuation

A transmission line can be defined as a “conductive connection between a transmitter and a receiver capable of carrying a signal” (F. Caignet et al, 2001). Traditionally, transmission lines are thought of as telecom-based cables operating over long distances and functioned to connect 2 or more different devices. However, even the shortest passive printed circuit board (PCB) track suffers from transmission line effects as the digital speed is keep increasing. At low frequencies a wire or a PCB track may be considered to be an ideal circuit without resistance, capacitance, or inductance. But at high frequencies, AC circuit characteristics dominate, causing impedances, inductances, and capacitances to become prevalent in the wire (S. Chun et al, 2001). Figure 2.3 shows the circuit model used to determine the characteristic impedance of the wire or signal trace. This wire impedance is extremely important, as any mismatch within the transmission path will cause voltage reflection and results in a reduction in signal quality.

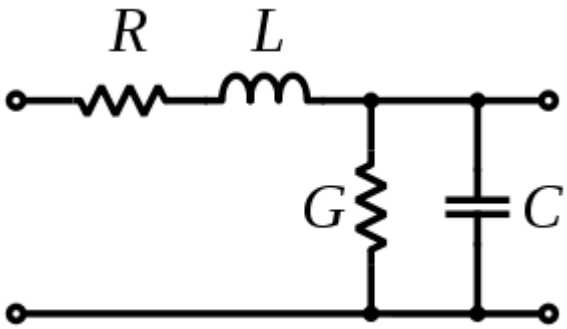

Figure 2.3: Circuit model for the Transmission Line Model.

Practically, the characteristic impedance of the signal trace should be controlled at 50Ω for single ended signal and 100Ω for differential pair signal in order to avoid the effect of impedance mismatch. It is caused when the output impedance of the source, the characteristic impedance of the signal line and the impedance of the receiver or load are not equal (W. R. Eisenstadt et al, 1992). As a result, the transmitted signal is not fully absorbed within the receiver and the excess energy will be reflected back to the transmitter and dissipate as heat. This process will continue back and forth until all of the energy is absorbed and steady state of voltage level is achieved. At high data rates, this phenomena will cause overshoot, undershoot, ringing, and stair-step waveforms and end up with the errors in signaling. In order to solve this signaling problem, characteristic impedance of the signal should be controlled via careful selection of medium and proper termination. Normally, there will be some tolerance of impedance value on driver, transmission line and receiver. In this case, different termination scheme like, series termination, far end parallel termination, RC termination and far end termination to voltage of power supply (Vcc) or ground (Gnd) should be used.

Although external component can often help for signal quality improvement, high-frequency signals are subject to losses along transmission lines, which interfere with the receiver's ability to interpret the information due to the transmission medium used to carry the signal (A. Deutsch et al, 1990). One of the major causes of losses along signal trace is dielectric absorption. It happened when high-frequency signals excite molecules in the insulator causing it to absorb signal energy resulting in a

reduction of the signal strength (V. Adsure et al, 2002). Dielectric absorption is directly related to the printed circuit board (PCB) material being used, and can be improved by careful selection of material.

Besides this, skin effect also plays an important role for a better signal quality. Skin effect occurred when current's waveforms are kept varying which directly caused by AC and high-frequency signals, then it tend to travel on the surface of a conductor. This results in the self-inductance of the material producing an increased inductive reactance at high frequencies, forcing electrons to the surface of the material (J. Fan, X. et al, 2010). The effective reduction of conductive area causes an increase of resistance and therefore attenuation of the signal. Increasing track width can reduce skin effect, but this is not always possible due to physical size limitation.

2.3 Summary

In this chapter, the basic concept of 3D integration and packaging was discussed. This technology allowed the signal and power of the stacked dies travelled vertically to device strata through short interconnect like wire bonding and interposer interconnection. Besides, the process flow of TSV was covered. The process sequence is different in TSV application, depending on either via first or via last formation approach is applied. However, the general process steps of TSV technology are bonding, thinning, wafer processing on bonded/thinned wafers, and subsequent de-bonding. In addition, the transmission line model which used to model the high speed

channel and methods used to optimize the electrical performance were explained in detail. Furthermore, the electrical performances are described for 3 of the different interconnection model in term of the S-parameter performance. Table 2.1 shows the summary of the S-parameter result by using both actual simulation and de-embedded technique.

Table 2.1: S-parameter result for solder bump interconnection, SAB interconnection, and TSV interconnection models technique for all of the models.

Stacked Die Model	**Return Loss, dB**		**Insertion Loss, dB**	
	30 GHz	**45 GHz**	**30 GHz**	**45 GHz**
Solder Bump Interconnection	-9.01	-6.13	-1.51	-1.92
SAB Interconnection	-12.78	-8.36	-1.24	-1.35
TSV Interconnection	-21.78	-17.36	-0.94	-1.15

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CHAPTER 3

METHODOLOGY AND PHYSICAL DESIGN IMPLEMENTATION

3.0 Introduction

In this chapter, the model and differences between stacked die package with solder bump interconnection, SAB, and VSCI were highlighted. Then, acomprehensive physical design cycle flow is presented for better illustration and to gain high accuracy result in this study.

In the TSV based 3D IC design, signal integrity is becoming the major design obstacle due to the high frequency loss, noise coupling, and electromagnetic radiation, while more than thousands of vertical and lateral interconnections are routed in a tiny 3D space (J. Kim et al, 2010). Besides that, current technologies which focus on the multi-stacked die package s signal distortion as the total z-height or the number of stacked die increases. Consequently, the functionality of a highly integrated stacked device is impacted as the signals travelling vertically through the TSV are more capacitive in nature.

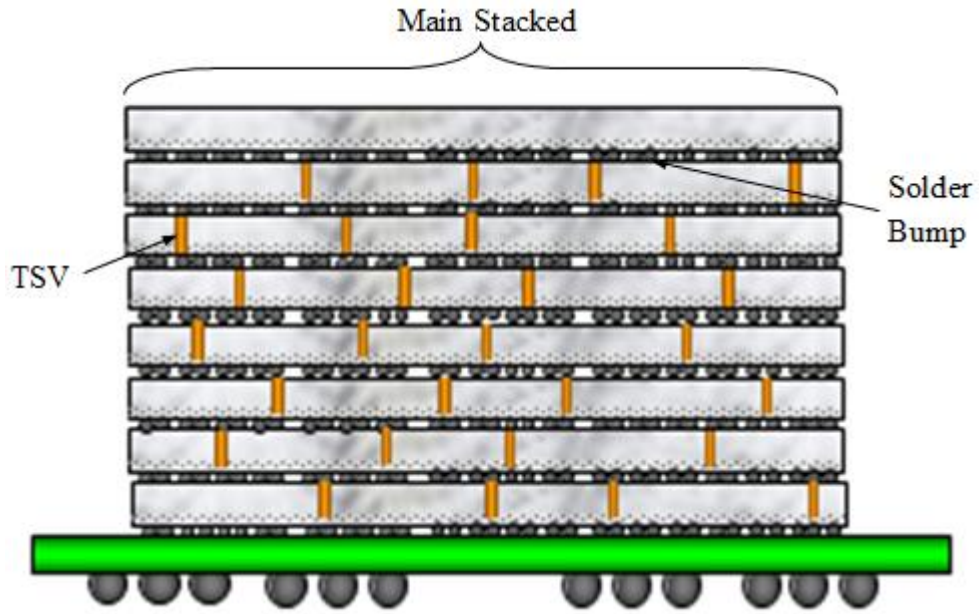

Figure 3.1: 8-die stacked package with *solder bump interconnection* (baseline).

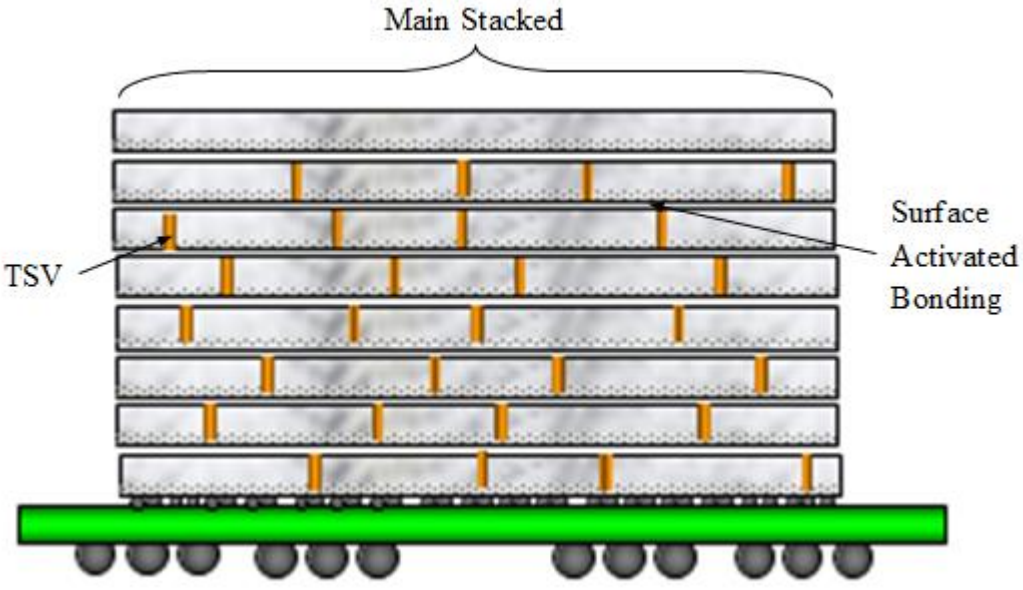

Figure 3.2: 8-die stacked package with *surface activated bonding (SAB)* interconnection.

In this chapter, the electrical performance and physical attributes of the stacked die package with VSCI [Figure 3.3] is pitted against the stacked die package with solder bump and SAB. The lateral signal length for the VSCI model is comparable with the z-height of the others two models. In addition, the lateral signal length or transmission line of the VSCI model is further extended for more practical implementation. Practically, a system-on-chip (SoC) processor size can be in range of 5mm x 5mm to 7mm x 7mm e.g. Intel Atom processor N550 and N450 are 5mm x 6mm. Hence, it is important to include such investigation in alignment to the industrial perspective.

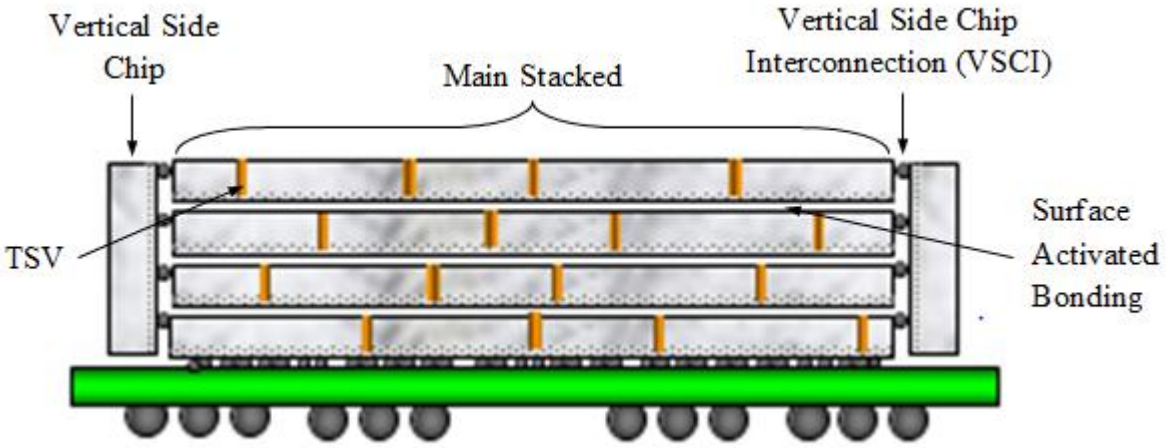

Figure 3.3: 8-die package with *VSCI*: 4 main-stacked dies with 4 vertical side chips (cross-sectional view).

Then, the optimization effort on signal integrity of VSCI is established in order to provides the trending of TSV signal orientation, TSV signal to ground ratio and TSV signal pitch impact to the overall signal integrity electrical performances. Lastly, the sensitivity of channel termination on vertical side-chip interconnection (VSCI) was carried out. The trends of eye height opening, one of the critical signaling parameters,

were analyzed based on transmission channel length, input rise time, receiver device capacitance and termination resistance factors.

3.1 Physical Design Flow for Modeling and Simulation

The whole design cycle for this project consists of pre-routing, modeling, package extraction, file conversion, simulation, routing optimization, and channel sensitivity analysis by referring to Figure 3.4. The pre-routing begin with the information on the designs rules, number of signal and ground, stack-up configuration, and up-front calculations of electrical parameters based on physical parameters like trace length, package thickness, signal pitch, and dielectric constant for medium layer. Then, package modeling and simulation were performed to generate both frequency and time domain analysis. Lastly, optimization effort was carried out by vary the TSV pitch, TSV orientation, and TSV signal to ground ratio followed by the sensitivity study of channel termination for VSCI model. The detail explanation of each design cycle had been presented in the subsection 3.2 to 3.6 of this chapter.