

# **LNA IC DESIGN FOR COGNITIVE RADIO IMPLEMENTATION**

**by**

**CHEONG CHEE HAN**

**Thesis submitted in fulfillment of the  
requirements for the degree of  
Master of Science**

**July 2013**

## **ACKNOWLEDGEMENT**

The author would like to express sincere gratitude to his project supervisor Dr. Norlaili binti Mohd. Noh for the guidance and patience throughout the inception of this project until its completion. Her ability to handle each project meeting and discussion in a short duration of time yet productive is definitely strength of hers.

Here, the author would like to express thanks to Farshad, a PhD candidate in the same team for his invaluable advises and assistance in both circuit design and software tools, Cadence. Thus, it helped in speeding up the process of completing this project.

Lastly, the author would like to thank his family for the support given throughout the studies.

## **TABLE OF CONTENTS**

	<b>PAGE</b>
ACKNOWLEDGEMENTS	ii
TABLE OF CONTENTS	iii
LIST OF TABLES	v
LIST OF FIGURES	vi
LIST OF SYMBOLS	viii
LIST OF ABBREVIATIONS	x
ABSTRAK	xii
ABSTRACT	xiii
 <b>CHAPTER ONE – INTRODUCTION</b>	
1.1 Background	1
1.2 What is Cognitive Radio and how it works	1
1.3 Conventional Radios, Software Defined Radios and Cognitive Radios	3
1.4 Problem Statement	4
1.5 Objectives	4
1.6 Organization of the Thesis	5
 <b>CHAPTER TWO – BACKGROUND AND LITERATURE REVIEW</b>	
2.1 Background	6
2.1.1 Low Noise Amplifier	6
2.1.2 Active Inductor	9
2.1.3 Negative Feedback	10
2.1.4 Common Source Amplifier	12
2.1.5 Radio Spectrum	14
2.1.6 Architectures of Cognitive Radio	14
2.2 Literature Review	16
2.2.1 Low Noise Amplifier for Cognitive Radio	16
2.2.2 Circuit Topologies	17
 <b>CHAPTER THREE – DESIGN METHODOLOGY</b>	
3.1 Proposed LNA	21
3.2 Hand Analysis	25
3.3 Circuit performance optimization	28

3.4	Considerations and best practices for the layout design	29
 <b>CHAPTER FOUR – RESULTS AND DISCUSSION</b>		
4.1	Introduction	31
4.2	Pre-layout simulations	31
4.2.1	Global Foundries’ 0.13 $\mu\text{m}$ process	32
4.2.2	Silterra’s 0.13 $\mu\text{m}$ process	38
4.3	Post-layout simulation	40
 <b>CHAPTER FIVE – CONCLUSIONS AND FUTURE WORK</b>		
5.1	Conclusions	46
5.2	Future work	47
 <b>REFERENCES</b>		
 <b>APPENDICES</b>		
Appendix A Layout diagrams of the LNA		

## LIST OF TABLES

	Page
Table 1.1: Conventional Radio, SDR and Cognitive Radio(Reed and Neel, 2008) ....	3
Table 2.1: Frequency bands (Regulation, 2010) .....	14
Table 3.1: Parameters of NMOS for two processes .....	25
Table 3.2: Comparison of LNA performance .....	26
Table 3.3: Parameters of LNA .....	28
Table 3.4: Final parameter values of the LNA.....	29
Table 4.1: Pre-layout simulated performance metrics .....	38
Table 4.2: Comparison of performance between process technologies .....	39
Table 4.3: Comparison of pre and post-layout simulated results.....	45
Table 4.4: Comparison of LNA performance .....	45

## LIST OF FIGURES

	Page
Figure 1.1: Block Diagram of Cognitive Radio (Haykin, 2005) .....	2
Figure 2.1: S-parameter port variable definitions .....	7
Figure 2.2: $P_{1dB}$ and $IP_3$ .....	8
Figure 2.3: Schematic of an active inductor and its equivalent circuit(Hampel et al., 2009) .....	9
Figure 2.4: General structure of a feedback amplifier (Sedra and Smith, 2004) .....	11
Figure 2.5: Basic configuration of common source amplifier (Razavi, 2002) .....	13
Figure 2.6: Physical architecture of CR(Akyildiz et al., 2006).....	15
Figure 2.7: Wideband RF front-end architecture(Akyildiz et al., 2006).....	16
Figure 2.8: Simplified Band Pass Filter LNA (Bevilacqua and Niknejad, 2004).....	17
Figure 2.9: Basic Noise Cancelling LNA (Razavi, 2010).....	18
Figure 2.10: Three-stage common source amplifier with negative feedback (Razavi, 2010) .....	20
Figure 3.1 Schematic of proposed LNA .....	21
Figure 3.2: Simplified model of the topology (Razavi, 2010) .....	22
Figure 3.3: Plot of components of $Y_{in}$ with frequency (Razavi, 2010).....	23
Figure 3.4: Noise model (Cheng et al., 2011) .....	24
Figure 4.1: Simulated $S_{11}$ .....	33
Figure 4.2: Simulated $S_{21}$ .....	34
Figure 4.3: Simulated $S_{22}$ .....	34
Figure 4.4: Simulated noise figure .....	35
Figure 4.5: Simulated stability factor, $K_f$ .....	35
Figure 4.6: Smith chart of $S_{11}$ showing the inductive effect .....	36
Figure 4.7: Simulated $P_{1dB}$ at 5 GHz.....	36
Figure 4.8: Simulated $IP_3$ at 5 GHz.....	37
Figure 4.9: $IP_3$ and $P_{1dB}$ from 300 MHz to 10 GHz .....	37

Figure 4.10: Smith chart of $S_{11}$ showing the inductive effect .....	39
Figure 4.11: Post-layout simulated $S_{11}$ .....	42
Figure 4.12: Post-layout simulated $S_{21}$ .....	43
Figure 4.13: Post-layout simulated $S_{22}$ .....	43
Figure 4.14: Post-layout simulated noise figure .....	44
Figure 4.15: Smith chart of $S_{11}$ .....	44

## LIST OF SYMBOLS

$\Omega$	Ohm
$\gamma$	Noise factor, $\gamma = 2/3$ for long-channel
$\mu_n$	Mobility of electron
$\epsilon_0$	Permittivity of free space, $\epsilon_0 = 8.854 \times 10^{-12}$ F/m
$\epsilon_{ox}$	Permittivity of oxide
$A_0$	Voltage gain at DC
$A_{CL}$	Closed-loop voltage gain
$A_{OL}$	Open loop voltage gain
$\beta$	Feedback factor
$C_{in}$	Input capacitance
$C_{ox}$	Oxide capacitance of NMOS
$f$	Frequency
$g_m$	Transconductance of the transistor
$I_D$	DC drain current
$\bar{i}_n$	External current noise generator
$K_{ox}$	Relative permittivity of silicon dioxide
$L$	MOSFET's channel length
$P_D$	Power dissipated by the LNA
$R_F$	Feedback resistor
$r_o$	Output resistance of the MOSFET
$R_S$	Source (Input) resistor
$S_{11}$	Input reflection coefficient
$S_{12}$	Reverse transmission coefficient
$S_{21}$	Forward transmission coefficient
$S_{22}$	Output reflection coefficient



$t_{\text{ox}}$	Oxide-thickness
$V_{\text{DD}}$	Supply voltage
$V_{\text{DS}}$	Drain-Source voltage
$V_{\text{gs}}$	Gate-Source voltage
$V_{\text{in}}$	Input voltage
$\overline{V_n^2}$	Noise voltage
$V_{\text{th}}$	Threshold voltage
$W$	MOSFET's width
$\omega$	Angular frequency
$\omega_0$	Cut-off frequency
$Y_{\text{in}}$	Input admittance
$Z$	Impedance
$Z_{\text{in}}$	Input impedance
$Z_o$	Ouput impedance

## **LIST OF ABBREVIATIONS**

AC	Alternating Current
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
CG	Common Gate
CMOS	Complementary Metal-Oxide-Semiconductor
CS	Common Source
CR	Cognitive Radio
dB	Decibel
DC	Direct-Current
DRC	Design Rule Check
EHF	Extremely High Frequency
GHz	Gigahertz
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HF	High Frequency
IF	Intermediate-Frequency
IIP <sub>3</sub>	Input-Referred Third-Order Intermodulation Point
IP <sub>1dB</sub>	Input 1-dB Compression Point
ISM	Industrial, Science and Medical
LF	Low Frequency
LNA	Low Noise Amplifier
LO	Local Oscillator
LVS	Layout versus Schematic
MCMC	Malaysia Communications and Multimedia Commission
MF	Medium Frequency

MHz	Megahertz
MOSFET	Metal-Oxide-Semiconductor Field-Effect-Transistor
NF	Noise Figure
NMOS	N-channel MOSFET
OIP <sub>3</sub>	Output-Referred Third-Order Intermodulation Point
OP <sub>1dB</sub>	Output 1-dB Compression Point
PEX	Parasitic Extraction
PLL	Phase Locked Loop
QoS	Quality of Service
SDR	Software Defined Radio
SHF	Super High Frequency
UHF	Ultra High Frequency
VCO	Voltage Controlled Oscillator
VLF	Very Low Frequency
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

## ABSTRAK

Tesis ini membentangkan LNA yang berjalur lebar tanpa induktor dengan tiga peringkat punca sepunya dan siap balik negatif untuk aplikasi komunikasi radio kognitif yang meliputi frekuensi 300 MHz ke 10 GHz. LNA ini direka dalam proses CMOS 0.13  $\mu\text{m}$  oleh Global Foundries dan melalui simulasi pos bentangan dalam lingkungan frekuensi yang dibincangkan,  $S_{21}$  minimum dan maksimum adalah masing-masing 10dB dan 12.1 dB manakala NF didapati dari 3.9 hingga 5.1 dB.  $S_{11} < -8.5$  dB dan  $S_{11} < -10$  dB dicapai sehingga 8.7 GHz.  $IIP_3$  mencapai sekurang-kurangnya -0.5 dBm dan maksimum 0.8 dBm pada pra-simulasi. Penggunaan kuasa adalah 36 mW pada 1.2 V. LNA ini menggunakan kawasan seluas  $26 \mu\text{m} \times 46 \mu\text{m}$  tanpa pad dan  $672 \mu\text{m} \times 233 \mu\text{m}$  dengan pad.

## ABSTRACT

This thesis presents a wideband inductorless three-stage common source (CS) low noise amplifier (LNA) with negative feedback for cognitive radio communication applications covering the range of 300 MHz to 10 GHz. Designed in Global Foundries' 0.13  $\mu\text{m}$  CMOS process and through post-layout simulations over the covered band, the minimum and maximum voltage gain is 10 dB and 12.1 dB respectively whereas noise figure of 3.9 to 5.1 dB.  $S_{11} < -8.5$  dB for the covered band and  $S_{11} < -10$  dB is achieved up to 8.7 GHz.  $IIP_3$  achieves a minimum of -0.5dBm and maximum of 0.8 dBm at pre-layout simulations. The power consumption is 36 mW at 1.2 V. The LNA occupies an area of  $26 \mu\text{m} \times 46 \mu\text{m}$  excluding pads and  $672 \mu\text{m} \times 233 \mu\text{m}$  with pads.

# **CHAPTER ONE**

## **INTRODUCTION**

### **1.1 Background**

The explosive growth of wireless devices such as mobile phone is gradually congesting the pre-allocated bands of the frequency spectrum. As projected by CISCO (xG, 2012), the network capacity will soon be outstripped by mobile bandwidth demand. However, the wideband spectrum especially licensed bands are still underutilized given the location, time and frequency bands. This means not all the licensed channels are occupied all the time and yet, the channels cannot be used by other users of both licensed and unlicensed. For example, in United States of America the Federal Communications Commission revealed that the utilization in the most densely packed urban areas rarely passes 35%. Also, the usage of spectrum could vary from 15% to 85% depending on the place and time of day (RAO et al., 2011). Therefore, cognitive radio (CR) enables unlicensed users (WLAN, ISM) to use the licensed spectrum, plus minimizing interference.

### **1.2 What is Cognitive Radio and how it works**

CR was first introduced by Mitola III and Maguire Jr (1999). CRs find its application in alleviating the congestion by opportunistic spectrum sharing. When the primary users of certain frequency bands are not using them, secondary users are able to access the vacant frequency bands without agreement. These frequency bands could span from either licensed or unlicensed frequencies which ranges from satellite, TV, telecommunication to radio stations, and even WLAN. For example, a CR mobile phone can connect to the Internet by using any frequency band deemed suitable for its current application (Klumperink, 2012).

To achieve these features, the CRs have to be able to accommodate and operate at a very wide bandwidth, typically from Megahertz to Gigahertz. To further elaborate the concept of cognitive radio, it is a way in designing a radio network system having both intelligence and agility. CRs operates by continually monitor, sense and detect the surroundings, and dynamically reconfigures itself to adapt those environment. Figure 2.1 illustrates the processes involved in a CR system. CRs enable the wireless devices to use the frequency spectrums in an efficient way, by adjusting and optimizing transmitting parameters like output power, frequency range, and modulation type for users. In 2012, (xG, 2012) demonstrated its product xMax Cognitive Radio System in a rural area and claimed successful in delivering high quality mobile broadband connection to a group of users by connecting their smartphones and laptops to the Internet using unlicensed spectrum.

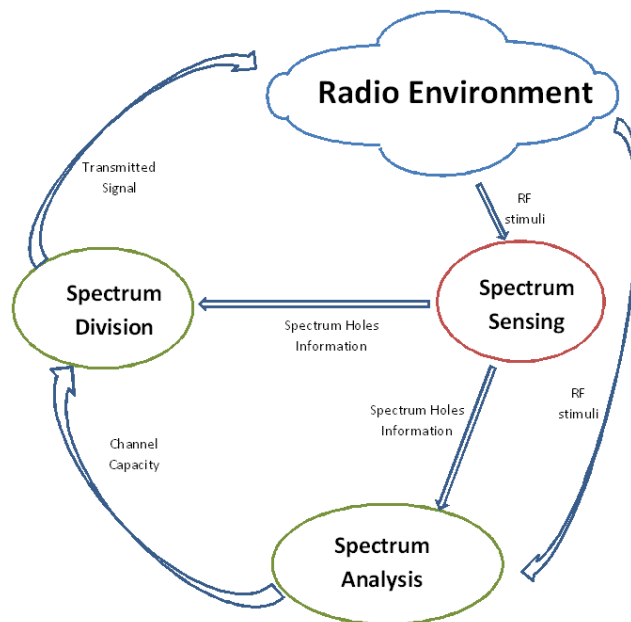


Figure 2.1: Block Diagram of Cognitive Radio (Haykin, 2005)

### 1.3 Conventional Radios, Software Defined Radios and Cognitive Radios

Another type of radio is called Software Defined Radio. It has similar capabilities as the Cognitive Radio. SDR is able to configure its wireless communication protocols such as frequency band, air interface protocol and functionality without replacing the hardware. In fact, to qualify a Cognitive Radio, it has to have some of the features of the SDR. One can view Cognitive Radio as an upgraded version of SDR (Instrument, 2013)

Some of the differences for conventional, software defined and cognitive radios are listed in the Table 1.1 as follows

Table 2.1: Conventional Radio, SDR and Cognitive Radio(Reed and Neel, 2008)

CONVENTIONAL RADIO	SOFTWARE DEFINED RADIO	COGNITIVE RADIO
<b>Application</b>		
Supports only a fixed number of systems	Supports multiple systems, protocols and interfaces dynamically	Can create its own waveforms
Re-configurability is difficult	Provides a wide range of services with a number of Quality of Service (QoS)	Supports add-on interfaces
Supports a number of services but chosen at the time of design		Configure operations to meet QoS according to application and signal environment
<b>Design</b>		
Traditional RF Design	Conventional Radio + Software Architecture	SDR + Intelligence
Traditional Baseband Design	Supports re-configurability	Environment sensing and learning
<b>Upgrade Cycle</b>		
Not upgradable / future proof	Future proof	Includes SDR's upgrade mechanism
	Supports over-the-air (OTA) upgrade mechanism	Supports internal and collaborative upgrades



## 1.4 Problem Statement

More applications are expected from CR and thus expectations are getting higher in terms of bandwidth it can cover, aside from the popular mobile phone communication bands. Such applications will require the radio to operate from tens to hundreds of Megahertz to cover TV and FM broadcasting and a high frequency of Gigahertz to cover satellite bands. This means the LNA needs to have enough power gain and low noise figure yet flat and a good input impedance matching across the decade-wide bandwidth. A good linearity is essential to tolerate interferers as the radio is operating across different standards or bands.

## 1.5 Objectives

With the problems as stated in the previous section, the following objectives are set.

- a) To design and optimize an LNA to cater for the wide bandwidth requirement of a Cognitive Radio by using the 0.13  $\mu\text{m}$  Silterra process
- b) The LNA designed must be stable and able to display a flat gain across the wide frequency range

In relation to this, the specification of the design is set to be as follows

- Bandwidth of 300 MHz to 10 GHz
- Flat gain of more than 10 dB
- Flat NF of approximately 5 dB
- $|S_{11}|$  more than 10 dB

## **1.6 Organization of the Thesis**

The thesis starts with Chapter 1 where CR is introduced. This chapter also presents the problem statement of the LNA for CR followed by the objectives. Chapter 2 covers the necessary background and theory needed for the circuit design. Circuit topologies are also discussed with pros and cons of each technique. Subsequently, the inductorless three-stage common source with negative resistive feedback topology chosen is elaborated in Chapter 3. The design methodology for this specific LNA topology is given in this chapter. This includes the hand analysis, optimizations and calculations needed to determine the components and parameters of the LNA. Chapter 4 presents the simulation results for both pre and post layouts with analysis on the findings. Finally, Chapter 5 wraps up this thesis with concluding remarks and recommendation for future work.

## CHAPTER TWO

### BACKGROUND AND LITERATURE REVIEW

#### 2.1 Background

##### 2.1.1 Low Noise Amplifier

Low Noise Amplifier (LNA) is a type of electronics amplifier which is used in communication systems (for example GPS) to amplify weak signals captured by an antenna. It is typically employed as the first stage of a receiver system, and it is important that this stage to be designed with lowest noise possible while giving sufficient signal gain to the weak signal from the antenna. The reason being the total noise figure of the receiver system is dominated by the first few stages, and the effect of the noise from other stages can be reduced by the gain of the LNA, while injecting its noise to the received signal.

Besides having low noise figure, an LNA has to abide to some other important performance metrics as well. They are the impedance matching, gain and linearity. The impedance matching and gain are usually measured by the S-parameters represented by  $S_{11}$ ,  $S_{12}$ ,  $S_{21}$  and  $S_{22}$ . S-parameters are usually used to evaluate a design in high frequencies due to its simplicity of not needing to synthesize a short or open circuit, and terminating the two-port in  $Z_0$  reduces possibility for oscillation. Referring to Figure 2.1, if  $Z_0$  is the source and load termination, port 1 is the input, port 2 is the output,  $S_{11}$  will mean the ratio of reflected power from port 1 to the applied power to port 1, and is also termed as input port reflection coefficient or input return loss. The lower the  $S_{11}$  ( $S_{11} = -\infty$  for perfect input impedance matching), the lesser the input signal be reflected from the LNA, as well as a closer value of input impedance to 50  $\Omega$ . The input impedance has

to be designed to a typical value  $50\ \Omega$  so as to provide matching to the input source, as most antennas have impedance of  $50\ \Omega$ .  $S_{21}$  is related to gain since squaring its magnitude is known as forward power gain.

$S_{22}$  is the output reflection coefficient (or output return loss) which has a similar definition as  $S_{11}$  but applies to output port. Lastly,  $S_{12}$  is the reverse isolation (or reverse transmission coefficient) which determines the level of feedback from the output to the input of the LNA, thus defines its stability (Lee, 2004)

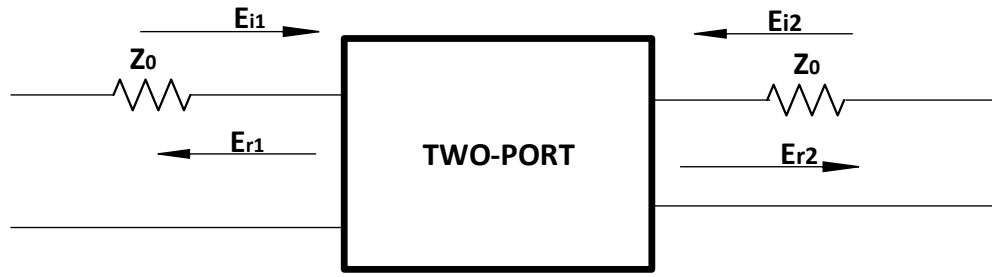


Figure 2.1: S-parameter port variable definitions

Next, an important aspect to be considered when designing an LNA is the linearity. A good LNA must also be to maintain linear operation even when receiving strong signals, and weak signals in the presence of interference. Else, this intermodulation distortion will cause desensitization (or blocking) and cross-modulation. Blocking happens when the intermodulation products caused by the strong interferer flood the desired weak signal. Cross-modulation occurs when nonlinear interaction transfers the modulation of one signal to another carrier. Thus, there is a need to minimize the impact of these effects as well. The commonly used measures of linearity are third-order intercept (input,  $IIP_3$ , with output,  $OIP_3$ ) and 1-dB compression point (input,  $IP_{1dB}$  with output,  $OP_{1dB}$ ).

As indicated, an LNA must be able to maintain linearity at both weak and strong receiving signals. However, there is a limit at which as the input signal increases to a certain point, its gain decreases. Here, the  $P_{1dB}$  indicates the power level or a point where the gain drops by 1 dB from its small signal value. Further increasing the input power reduces the gain, which means the circuit is no longer linear. This is as shown in Figure 2.2.

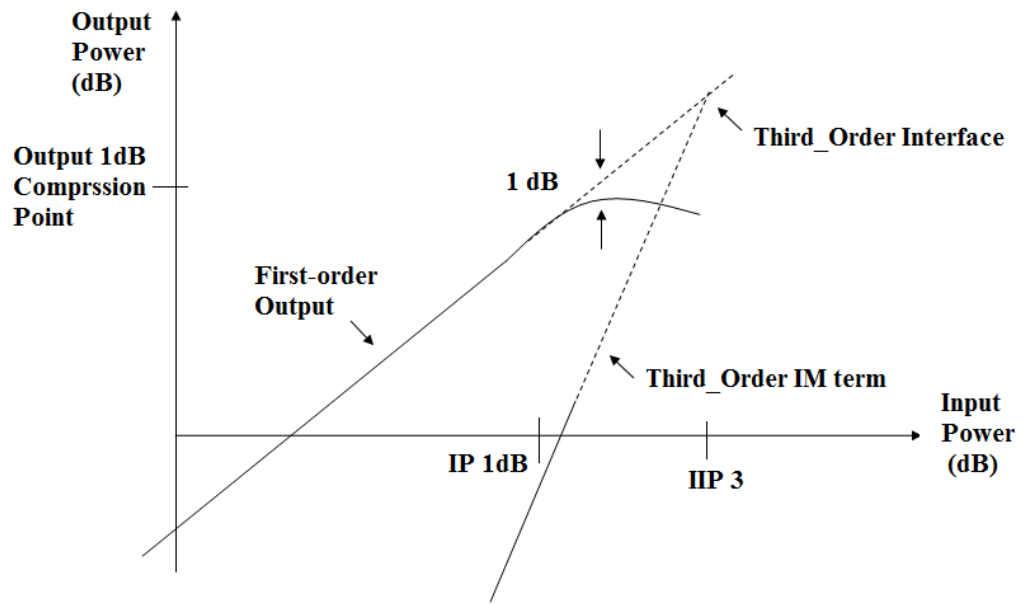


Figure 2.2:  $P_{1dB}$  and  $IP_3$

Another way to measure linearity is to apply two signals at the input, of same amplitude but slightly different in frequency. Referring to Figure 2.2, after plotting the fundamental and intermodulation output power as a function of input power, the third-order intercept point ( $IP_3$ ) can be determined. The  $IP_3$  is a point where amplitudes of the intermodulation tones at  $2\omega_1 - \omega_2$  and  $2\omega_2 - \omega_1$  are equal to the amplitudes of the fundamental tones at  $\omega_1$  and  $\omega_2$ .

### 2.1.2 Active Inductor

Large area in the layout required by the inductors is always the drawback for LNA topologies in the likes of distributed amplifiers and common source amplifier using a band-pass filter network. The concept of active inductor can be employed to overcome this problem by replacing passive inductors with active inductors or by constructing a design that exhibits the effects of active inductor. An example of the concept is shown in Figure 2.3 where the gate drain terminal is connected by a resistor and gate source terminal is connected by a bypass capacitor, to allow better design freedom or control towards the inductance. The input impedance looking into the source terminal can be expressed as follows (Hampel et al., 2009)

$$Z_{in,AI} = R_{AI} + j\omega L_{AI} \quad (2.1)$$

where

$$R_{AI} \approx \frac{1}{g_m} \quad (2.2)$$

$$L_{AI} \approx \frac{R_g(C_{gs} + C_{by})}{g_m} \quad (2.3)$$

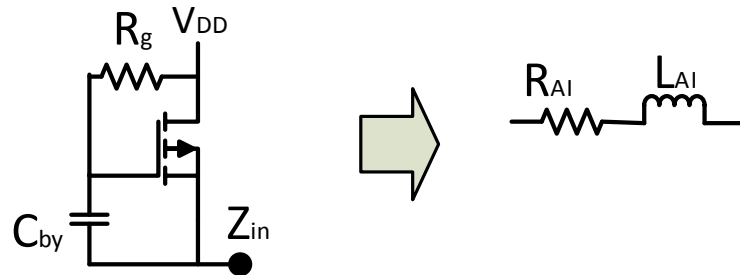


Figure 2.3: Schematic of an active inductor and its equivalent circuit(Hampel et al., 2009)

### 2.1.3 Negative Feedback

According to Sedra and Smith (2004), negative feedback can be viewed as a path that returns a part of output signal out of phase with the input signal. In an amplifier design, a negative feedback is usually employed when the designer wants the effect of the following properties.

- i. Extend the bandwidth of an amplifier at the expense of gain.
- ii. Make the amplifier gain less sensitive to component variations, thus a more constant gain.
- iii. Control the input and output impedance with appropriate feedback topology. It may also cause these impedances to become sensitive with gain.
- iv. Reduce noise, when the anti-phase noise is fed back, it subtracts the noise generated within the closed loop.

Figure 2.4 shows the basic structure of a feedback amplifier. Without feedback, the input and output voltage can be related to open loop gain by

$$V_o = A_{OL} V_i \quad (2.4)$$

where

$V_o$  is the output voltage

$V_i$  is the input voltage

$A_{OL}$  is the open loop gain

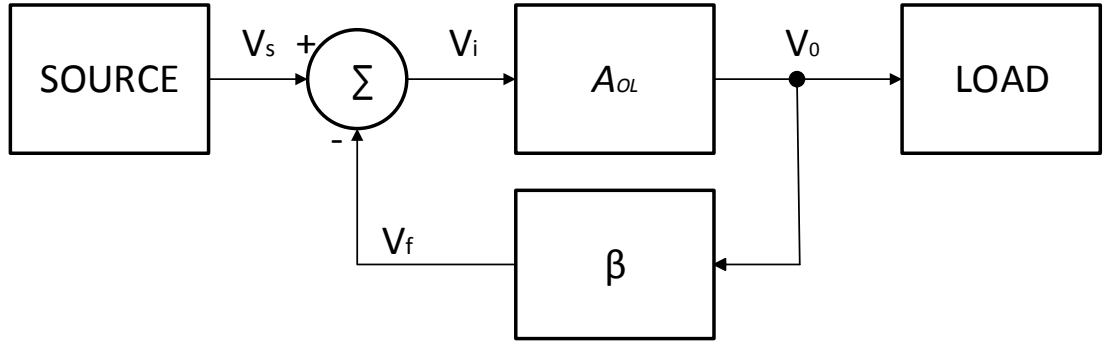


Figure 2.4: General structure of a feedback amplifier (Sedra and Smith, 2004)

The output signal,  $V_o$  is passed to the load and also the feedback path, thus the feedback signal,  $V_f$  is related to  $V_o$  by the feedback factor,  $\beta$ .  $V_f$  is then subtracted from the  $V_s$ , producing  $V_i$  which serves as the input of the amplifier.

$$V_f = \beta V_o \quad (2.5)$$

It follows that

$$V_i = V_s - V_f \quad (2.6)$$

Basically, this subtraction reduces the  $V_s$  to  $V_i$ . The closed-loop gain of the amplifier can be obtained by solving Equations 2.4 to 2.6, yielding

$$A_{CL} \equiv \frac{V_o}{V_s} = \frac{A_{OL}}{1 + A_{OL}\beta} \quad (2.7)$$

This shows the reduction of open loop gain. Feedback can also be used to extend the bandwidth of an amplifier. Suppose now an amplifier is operating in a high frequency and can be modeled by a one-pole response. Its open loop response can be expressed as



$$A_{OL}(s) = \frac{A_0}{1 + \frac{s}{\omega_0}} \quad (2.8)$$

where

$A_0$  is the amplifier's DC gain

$\omega_0$  is the cut-off frequency

If the feedback is applied to the amplifier, the closed-loop gain will now become (substituting Equation 2.8 into Equation 2.7)

$$A_{CL}(s) = \frac{A_0}{(1 + \beta A_0)(1 + j\frac{\omega}{(1 + \beta A_0)\omega_0})} \quad (2.9)$$

#### 2.1.4 Common Source Amplifier

According to Gray and Meyer (1993) and Razavi (2002), common source amplifier is one of the three basic amplifier configurations. It can be identified when the signal is applied to the gate terminal and amplified signal is taken from the drain terminal. Figure 2.5 shows the configuration the amplifier. This topology can hardly be used in high frequency applications as its functionality will be greatly affected by the terminal capacitance and usually band-pass filters are required at the input where they are composed of area consuming components like inductors and capacitors (Li, 2011). A common source amplifier can be analyzed by DC and AC analysis. In DC analysis, the circuit is analyzed to find the operating or bias point that determines the maximum lower and upper voltage swing of the amplifier. Also, the NMOS must be biased in order to keep the amplifier working in saturation region ( $V_{DS} > V_{gs} - V_{th}$ ). Referring to Figure 2.7, it can be written that

$$V_{out} = V_{DD} - I_D R_1 \quad (2.10)$$

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{gs} - V_{th})^2 \quad (2.11)$$

$$C_{ox} = \frac{K_{ox} \epsilon_o}{t_{ox}} \quad (2.12)$$

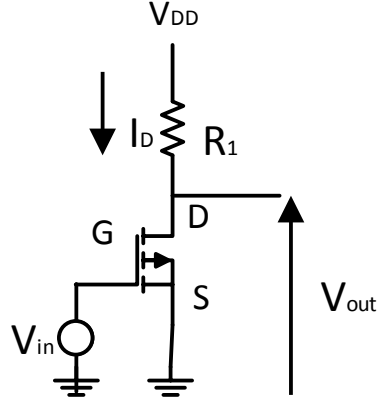


Figure 2.5: Basic configuration of common source amplifier (Razavi, 2002)

The parameters of interest would usually be solving for the size of the transistor (given by width and length), the operating current  $I_D$ ,  $V_{gs}$ ,  $V_{out}$ , and/or  $R_1$ . In AC analysis however, calculations of circuit gain and terminal impedances can be simplified by using linear equations on the nonlinear behaviour of the device. The small signal voltage gain can be expressed as

$$A \equiv \frac{V_{out}}{V_{in}} = -g_m(r_o || R_1) \quad (2.13)$$

$$g_m = \frac{2I_D}{V_{gs} - V_{th}} \quad (2.14)$$

$$r_o \approx \frac{1}{\lambda I_D} \quad (2.15)$$

### 2.1.5 Radio Spectrum

CRs make use of a wide range of frequency to gain more options for the system to operate. Therefore, it has to make use of both licensed and unlicensed spectrum. Table 2.1 shows a list of radio frequency spectrum with its applications

Table 2.1: Frequency bands (Regulation, 2010)

Band	Frequency	Application
VLF	3 - 30 kHz	Submarine communications time signals, storm detection
LF	30 - 300 kHz	Broadcasting (long wave), Navigation beacons
MF	300 – 3000 kHz	Broadcasting (medium wave), maritime communications, analogue cordless phones
HF	3 – 30 MHz	Broadcasting (short wave), aeronautical, citizens band
VHF	30 – 300 MHz	FM broadcasting, Business Radio, Aeronautical
UHF	300 – 3000 MHz	TV Broadcasting, WLAN, GPS, mobile phones, digital cordless phones, military use
SHF	3 – 30 GHz	Point to point links, satellites, fixed wireless access
EHF	30 – 300 GHz	Point to point links, multimedia wireless systems

### 2.1.6 Architectures of Cognitive Radio

A physical architecture of a CR transceiver is shown in Figure 2.6. Here, a wideband signal is received through RF front-end, amplified, mixed, converted to digital and measurements carried out to detect the licensed user signal. Looking into the wideband RF front-end architecture shown in Figure 2.7, the wideband antenna receives signals from various sources or transmitters operating at various power levels, bandwidths and locations, so the RF front end should be able to detect weak signals in the presence of very strong signals over a wide dynamic range.

Consequently, the linearity of the RF circuits must be designed with more stringent requirements. A short description that describes the components of the cognitive radio RF front-end is as follows:

- RF filter: Selects the desired band by using band-pass filter on the received signal.
- LNA: Amplifies the desired signal while minimizing noise
- Mixer: the signal is mixed with local generated RF frequency and then converted to IF or baseband.
- VCO: Generates signal at a desired frequency and voltage to mix with the incoming signal.
- PLL: Locks the signal at a specific frequency
- Channel Selection Filter: Selects desired channel and rejects adjacent channels
- AGC: Maintains a constant gain or output power level of an amplifier over a wide range of input signal levels (Akyildiz et al., 2006)

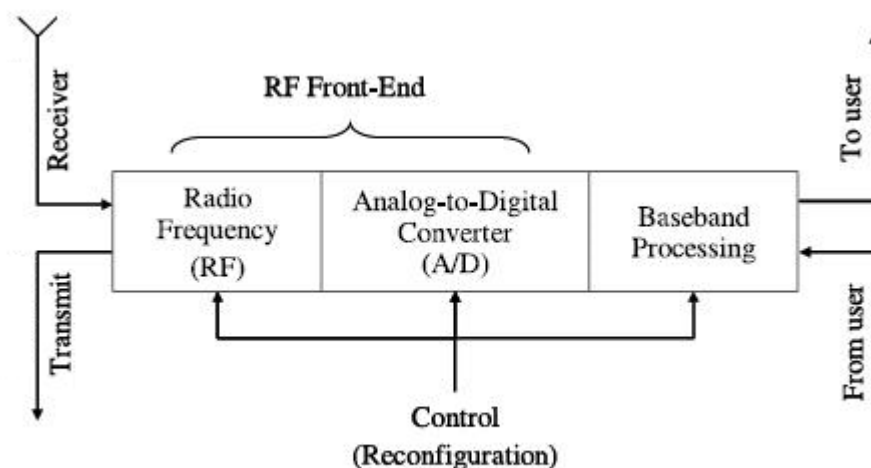


Figure 2.6: Physical architecture of CR(Akyildiz et al., 2006)

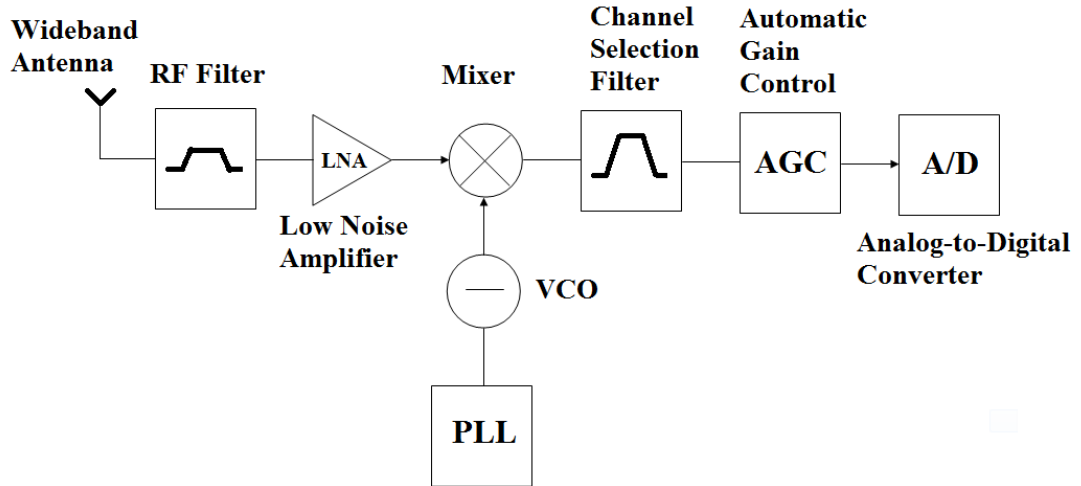


Figure 2.7: Wideband RF front-end architecture(Akyildiz et al., 2006)

## 2.2 Literature Review

### 2.2.1 Low Noise Amplifier for Cognitive Radio

Many designs have been made so far to cover as much frequency range as possible, targeting especially TV bands below 1 GHz. An LNA topology introduced by Razavi (2010) was able to operate from 50 MHz to 10 GHz. However, this bandwidth alone is insufficient to define the transceiver as a CR yet, it may be deemed as a “supersized” SDRs. CRs must be able to operate at any frequency for the range covered. This is unlike of SDRs, which target certain standards or bands. Next, CRs must be able to tolerate interferers at any frequency bands (WCDMA, GPRS and GSM to name a few) in its bandwidth  $BW_{CR}$ . Hence, its  $IP_3$  metric has to meet more stringent bounds. The CR receiver has to provide a relatively flat gain with adequate input return loss across these decades wide of frequency, thus traditional RF circuit techniques are struggling to comply (Razavi, 2009).

### 2.2.2 Circuit Topologies

Favourite topologies for wideband LNA like Common Gate (CG), Resistive-Feedback and Inductive Degeneration are good if the required bandwidth covers a few Gigahertz. As far as decades wide bandwidth is concerned, there are limited topologies that have been discussed (Razavi, 2010). In this section, works of other authors comprise of several techniques in the field of ultra wideband LNA design are discussed.

#### 2.2.2(a) Band-pass Filter Technique

This topology employs common source configuration as shown in Figure 2.8. Wideband applications can be achieved by incorporating the input of the common source LNA into a band-pass filter network. However, this topology faces its limitation of providing a wide range of bandwidth especially at lower frequencies. Another drawback of this topology is large area consumed by the input band-pass filter(Battista et al., 2008) (Kargaran and Kargaran, 2009).

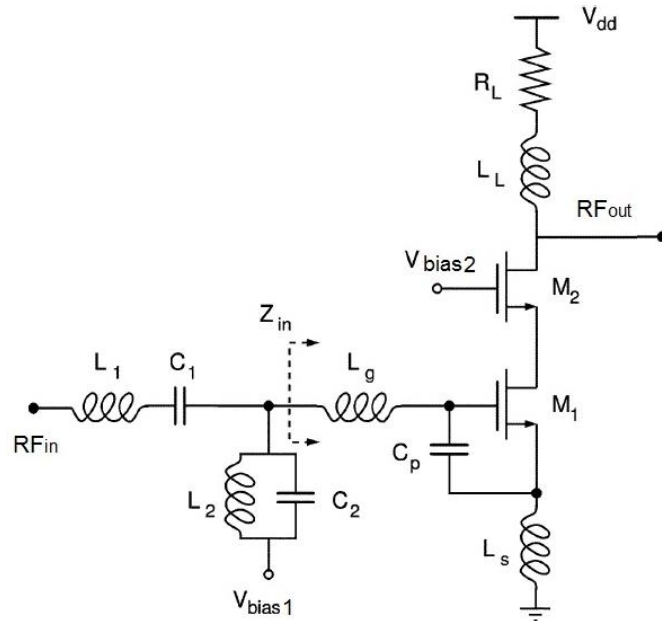


Figure 2.8: Simplified Band Pass Filter LNA (Bevilacqua and Niknejad, 2004)

### 2.2.2(b) Noise Cancellation Technique

The common gate topology, which is supposedly a suitable candidate for wideband input matching, suffers from a relatively high noise figure. In order to reduce the noise, another common source stage which has the same gain is attached as the second stage of the LNA. Referring to Figure 2.9, since the noise show up at both the output node of CG and CS, the output differential is able to cancel the noise. However, as decade-wide bandwidth is concerned, this topology faces difficulties in maintaining a low NF at high frequencies (Blaakmeer et al., 2007) (Najari et al., 2010) (Liao and Liu, 2007).

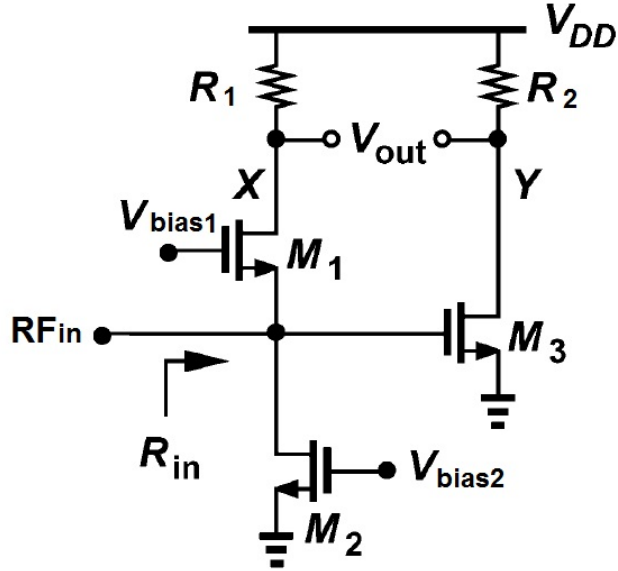


Figure 2.9: Basic Noise Cancelling LNA (Razavi, 2010)

### 2.2.2(c) Three-Stage Common Source with Negative Feedback

An LNA topology proposed by Razavi (2010) was reported to be able to achieve bandwidth of 50 MHz to 10 GHz with gain of 18 to 20 dB, NF of 2.9 to 5.9 dB,  $|S_{11}| > 10$  dB,  $IP_3$  of -11 to -7 dBm and power of 22 mW on a fabricated chip

using 65 nm process technology. The circuit is as shown in Figure 2.10. This topology incorporates three stages of common source amplifiers, plus a negative resistive feedback. Since the drawback of using a negative feedback is that it lowers down the gain of the system by the factor of  $1 + \beta A_{OL}$  (see Equation 2.7), this drawback is compensated by the high voltage gain from the three stages of common source amplifier. The negative resistive feedback has an added advantage of exhibiting inductive input impedance effect which was as discussed in section 2.1.2. This explains the absence of inductors in this topology is still workable, albeit having common source configuration in the design.

Current  $I_1$  is used to solve the issue of having low quiescent voltage at point Y. This is caused by low  $V_{gs}$  of about 200 mV, since having a large width. As a result, the current  $I_1$  drawn from  $R_F$  is able to shift the voltage up by approximately 250 mV. With three stages, this design could suffer from phase margin as well as peaking in frequency response, thus leading to a more complex analysis especially on the inductance part. However, the author of this topology had confirmed with behavioral simulation that the one-pole approximation still holds the calculation of input admittance accurately. The output of this LNA is taken between nodes X and Y. Although the nodes exhibit phase difference, this pseudo differential still increases the gain and linearity. Device labeled as Z at the output node is a buffer, implemented to facilitate the testing of the LNA.



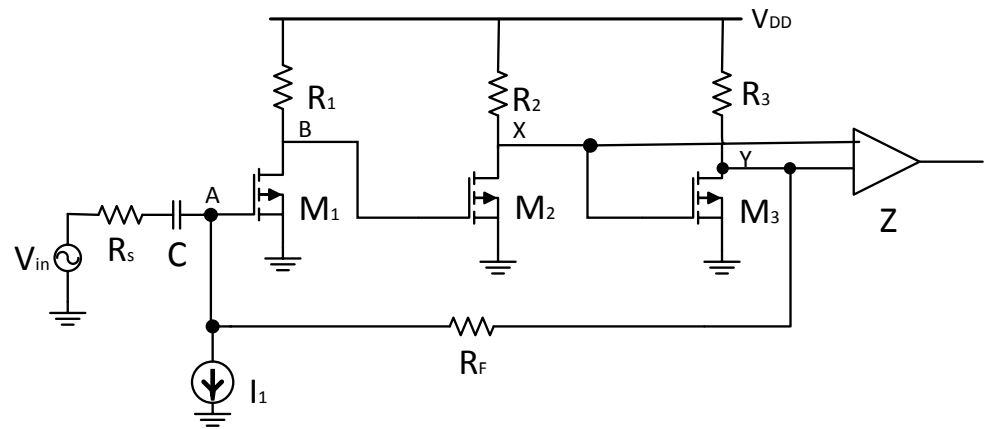


Figure 2.10: Three-stage common source amplifier with negative feedback (Razavi, 2010)

## CHAPTER THREE

### DESIGN METHODOLOGY

#### 3.1 Proposed LNA

To the author's knowledge, Razavi (2010)'s topology achieved a good overall performance with a high gain over a bandwidth from 50 MHz to 10 GHz. However, the noise figure (5.9 dB) and  $IP_3$  (-11.2 dBm) did not perform well. Thus, the proposed design is meant to investigate and improve both the linearity and noise figure. Figure 3.1 shows the schematic of the proposed LNA.

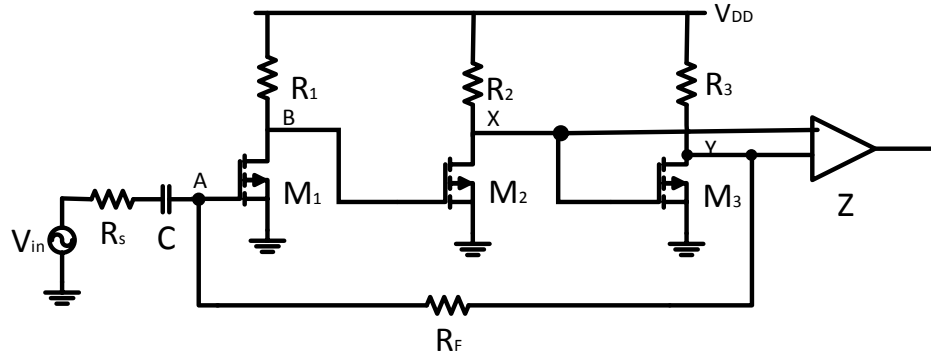


Figure 3.1 Schematic of proposed LNA

To further analyze the circuit, the inductive effect from the negative resistive feedback (resistive shunt) will be used in input matching, specifically to cancel the input capacitance,  $C_{in}$  of the common source configuration (Figure 3.2) at low frequencies. The effect will be obvious if depicted in the smith chart as the  $S_{11}$  curve will be seen turning clock-wise above the real axis (inductive) and ending at the below of the real axis (capacitive).

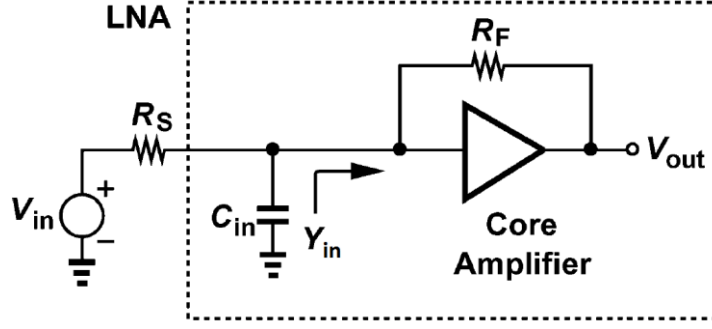


Figure 3.2: Simplified model of the topology (Razavi, 2010)

From Figure 3.1, the open loop DC gain of the three stages can be approximated as Equation 3.1 as  $r_o$  is much larger than its resistance connected at drain terminal while feedback factor is given by Equation 3.2.

$$A_0 \approx g_{m1}R_1 \cdot g_{m2}R_2 \cdot g_{m3}R_3 \quad (3.1)$$

$$\beta = \frac{R_S}{R_S + R_F} \quad (3.2)$$

With the open loop transfer function (Equation 2.8), and applying Miller's theorem to the feedback resistor,  $R_F$  yields the input admittance which is expressed as

$$Y_{in}(s) = \frac{s + (A_0 + 1)\omega_0}{R_F(s + \omega_0)} \quad (3.3)$$

Taking out the real and imaginary parts yields

$$\frac{1}{\text{Re}\{Y_{in}\}} = \frac{R_F(\omega_0^2 + \omega^2)}{(1 + A_0)\omega_0^2} \approx \frac{R_F}{1 + A_0} \quad (3.4)$$

$$\text{Im}\{Y_{in}\} = \frac{-A_0\omega\omega_0}{R_F(\omega_0^2 + \omega^2)} \approx \frac{-A_0\omega}{R_F\omega_0} \quad (3.5)$$

For input matching,  $\frac{1}{\text{Re}\{Y_{in}\}}$  is set equal to  $R_s$ , and  $\text{Im}\{Y_{in}\}$  is used to cancel

$C_{in}\omega$ . Both the real and imaginary components are modeled in Figure 3.3.

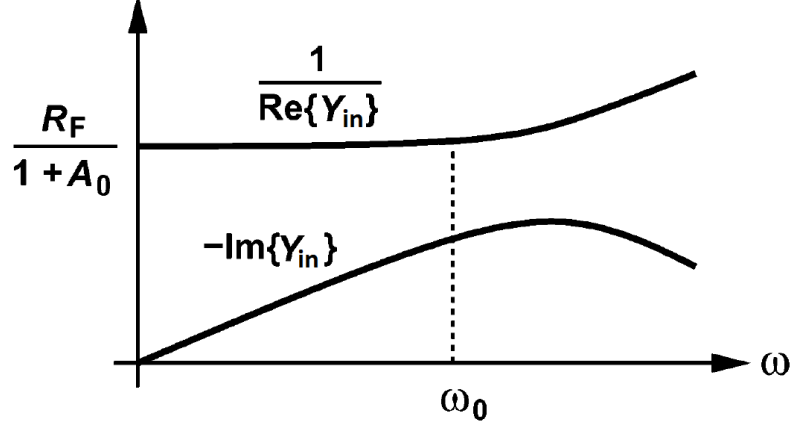


Figure 3.3: Plot of components of  $Y_{in}$  with frequency (Razavi, 2010)

The width of the input transistor  $M_1$  is set larger to minimize the noise which is contributed by thermal noise approximate by  $I_{n,M}^2 = 3kT\gamma g_m$  where  $\gamma$  is the noise factor. The noise figure can be modeled as in Figure 3.4. Considering thermal noise, the total output noise power is given as (Cheng et al., 2011)

$$\begin{aligned}
 \overline{V_{n,out}^2} &= \sum (V_{n,x} - V_{n,y})^2 \\
 &= \frac{1}{(1 - \beta A_0)^2} \sum \overline{(V_{n,xo} - V_{n,yo})^2} \\
 &= \frac{1}{(1 - \beta A_0)^2} (\overline{V_{n,ln}^2} + \overline{V_{n,\beta}^2} + \overline{V_{n,1}^2} + \overline{V_{n,2}^2} + \overline{V_{n,3}^2}) \quad (3.6)
 \end{aligned}$$

where

$$\begin{aligned}
 \overline{V_{n,ln}^2} &= \overline{V_{n0,R_s}^2} \\
 \overline{V_{n,\beta}^2} &= \overline{V_{n0,R_F}^2} \\
 \overline{V_{n,1}^2} &= \overline{V_{n0,R_1}^2} + \overline{V_{n0,M_1}^2}
 \end{aligned}$$

$$\overline{V_{n,2}^2} = \overline{V_{n0,R_2}^2} + \overline{V_{n0,M_2}^2}$$

$$\overline{V_{n,3}^2} = \overline{V_{n0,R_3}^2} + \overline{V_{n0,M_3}^2}$$

Thus, noise figure is given by

$$NF = \frac{1}{4kTR_S} \frac{\overline{V_{n,out}^2}}{\left(\frac{R_{in}}{R_S + R_{in}} A\right)^2} \quad (3.7)$$

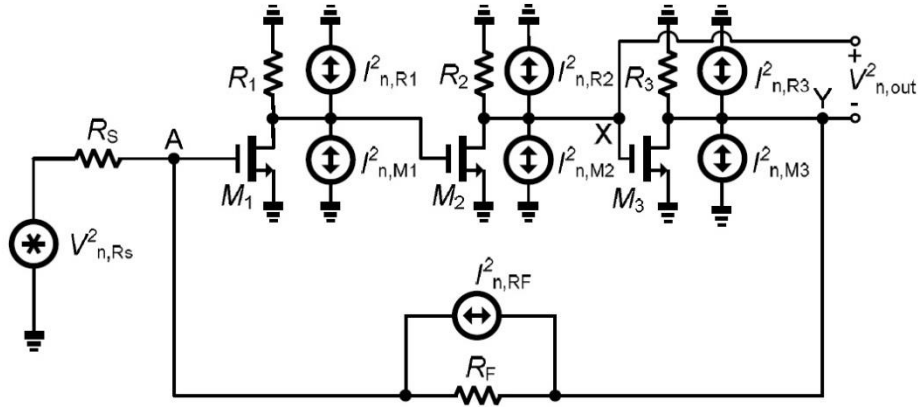


Figure 3.4: Noise model (Cheng et al., 2011)

In this design (Figure 3.1), the current source  $I_1$  (Figure 2.10) is taken out since its function of shifting up the quiescent voltage is not needed. Referring to the list of parameters extracted from the Global Foundries' model library (Table 3.1),  $C_{gs}$  and  $C_{ox}$  can be calculated by  $C_{gs} = (2/3)WLC_{ox}$  and  $C_{ox} = \epsilon_{ox}t_{ox}$  with  $\epsilon_{ox} = 3.9\epsilon_o$ .  $C_{gs}$  turns out to be  $1.32e-13$  F if  $W = 110 \mu m$  and  $L = 130$  nm. Also, the  $V_{gs}$  has to be biased for at least 0.324 V, which is much more than that of Razavi (2010)'s topology of 0.2 V in 65 nm process node. Biasing every stage at half of the supply voltage,  $V_{DD}$  is planned for and reduction of the amplifier's gain is expected as the consequence of increasing the  $IP_3$ . Component Z in this design will be replaced by a balun to convert the two output signals to a single output signal.