ENHANCEMENT OF METHODOLOGY AND DEFINITION FOR SERIAL PROTOCOL ELECTRICAL SPECIFICATION COMPATIBILITY FOR NON-COMPLIANT FPGA

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By

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LIST OF ABBREVIATIONS

BGA	Ball Grid Array
BER	Bit Error Rate
CDR	Clock Data Recovery
CEI	Common Electrical I/O
CID	Consecutive Identical Digits
CPRI	Common Public Radio Interface
CTLE	Continuous Time Linear Equalizer
DCD	Duty Cycle Distortion
DFE	Decision Feedback Equalization
DJ	Deterministic Jitter
DLE	Decision Linear Equalizer
DUT	Device Under Test
EMI	Electro-Magnetic Interference
FPGA	Field Programmable Gate Array
ISI	Inter-Symbol Interference
LTD	Lock to Data
LTR	Lock to Reference
PCIE	Peripheral Components Interconnects Express

PDN	Power Distribution Network
PLL	Phase Lock Loop
RF	Radio Frequency
RJ	Random Jitter
RX	Receiver
SJ	Sinusoidal Jitter
TJ	Total Jitter
TX	Transmitter
UI	Unit Interval
VNA	Vector Network Analyzer

ABSTRACT

A new methodology and definition for a clearer compatibility for middle-range and low-end Field Programmable Gate Array (FPGA) transceiver is presented in this research. It has been a big challenge to balance between cost and performance in order to meet the full industrial protocol specification for middle-range and low-end FPGA. When the products are not able to achieve full protocol specification, the company will still market these products and claim that they are compatible. With this kind of situation, there are no guidelines can be followed; hence, users will not have confidence to design the product. In this research, a clearer compatible specification is obtained to provide channel loss requirement by extracting the timing margin at different test points. The research also ensures that quantifiable margin is allocated when compatible specification is defined. The middle-range FPGA that used in this research is Arria V GT device to define the new compatible specification with reference to IEEE 10GBASE-KR protocol where the compatible specification is used for board-based 10Gbps applications. The methodology used is by extracting the timing margin and find out the channel loss from 3 different test points which include Scenario 1) Transmitter is Arria V GT; Receiver is Compliant Receiver, Scenario 2) Transmitter and Receiver are from Arria V GT and Scenario 3) Transmitter is Compliant Transmitter; Receiver is from Arria V GT. 16-ps of timing margin is obtained from the research, while the channel loss for Scenario 1 is -16dB, Scenario 2 is -12dB and Scenario 3 is -17dB with error-free transfer for $BER10^{-12}$.

ABSTRAK

Metodologi dan definisi baru untuk keserasian yang lebih jelas untuk Get Tatasusunan Boleh-aturcara Medan (FPGA) dari kategori transceiver petengahan dan rendah dibentangkan dalam kajian ini. Bagi memenuhi spesifikasi protokol perindustrian yang penuh bagi pertengahan dan rendah FPGA merupakan satu cabaran besar untuk mengimbangi antara kos dan prestasi. Apabila produk tidak dapat mencapai spesifikasi protokol penuh, syarikat masih akan memasarkan produk-produk ini dengan spesifikasi serasi. Dalam situasi ini, tiada garis panduan boleh diikuti bagi pengguna. Oleh itu, pengguna tidak akan mempunyai keyakinan untuk mereka bentuk produk ini. Dalam kajian ini, spesifikasi serasi yang lebih jelas diperolehi untuk menyediakan keperluan kehilangan saluran dengan mengekstrak margin masa ini di tempat-ujian yang berbeza. Kajian ini juga memastikan margin yang boleh diukur diperuntukkan apabila spesifikasi serasi ditakrifkan. FPGA dari kategori pertengahan yang digunakan dalam kajian ini adalah peranti Arria V GT untuk menentukan spesifikasi serasi baru dengan merujuk kepada IEEE protokol 10GBASE-KRyang mana spesifikasi yang serasi ini digunakan bagi aplikasi 10Gbps berasaskan papan. Kaedah yang digunakan ialah dengan mengekstrak margin masa dan mendapatkan kehilangan saluran daripada 3 ujian yang berbeza iaitu Senario 1) Pemancar adalah Arria V GT; Penerima adalah Penerima yang mematuhi spesifikasi, Senario 2) Pemancar dan Penerima adalah dari Arria V GT dan Senario 3) Pemancar adalah Pemancar yang mematuhi spesifikasi; Penerima adalah dari Arria V GT. Keputusan yang diperolehi daripada kajian ini adalah di mana margin masa adalah 16ps, kehilangan saluran bagi Senario 1 adalah -16dB, Senario 2 adalah -12dB dan Senario 3 adalah -17dB dengan pemindahan bebas dari ralat untuk BER10^{-12}.

CHAPTER 1

INTRODUCTION

1.1 Background Study

In a serial link to communicate among several component, subsystem and organization, information technology and communication system have to establish a protocol to take care of the interaction between each other. Protocol compliance is a industrial protocol that are used to ensure the functionality of a system. Protocol compliant means exactly following the parameters and test methodology provided in the particular protocol and meeting the standard provided in the protocol.

However, for middle-range and low end Field Programmable Gate Array, meeting full compliance industrial protocol specification has been a big challenge. This is because of the need to have balance between cost and performance. Under many circumstances these products are not able to achieve full protocol specification compliance; some critical parameters have failed because of the architecture limitation. Re-architecture of the transceiver will be too costly and time consuming. Therefore, some company will still market these products as being compatible to the specification instead of being compliant. Protocol Compatible means performs the measurement slightly different but similar to the rules provided in that particular protocol.

With current situation, system margin requirements that help to ensure the system is functional within a defined boundary have not been stated. This creates many hurdles to

users, as extensive system simulations and validations are needed which involve a lot of man power, high-end equipment that are very costly.

Many methods of system testing have been done in the past, but all these tests only show functionality under several test setups. They do not provide the amount of margins available and the breakdown of the margins. The current ways of validating also do not have good linkage to the interoperability scenarios for some critical parameters of the industry specification.

Protocol compliance is important to ensure functionality of the system. When data transmission is being done across the link, various signal impairment will happen. Noise from clock source, Power Distribution Noise (PDN), crosstalk and channel attenuation will consume the margin for error free transmission.

In this research, several equalizers are used which include, Pre-emphasis, Continuous Time Linear Equalizer (CTLE), Decision Feedback Compensation (DFE) to obtain an optimized timing margin for the specification.

Pre-emphasis helps to boost up the high frequency component of the signal (Altera(a), 2013). Pre-emphasis is boosting the signal that is in the transmitter before entering device. However, CTLE is located at receiver. It is designed to boosts the frequency components attenuated by the backplane. It boosts the gain at higher frequencies to negate the effect of high frequency signal loss in the cable or backplane (Palermo (a), 2010; Choi, 2011). DFE is designed to compensate for the backplane attenuation due to insufficient bandwidth. DFE helps to cancel the post-cursor that cause by the insertion loss. It boosts the power of highest frequency component of receive data without

increasing noise power. DFE always used in conjunction with transmitter's pre-emphasis and receiver linear equalization (Altera(c), 2013; Austin, 1967; AgilentEE, 2013).

In this research, Altera FPGA that is from category of middle-range - Arria V GT device is used as the Device Under Test (DUT) as Arria V GT is low cost and low power performance device. Stratix V (SV) device is used as the protocol compliant unit for 10GBASE-KR protocol as this product is able to meet the specification for 10GBASE-KR protocol that defined by IEEE.

1.2 Problem Statements

For middle-range and low-end transceiver devices, meeting full industrial protocol specification has been a big challenge in terms of balance between cost and performance. When the products are not able to achieve full protocol specification, the company will still market these products and claim that they are compatible.

In this situation, users will not have confidence to design the product because there is no longer any guideline that can be followed. Hence, with these problem statements, compatible specification needs to be defined clearly.

1.3 Objectives and Scope of Study

The objectives of this research are

- To give users more clarity in specification compatibility for middle-range and low-end FPGA transceiver devices
- To provide channel loss requirement by extracting the timing margin at different test points and provide quantifiable margin for the compatible specification

The scope of study for this research include

a) Altera Arria V Data Sheet- Altera Arria V Data Sheet needs to be understood as this is the main device that is going to be used throughout the research. By understanding the features of Arria V, it can help in designing the programming file that controlling the FPGA.

b) Pre-emphasis, Decision Feedback Equalization and Continuous Time Linear Equalizer - These are the types of equalizer that help to improve the timing margin of the measurement. The equalizer settings need to be fined tune to an optimum settings. The higher the values of the settings are not necessary giving the best results.

c) S-parameters - S-parameter is able to determine the channel link loss that obtained from the measurement. It is able to measure the total link loss from the Ball Grid Array (BGA) to the test trace and all the connectors and cables that passing through.

d) Bit Error Rate - Bit Error Rate is use to determine the number of errors that occur in a certain bits. There are criteria that need to be fulfilled for the accuracy of the number of errors for example, the longer the bits send, the higher the Random Jitter (RJ) and it will cause errors where it will be explained further in Chapter 2.

e) 10GBASE-KR protocol - 10GBASE-KR protocol is the reference protocol that is going to be used throughout the research. 10GBASE-KR protocol is the protocol that is from 10-gigabit Ethernet that operate with backplane (IEEE, 2008). It is working at 10Gbps board base application.

f) The equipment that is going to be used in this research needs to be studied. The equipment including: BERTScope Analyzer, BERTScope Clock Data Recovery, BERTScope Digital Pre-emphasis Processor, Lecroy SDA Oscilloscope, Pattern Generator, Power Supply and etc.

CHAPTER 2

LITERATURE REVIEW

2.1 S-Parameters

In a two-port linear network as shown in Figure 2.1, a set of parameters that will completely characterize this network based on its terminal responses can be defined (Nelson, 2001).

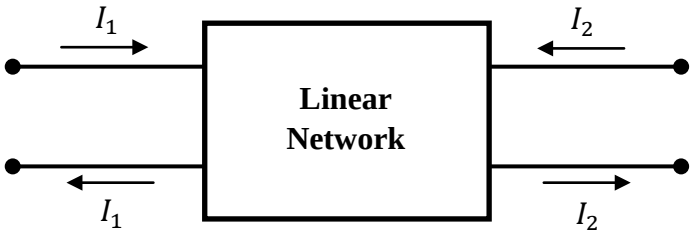

Figure 2.1 : Two-Port Linear Network (Stephen, 2009)

S-Parameters or also known as Scattering Matrix is able to describe a network of N-Ports in terms of incident and reflected signals that seen at each port. S-Parameters is introduced due to the high Radio Frequency (RF) and Microwave Frequency, as it is hard and tedious to measure by using Y-Parameters, Z-Parameters or H-Parameters.

Y-Parameters is known as admittance parameters, $I = YV$.

By referring to Figure 2.2, Eq. 1 can be obtained which is use to calculate the Y-Parameters value (Ramo, 2014),

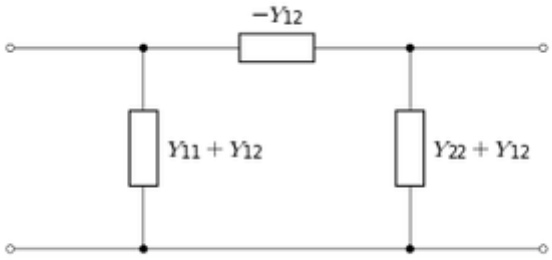

Figure 2.2 : Two Ports of Y-Parameters Equivalent Circuit (Stephen, 2009)

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} Y_{11} \\ Y_{21} \end{bmatrix} \tag{1}$$

where Y_{ij} , i is the port that the admittance is measured and j is the port where the admittance is injected.

Z-Parameters is known as impedance parameters, $V = ZI$. The Z-Parameters circuit is shown in Figure 2.3.

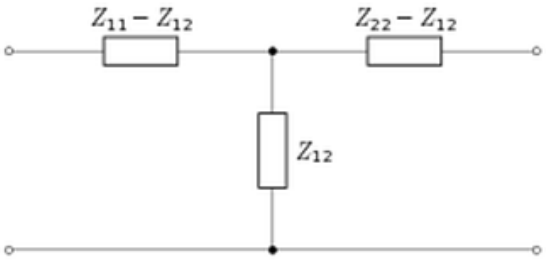

Figure 2.3 : Two Ports of Z-Parameters Equivalent Circuit (Raza, 2013)

The formula to obtain the Z-Parameters value is shown in Eq.2 (Ramo, 2014),

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_{11} \\ I_{21} \end{bmatrix} \tag{2}$$

where Z_{ij} , i is the port that the impedance is measured and j is the port where the impedance is injected.

Hybrid Parameters or H-Parameters are often to be chose when a current amplifier needed to be at the output. Figure 2.4 shows the equivalent circuit to obtain the H-Parameters value (DAE, 2014).

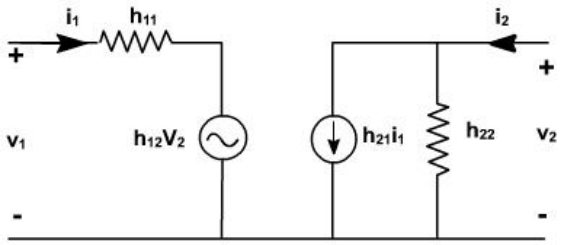

Figure 2.4 : Two Ports of H-Parameters Equivalent Circuit

Eq.3 shows the equation for H-Parameters that extract from the circuit in Figure 2.4,

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_{11} \\ V_{21} \end{bmatrix} \tag{3}$$

where H_{ij} , i is the port that the voltage and current are measured and j is the port where the voltage and current are injected.

From the Eq. 1-3 and the circuits shown, Y-, Z- and H-Parameters required current and voltage. Hence, with the high frequency technology, there are no equipment that is able to measure the RF or Microwave total current and voltage. While when doing the measurement, a perfect shorts or open is required which it is hard to achieve (Dunleavy, 2001).

Hence, under these circumstances, the only way to measure it is by measuring the measurable quantities voltage (Power) in terms of incident, reflected and transmission waves which are directly related to the reflection and transmission coefficient at the measurement ports.

Figure 2.5 is a two-port junction for S-parameters.

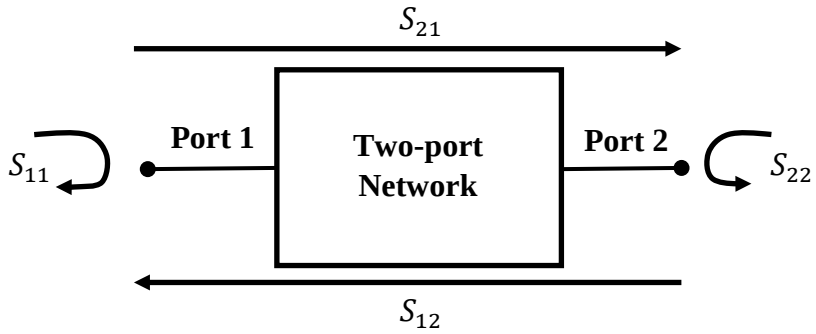

Figure 2.5 : Two-port junctions for S-parameters (Stephen, 2009)

The formula that used to define S-Parameter is as Eq. 4 (Ramo, 2014),

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_{11} \\ a_{21} \end{bmatrix} \tag{4}$$

where S_{ij} , i is the port that the power is measured and j is the port where the power is injected. For example S_{21} means that the power is measured at port 2 and injected at port 1. S_{11}, means that the square root of the ratio between the power reflected at port 1 over the power injected at port 1 (Stephen, 2009).

S-parameters can define return loss, insertion loss and crosstalk behaviors. Return loss is the reflected wave for example S_{11} or S_{22} while insertion loss is incident wave for example, S_{12} or S_{21}. Figure 2.6 shows the example of insertion loss and return loss for a cable. The channel loss is measured by using Vector Network Analyzer by passing through a signal to a certain length of cable to obtain the channel loss of the cable (Agilent, 2012).

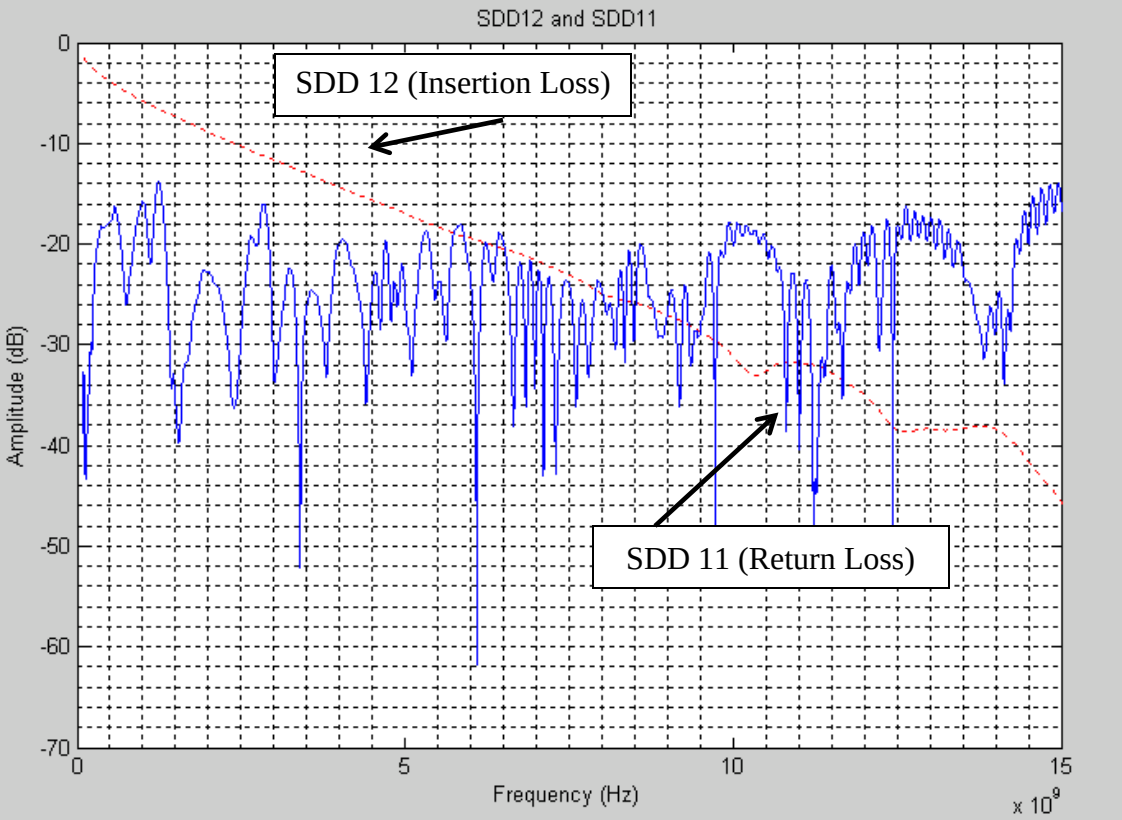

Figure 2.6 : Insertion loss and Return loss

2.2 Arria V GT device

Arria V family FPGAs offer the highest bandwidth and deliver the lowest total power for midrange applications (Altera(a), 2014). There are five variants in Arria V family, where it is shown in Table 2.1.

In this research Arria V GT device is chosen as the FPGA device as it is the device that operate at 10.3125Gbps. Arria V GT device is Altera low power and middle-range transceiver device. Arria V GT device is used to define the new compatible specification with reference to the 10GBASE-KR protocol where the compatible specification is used for board-based 10Gbps applications.

Table 2.1 : Arria V FPGA Family Variant (Altera(a), 2014)

Variant	Description
Arria V GZ FPGA	Highest bandwidth midrange FPGA with up to 36 backplane-capable 12.5Gbps transceivers.
Arria V GT FPGA	Lowest power midrange FPGA for applications that require up to 20 transceivers at 10.3125Gbps and SFF 8431 compliance
Arria V GX FPGA	Lowest power midrange FPGA for applications that require up to 32 backplaned-capable 6.5536Gbps transceivers
Arria V ST Soc	SoC with ARM-based HPS and 10.3125 Gbps transceivers
Arria V SX Soc	SoC with ARM-based HPS and 6.5536 Gbps backplane-capable transceivers

According to the handbook of Arria V GT as shown in Table 2.2, it is only support up to 6.55Gbps with backplane while in order to support beyond 6.5536 Gbps, Arria V GZ need to be used instead (Altera(a), 2013). Arria V GT device is design to support chip-to-chip in 10Gbps condition.

Table 2.2 : Arria V Variant across data rate

Variants	Hard Processor System (HPS)	Up to 6.5536 Gbps	Beyond 6.5536 Gbps
GX	N/A	Backplane	N/A
GT	N/A	Backplane	N/A
GZ	N/A	Backplane	Up to 12.5 Gbps with backplane support
SX	Yes	Backplane	N/A
ST	Yes	Backplane	N/A

In Altera Transceiver PHY IP User Guide, it mentioned that the devices that support 10GBASE-KR protocol are Arria V GZ and Stratix V device (Altera(b), 2013). However, to support 10Gbps data rate with backplane (Insertion Loss) is not impossible. It is still able to do so but with some workaround which this research is going to carry out.

2.3 Specification for 10GBASE-KR

One of the most stringent specifications for 10Gbps protocols is from 10GBASE-KR which requires low TX jitter, high channel loss and effective equalization at the RX (Chestnut, 2013). To define the compatible specification for the Arria V GT device, 10GBASE-KR transmitter and receiver margin is used as a reference.

By referring to the 10GBASE-KR specification (IEEE, 2008), the data pattern for TX and RX jitter measurements shall be tested pattern PRBS-31 and jitter specification are specified for BER10^{-12}. The Arria V GT device failed the TX jitter specification. Table 2.3 lists the 10GBASE-KR transmitter jitter specification.

Table 2.3 : Transmitter Characteristics for 10GBASE-KR (IEEE, 2008)

Parameter	Subclause reference	Value	Units
Signaling speed	72.7.1.3	10.3125 ± 100 ppm	GBd
Differential peak-to-peak output voltage (max.)	72.7.1.4	1200	mV
Differential peak-to-peak output voltage (max.) with TX disabled	72.6.5	30	mV
Common-mode voltage limits	72.7.1.4	0–1.9	V
Differential output return loss (min.)	72.7.1.5	[See Equation (72–4) and Equation (72–5)]	dB
Common-mode output return loss (min.)	72.7.1.6	[See Equation (72–6) and Equation (72–7)]	dB
Transition time (20%–80%)	72.7.1.7	2–47	ps
Max output jitter (peak-to-peak) Random jitter[a] Deterministic jitter Duty Cycle Distortion[b] Total jitter	72.7.1.8	 0.15 0.15 0.035 0.28	 UI UI UI UI

[a]Jitter is specified at BER 10^{-12}.
[b]Duty Cycle Distortion is considered part of the deterministic jitter distribution.

Table 2.4 shows the pre-emphasis requirement for 10GBASE-KR where the minimum post-tap ratio is 4dB while pre-tap ratio is 1.54.