DIGITAL PHASE LOCKED-LOOP WITH WIDE TUNING RANGE AND DYNAMIC PHASE SHIFT

BY

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Thank you ALLAH.

To my source of strength and inspirations; ibu, ayah, abang Izam & Ayu. Most supportive boss ever; Wai Tat Wong. My understanding supervisor, Dr Nur Syazreen. This, without doubt is impossible without all of you.

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LIST OF ABBREVIATION AND NOMENCLATURE

Abbreviation	**Meaning**
PLL	Phase Locked Loop
VCO	Voltage Control Oscillator
PD	Phase Detector
PFD	Phase Frequency Detector
CP	Charge-Pump
PVT	Process, Voltage and temperature variations
SPE	Static Phase Error

Terminology	**Definition**
Locking	A condition where VCO output and reference input are in phase and the frequency matched.
Lock Range	Range of input frequency where PLL able to stay lock. Mainly depending on VCO range.
Capture Range	Range of input frequency where PLL able to lock from unlock condition. Mainly depending on Phase Detector and Loop filter
Tuning range	Range where VCO frequency is linearly proportional to the change of its input voltage
Free Running Frequency	VCO frequency when no input applied
Lock time/Settling time	Time required for the PLL to lock itself on to the reference clock
Static Phase Error PLL	Error in terms of phase between input and output signal when is already in lock condition..
Jitter	variations of a signal from its original position in time

Symbols	Descriptions
V_{ctrl}	Control voltage
Φ_{err}	Phase error
Φ_o	Output phase
Φ_{ref}	Reference phase
Φ_{div}	Feedback phase
Φ_m	Phase Margin
I_{CP}	Charge-pump current
K_{VCO}	VCO gain
K_{PD}	Phase Detector gain (including charge-pump in PFD)
ω_c	Cut-off frequency
ω_{min}	Minimum frequency in VCO tuning range
ω_{max}	Maximum frequency in VCO tuning range
ω_{center}	Center frequency of VCO tuning range

ABSTRACT

For decades, Phase Lock Loop (PLL) has been widely used in numerous systems, such as telecommunications and digital design, where it plays significant role in improving overall system timing. Moving forward, with the latest revolution towards System-on-chip technology (SOC), the need of PLL in the form of Integrated Circuits has been growing tremendously.

Core of this research is to design a PLL with wide tuning range and dynamic phase shift feature, which is implemented in the Integrated Circuits level. In line with fierce competition and fast-paced semiconductor industry, PLL design with above features are definitely most sought after, as it will tremendously reduce turn-around time, cost and effort for a project.

Wide tuning range is achieved by introducing new Voltage Control Oscillator architecture, which will be able to provide wide tuning range without using very high $K_{VCO.}$ The new architecture proposed in this project is in differential input structure and consists of MOSFETs and capacitors; thus the area of implementation is small.

Besides, extra feature which is proposed in this PLL is Dynamic Phase Shift feature. Dynamically tunable phase shift is important since the accuracy of the phase could be adjusted without having to reprogram the PLL, thus saving a lot of time. Dynamic Phase Shift feature is a new idea, which its design is implemented by using UP/DOWN counters, OR and AND gates. The complete design includes synchronous system design work such as state machine, diagram and truth table for system simplification.

This proposed design achieved all specifications with wide-tuning range of 600MHz to 1300MHz is achieved with control voltage swing of 0.9V to 1.5V. Besides, the maximum static phase error measured in the simulation is 66ps, which is smaller than 200ps specification. Highest Period Jitter is 181ps while Cycle-to-Cycle Jitter is 55ps. Both types of jitter are within specification; lower than 300ps. Dynamic Phase Shift also successfully implemented where the UP/DN signal as the control to indicate either the phase is to be shifted up or down.

ABSTRAK

Litar Gelung Pengunci (PLL) telah lama dipraktikkan dalam pelbagai sistem elektronik seperti sistem telekomunikasi dan digital, yang mana ia berfungi untuk membantu sinkronisasi bagi isyarat secara keseluruhannya. Dengan revolusi teknologi elektonik, Sistem-atas-cip (SOC), keperluan untuk PLL di implementasikan dalam bentuk litar terpadu (IC) semakin berkembang.

Fokus dalam kajian ini adalah untuk menghasilkan PLL yang mempunyai julat frequensi yang luas, serta ciri istimewa ;alihan fasa secara dinamik, yang di implementasikan dalam litar persepadu (IC). Persaingan yang sengit dan pantas dalam dunia semikonduktor memerlukan tempoh rekabentuk yang singkat, maka, dengan julat variasi frekuensi yang luas, pelbagai aplikasi boleh menggunakan PLL yang sama, tanpa perlu untuk merekabentuk PLL dengan julat frequensi yang lain. Kedua-dua ciri yang disebut diatas amat berguna bagi pengguna PLL.

Julat frekuensi yang luas dicapai melalui rekabentuk baru litar pengayun kawalan voltan (VCO), yang mampu menghasilkan julat frequensi yang luas tanpa perlu menggunakan nilai K_{VCO} yang besar. Struktur litar ini terdiri daripada transistor MOSFET dan kapasitor. Oleh itu, saiz litar bagi rekabentuk ini adalah kecil.

Selain itu, ciri tambahan dalam litar gelung pengunci (PLL) ini adalah Alihan Fasa secara Dinamik. Pengalihan fasa secara dinamik ini amat penting untuk menjamin ketepatan fasa dalam isyarat yang dibekalkan oleh litar gelung pengunci, tanpa perlu mengkonfigurasi litar gelung pengunci dari awal operasi, justeru itu menjimatkan masa. Alihan Fasa secara

Dinamik merupakan satu idea baru yang di implementasi menggunakan litar penghitung (counter) dan litar digital OR/AND.

Rekabentuk yang dicadangkan ini berjaya mencapai kesemua spesifikasi yang ditetapkan, iaitu julat frekuensi dari 600MHz hingga 1300MHz, menggunakan voltan kawalan di antara 0.9V hingga 1.5V. Selain itu, perbezaan fasa antara isyarat input dan output juga kecil, sebanyak 66ps, berbanding spesifikasi maksimum yang ditetapkan, 200ps. Perbezaan frekuensi antara isyarat input dan output (jitter) juga kecil, dengan bacaan maksimum 181ps berbanding spesifikasi 300ps. Alihan Fasa secara Dinamik juga berjaya diimplementasi yang mana isyarat UP/DN merupakan isyarat kawalan yang menentukan samada alihan fasa yang di kehendaki adalah secara penambahan atau pengurangan.

CHAPTER 1

INTRODUCTION

1.1 OVERVIEW

A Phase-Locked Loop (PLL) could be simply visualized as a negative feedback system, where the output is used to track and compared with the input or reference signal. Specifically in PLL, the attribute of the signal which we are interested in tracking is the phase of the output signals relatively to its reference [8]. By using the mechanism implemented in PLL, the phase of output signal is forced to match the reference phase through adjustment of its feedback frequency. The point where both of these signals phases and frequency; output and reference are in-sync, this is called PLL locked state. Although highly undesirable, a small difference in terms of phase is to be expected and will be measured as it holds one of the most important characteristic of PLL.

1.2 MOTIVATION

The main motivation for selecting PLL as core of this research is due to its importance in electronic design, especially in digital system. To prove this importance, usages and applications of PLL in electronic system will be discussed here.

One of the most significant roles of PLL is to keep the timing of the whole system uniformed and synchronized [8]. To put it in a concept, clock distribution architecture normally consist mere buffers to recover the edge-rate of the signals, which however, will also produce delays from the origin to the destination point. Adding in a complicated and large scale design, for

example transceiver into the picture, thousands of buffers are employed; creating delays everywhere in the paths and in the end causing numerous timing mismatches. With PLL in the system, the input and output phases are forced to be aligned, thus the delays are compensated and the timing of the whole system could again be synchronized. Due to that reason, PLLs are found in a wide range of applications, especially in this digital era, where clocking is becoming the heart of each system.

Besides clock recovery and synchronization role, PLL is also widely used for frequency synthesis especially in the RF transceivers [5]. This function is enabled by adding-in input or output counters which act as frequency divider. Therefore, besides the ability to adjust the frequency of output signal to match its reference as mentioned above, PLL also able to produce the frequency by a factor of its reference. In this particular usage, PLL is often called as a frequency synthesizer.[5]

Furthermore, it is also widely used as noise and jitter suppression in communication system. As noise is highly undesirable in any electronic system, many noise suppression methods are explored and implemented [8]. Among simple yet effective noise minimization efforts are including filtering and feedback. Filters are often used to remove the noise outside the desired bandwidth; at the frequency lower and higher than intended, while negative feedback approach will be able to reduce noise within the intended bandwidth. The feedback signal from the output is in 180° phase relation to the reference (called anti-phase) contains both output and noise signal. Thus, when the anti-phase noise is being added-back, it will reduce the noise generated within the closed loop, by a factor of $1+A\beta$; where A is the open loop gain and $A\beta$ is the loop gain. PLL has both of these properties; band-pass filters and negative feedback; which makes it great noise and jitter suppressor.

Having the importance of PLL emphasized above, it is obvious that this topic is among highly attractive subject of research. Due to its wide and multi-purpose usage, further improvement on the features would be highly beneficial to all.

1.3 PROBLEM STATEMENT AND CONTRIBUTION

While there are many outstanding researches targeting to improve the key performance of the PLL itself, the research and design work in enabling extended features and flexibility of PLL is relatively fewer.

Looking in a bigger picture, due to its wide application, PLL could be improvised and designed to achieve higher flexibility as an answer to support various multi-frequency applications. While improvising the key performance of PLL could bring more accuracy or shorten locking or processing time, improvising PLL in terms of flexibility expand the market target. For example, with narrow tuning range PLL, a customer needs to acquire two different PLLs for different standards, although integrated in one system; for example Double-Data Rate memory (DDR) and Low Voltage Differential Signaling (LVDS) buffer. From the standard, DDR2 operates at 200Mbps [1] while high speed LVDS SERDES could be running at 655Mbps or higher [2]. In case of a narrow tuning range is being employed, the system designer will need to get two sets of PLL targeting different frequency range.

While there is another popular option available where a PLL tuning range could be widen by increasing the supply voltage, this method has becoming less favored due to the reason higher supply voltage will definitely cause higher power consumption.

Main contribution of this research is in producing a solution for the above problem by designing a wide tuning range PLL, which brings flexibility in the supported frequency

range. Besides, dynamic phase shift feature is also added as a bonus, to boost the accuracy performance.

This PLL is expected to be using digital component such as Phase Detector, counter and digital mux, as well as analog circuits; such as Loop filter, charge-Pump and Voltage Controlled Oscillator. With the combination of high speed and smaller area of digital component and higher sensitivity and accuracy in analog blocks, this PLL is aimed to be at the top of its class and be at par in the industry standards, which will be clearly shown in the comparative results in Chapter four.

Besides, from business and project management perspective, a wide-tuning range PLL will enable re-use and multi-instances of this PLL, thus reducing a product development turnaround time and reducing costs and effort- the perfect solution in gaining an upper hand in this fierce electronic market.

Again, by having a wide tuning range, most application will no longer need specific or customize type of PLL for low or high frequency application. In other words, by having wide tuning range, the proposed PLL could be used as general PLL which is suitable to most application.

Besides, wide tuning range of PLL is also beneficial in lowering power consumption of the system. In a digital system, although the clock is always transmitted, there will be area sub-systems which are not in use. By lowering the frequency of the clock in the un-used functions or sub-systems, the power consumption could be lowered too. Therefore, wide tuning range is desirable in order to help the overall power consumption.

Furthermore, dynamic phase shift feature provides a clever solution to achieve high accuracy without the need to go thru lengthy procedure of reconfiguration, thus save processing time.

1.4 SIMULATION TOOLS AND PROCESS

Design work presented here is implemented in 55nm, TSMC process and using HSPICE as simulation tools. Since this is an actual fabricated product, there are detail information which will not be disclosed due to confidentiality policy.

1.5 CHAPTER ORGANIZATION

This dissertation contains six chapters; Introduction, Literature Review, PLL Theory and analysis, Proposed Design of Wide Tuning Range PLL with Dynamic Phase Shift Feature, Conclusion and Discussion and finally, References.

Chapter two will discuss on the previous notable researches done on PLL.

In Chapter three, PLL theory and concepts, as well as the sub-blocks design. Among the highlighted topics are PLL basic operations, Phase Detector analysis and types, Charge pump operation and concepts, Loop filter usage, concept and architecture. Lastly, Voltage Control Oscillator (VCO) usage and theory will be discussed. The intention of this chapter is to prepare readers for the basic background and operation of PLL.

Chapter four contains detail design procedures of the proposed PLL. Since focus of this research is in widen tuning range and adding in a feature called dynamic phase shift, complicates concept and complex design procedures such as root locus analysis will not be

covered in this chapter. However, basic design of loop filter for stability and transfer function derivation of proposed PLL will definitely be covered in this chapter. Next, the improved architecture which would enable both of the above features is presented. At the end of this chapter, results are attached and presented.

Chapter five captures conclusion on the findings and plausibility of the proposed design and discussion of possible future work.

Finally, all the references are listed in the Reference section.

CHAPTER 2

LITERATURE REVIEW

This chapter intends to discuss on the history and background of PLLs, types as well as improvements as in previous works and researches.

2.1 PLL History and Background

Earliest research of Phase Locked Loop (PLL) is dated back to 1932, which resulted from a study by British researches in developing an alternative to Edwin Armstrong's superheterodyne receiver. In early 1930's superheterodyne receiver was regarded as invention of the time and was widely used. However, due to number of stages which needed to be tuned in a superheterodyne system, a simpler method was desired and led to the discovery of the Homodyne or direct-conversion receiver. In In the homodyne system, a local oscillator was tuned to the intended input frequency while the output is multiplied by the input signal, resulting an output signal with original audio modulation information. However, the performance of homodyne was affected by slight drift of the local oscillator frequency. Solution of the drifting oscillator was later solved by a French scientist, whom employed an automatic correction signal to the oscillator and therefore maintaining it in the same phase and frequency as the intended signal. The technique was described in 1932, in a paper by Henri de Bellescize, in the French journal *L'Onde Électrique*.[3][4][5]

In late in 1930's, PLL was employed in analog television receivers to synchronize horizontal and vertical sweep circuits. A line of monolithic circuits with complete PLL system on the

same chip, susch as NE565 by Signetics was introduced in 1969, thus further widening the usage of PLL[6]

2.2 Types of PLL

Since its widespread usage and extreme importance, many profound work and researches have been done in developing several variations of PLLs. Among the variations, the earliest of PLL generation to be found is analog phase-locked loop (APLL) also referred to as a linear phase-locked loop (LPLL), which working in all analog principles. In APLL, analog multiplier is used as the phase detector, loop filter is either passive or active and the usage of Voltage Control Oscillator (VCO) as the local oscillator. Further enhancement aiming for higher phase accuracy and speed resulting the second generation of Digital PLL (DPLL).detection, the differences of APLL and DPLL is the implementation of Digital Phase Detector in DPLL, such as JK Edge trigger flip-flop, Exclusive OR and the most popular one, Phase Frequency Detector (PFD). As proven from previous work, by introducing Digital Phase Detector, DPLL could achieve further phase accuracy and wider lock range, due to the linearity of its Digital Phase Detector. Latest generation of PLL substitutes all the analog components in PLL with digital, where the aim for this revolution is the higher frequency for processing speed. This type of PLL is called All-Digital PLL (ADPLL), in which digital loop filter, such as Time-to-Digital converter (TDC) is used to replace the conventional lopp filter and Digitally-Controlled-Oscillator or Numerically-contolled-Oscillator (NCO) as the substitutes of VCO. Software version of PLL , (SPLL) also made available where all the functional blocks are implemented by software, rather than hardware.[7]

All of the types of PLL above have their own strengths and drawbacks, therefore careful selection need to be done based on the ultimate goal of intended PLL development. For this

research, DPLL is chosen due to its low to medium frequency range of operation and wide locking range (linearity of PFD)[8] . Besides, one of the advantages of DPLL, since it is still maintaining analog components; charge-pump, filter and VCO, where the biggest static phase error could be controlled by matching charge-pump current, for pull-up and pull down.

2.3 Existing Work in PLL Wide Tuning Range and Phase Shift Accuracy

Regarding the topic of interest; wide tuning range of DPLL, there are also numerous researches have been done in this subject of matter. While the frequency target in some of these literatures are much higher that the frequency of interest in this research, it is no doubt still highly beneficial to review and study these existing profound works.

Guansheng Li et al [9] present a low phase noise and wide tuning range Quadrature VCO. In this paper, low-phase-noise and wide tuning-range quadrature oscillator is designed using an LC-ring resonator. It achieves low phase noise by employing inductor and passive coupling between stages. The proposed design consist four-stage LC-ring prototype in a 65nm CMOS process covering 2.78GHz - 5.00GHz tuning frequency. Besides, wide tuning range obtained having multiple resonant modes. In order to cover certain frequency range, user would need to switch between the resonant modes. Besides, this paper also addressed issue of uncertainty in oscillation frequency which is common issue in oscillators with multiple oscillation modes. To solve this issue, a novel mode switching method is proposed which make use of phase relation of high-order resonant signals to realize mode-dependent energy injection. This is possible due to the reason the mode selection relies on energy loss and energy injection. In the proposed work, whenever switching between modes took place, current will be injected to the intended modes so that only the intended resonant mode gets enough energy compensation to sustain the oscillation frequency in that particular mode. Simulated phase

noise is 186dB at 3.66GHz and >180dB across the entire tuning range. While the design, implementation and results obtained are outstanding, the biggest drawback of this design is its huge area of implementation. This is fully expected when using inductor as components in the ring oscillator. Based on this work, the area used for this type of VCO is 1mmx1mm. Since the VCO in this project is intended to be used in PLL and integrated in FPGA, such huge area of implementation is not acceptable.

You Lu et al. [10] present a tuning range of VCO is from 52.2 GHz to 61.3 GHz for a supply voltage as low as 0.7V, implemented in 90 nm CMOS technology. This is a novel design, incorporating variable inductor (VID) techniques, which consists a transformer and a variable resistor. The tuning of VCO voltage is through adjustment on its resistor. This is an outstanding approach of tuning VCO frequency without sacrificing their operating frequencies. VCO and DCO are both fabricated in 90 nm CMOS technology. Maximum phase noise from this design is about -118.75dBc/Hz at 10-MHz offset, with maximum current of 12.4mA. This existing work is very practical and managed to achieve high frequency range, without the need of high supply voltage. However, this existing work is not a perfect fit to be utilized in this project due to the complexity of the design; which incorporated VCO and DCO, as well as the frequency range target for this project is much lower than frequency ranges in this work. It is worth highlighting, while meeting specification is mandatory, over-designing a system or circuit is undesirable since it will cause unnecessary effort and cost.

Zhenbiao Li et al. [11] worked on VCO with tuning range of 667 MHz to 1156 MHz on 1.5V supply voltage, using 180nm CMOS technology. This design employed the usage of switched

resonators, which results in the ability of VCO to achieve wide tuning range. The switched resonator is constructed using top stacks of PMOS, the second stack is NMOS, while the most bottom transistor is PMOS bias transistor. Inductors are placed in between top and second stack and the input/output stage. Maximum phase noise achieved for this design is -124.2 dBc/Hz. Major limitation of this design is it needs three different voltages; tuning voltage, center voltage and bias voltage. For a larger system design such as PLL, such multi-voltages supplies are undesirable since more analog voltages to be produced, more caution needed to ensure the voltage levels are sufficient and correct and will directly impact the performance and functionality of the circuit or system.

Bodhisatwa Sadhu et al [12] present design techniques for optimizing the switched-capacitor array in a wide tuning range LC VCO. This work is using 130nm CMOS process. The switches in the capacitor array are optimally sized, in binary-weighted structure to maximize the tuning range. Additionally, parasitic interconnect inductance inherent in the capacitor array is used for increasing the equivalent capacitance value. This work achieved tuning range from 850MHz to 7.1GHz with phase noise between −107.1 and −119.1 dBc/Hz at 1MHz offset with maximum of 15 mW power consumption. Major limitation of this work is the interconnect capacitor and inductor is designed to be in binary weighted, therefore, any mismatches will have huge impact the capacitor bank step sizes and total values. Furthermore, each interconnects and wires will have their own parasitic capacitance, which will also be accumulated into total capacitance. Therefore, not only the physical interconnect capacitors need to be design for matching, but also the length and loading of each routed also need to be taken care and matched as much as possible. In short, this work need very through layout implementation to eliminate any possible mismatches which will results in inaccurate capacitor bank values.

Te-Wen Liao et al [13] present a low phase-noise phase locked loop (PLL) system with a Multi-Phase Over-Sampling Charge Pump (MPOSCP) for wireless applications. This design is implemented in 1.2V V_{DD}, 90nm CMOS process. Basic concept of this work is to use over-sampling charge-pump to reduce the noise on the control voltage of the ring voltage-controlled oscillator (VCO). This paper stressed more on the work of noise suppression to compensate on the inferior noise suppression in ring oscillator. Excellent small area of implementation is obtained in this work; 0.046mm2 with the total power consumption of 7 mW. The PLL achieved phase noise below -100 dBc/Hz. The only limitation of this work is due to its insufficient tuning range of 350MHz to 700MHz.

Luca Fanori et al. [14] present a development of 6.7-to-9.2GHz 55nm CMOS Hybrid Class-B/Class-C Cellular TX VCO. This work is focused on WCDMA application. Basic VCO structure being used in this design is using LC tank, while the class A, B and C is referring to its architecture which directly impact the power consumption of this VCO. This design is targeted to be compliant with the phase-noise specifications of cellular transmitters. This work produced phase noise of 169dBc/Hz on 1.5V VDD. Although the same process which is to be used in this project matched with this existing work, target frequency to be used is much lower than presented in this work. Besides, as the work itself, some improvement is needed to achieve lower phase noise.

Among the existing work on Phase Shift accuracy and adjustment are discussed next.

Dong Jiao et al [15] present an adaptive phase-shifting PLL that can achieve optimal clock data compensation by digitally programming the supply noise sensitivity and the phase shift of the PLL clock period. The proposed system consist of a frequency-phase detector, a charge pump, a low-pass filter, a supply tracking modulator, a differential voltage-controlled oscillator (VCO) and a frequency divider. The phase shift and noise sensitivity adjustment are