A STUDY ON POWER REDUCTION TECHNIQUES FOR COMPARATOR BASED ON BODY BIASING

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A STUDY ON POWER REDUCTION TECHNIQUES FOR COMPARATOR BASED ON BODY BIASING

By

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

ABBREVIATIONS	DESCRIPTION
ADC	Analog to Digital Converter
CAD	Computer Aided Design
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
DRC	Design Rule Check
FPGA	Field Programmable Gate Array
GIDL	Gate Induced Drain Leakage
GND	Ground
ITRS	International Technology Roadmap for Semiconductor
LVS	Layout Versus Schematic
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MTCMOS	Multi Threshold CMOS
NMOS	N Channel MOSFET
PEX	Parasitic Extraction
PMOS	P Channel MOSFET
RC	Resistance Capacitance
SCCMOS	Super Cut-off CMOS
SRAM	Static Random Access Memory

LIST OF SYMBOLS

SYMBOL	DESCRIPTION
V_{BS}	Bulk source voltage
V_D	Drain voltage
V_{DD}	Drain supply
V_{DS}	Drain source voltage
V_G	Gate voltage
V_{GS}	Gate source voltage
V_{IH}	Input upper limit
V_{IL}	Input lower limit
V_{IN}	Input voltage
V_N	Inverting input
V_{OH}	Output upper limit
V_{OL}	Output lower limit
V_{OS}	Offset voltage
V_{OUT}	Output voltage
V_P	Non-inverting input
V_{SS}	Source supply
V_{TN}	NMOS threshold voltage
V_{TP}	PMOS threshold voltage
V_{BP}	PMOS bulk biasing
V_{BN}	NMOS bulk biasing

KAJIAN TERHADAP TEKNIK PENGURANGAN KUASA UNTUK PEMBANDING BERDASARKAN PINCANGAN BADAN

ABSTRAK

Perkembangan peralatan elektronik mudah alih dalam pasaran pengguna telah membawa kepada inovasi reka bentuk kuasa rendah. Tambahan pula, pengecilan skala proses teknologi CMOS telah meningkatkan kepadatan transistor dalam sesuatu peranti. Hasilnya, peranti tersebut mempunyai lebih banyak fungsi tetapi lebih banyak kuasa digunakan oleh satu unit kawasan. Jadi, teknik pengurangan kuasa sedang giat diterokai dalam rekabentuk litar sepadu elektronik. Dalam penukar analog kepada digital kilat, pembanding adalah pengguna kuasa terbanyak. Dalam penyelidikan ini, teknik pengurangan kuasa seperti teknik memutuskan CMOS (SCCMOS), teknik transistor "sleepy", teknik timbunan transistor dan teknik pincangan badan telah dikaji. Pembanding konvensional, pembanding dengan pengurangan V_{DD} dan pembanding dengan SCCMOS dan timbunan transistor dilaksanakan dengan menggunakan proses teknologi CMOS 0.13 μm. Kemudian, pembanding kuasa rendah dicadangkan dengan menggunakan teknik SCCMOS, teknik "sleepy" dan timbuanan transistor serta teknik pincangan badan. Pincangan badan kehadapan digunakan untuk mengurangkan voltan ambang. Hasilnya, V_{DD} dapat dikurangkan. Seterusnya penggunaan kuasa dinamik turut berkurangan. Sementara itu, SCCMOS dan timbunan transistor "sleepy" digunakan untuk mengurangkan arus bocor. Daripada simulasi pasca-rangka lantai pembanding yang dicadangkan, kuasa statik ialah 94.6

pW berbanding 404.2 µW untuk pembanding konvensional. Sementara itu, kuasa dinamik untuk pembanding yg dicadangkan ialah 14.76 µW berbanding 1.127 mV untuk pembanding konvensional. Simulasi pasca-rangka lantai dan simulasi pra-rangka lantai menunjukkan tiada kesan parasitik yang ketara terhadap prestasi pembanding yang dicadangkan.

A STUDY ON POWER REDUCTION TECHNIQUES FOR COMPARATOR BASED ON BODY BIASING

ABSTRACT

The growth of portable electronic devices in consumer market has led to the innovation of low power design. Furthermore, the scaling down of CMOS process technology has increased the transistor density. As a result, the device has higher functionality but more power is consumed per area unit. Hence power reduction technique is being explored in electronic integrated circuit design. In flash analog to digital converter (ADC), comparator consumes the most power. In this dissertation, power reductions techniques such as sleepy transistor technique, stack transistor technique and body biasing technique are studied. A conventional comparator, comparator reduced VDD and comparator with super cut-off CMOS (SCCMOS) and sleepy stack are implanted using 0.13 μm CMOS process technology. Then, a low power comparator is proposed using body biasing technique, sleepy stack transistor and super cut-off CMOS. Forward body biasing technique is used to decrease the threshold voltage. As a result, V_{DD} is able to reduce. Hence, dynamic power consumption also reduced. Meanwhile, SCCMOS and sleepy stack transistor are used to reduce leakage current. As a consequence, the static power is reduced. From pre-layout simulation of proposed comparator, the static power is 94.66 pW compared to 404.2 μW for conventional comparator. Meanwhile, the dynamic power for proposed comparator is 14.76 μW compared 1.127 mV for conventional comparator. The pre-layout

simulation and post-layout simulation show there is no significant parasitic effect on the performance of proposed comparator.

CHAPTER 1

INTRODUCTION

This chapter introduces the background of this study as well as the problem statement. This chapter also presents the objectives and the scope of this study. Besides that, this chapter also presents the contribution of this study. Last but not least, this chapter presents the overview of this thesis.

1.1 Background

Nowadays, there are many portable or battery operated electronic devices available in the market. The electronic portable devices such as smartphone, tablet pc and laptop are small in size so that it can be easily carried. Moreover the portable electronic devices also have been adopted in medical field. The portable medical electronic devices such as portable blood pressure monitor and portable glucose meter have showing significant growth recently. Since the size of portable device is a limitation, the size of battery in portable electronic device cannot be traded-off for a powerful battery. Hence these devices have to consume a very low power so that the life of the battery can be prolonged. The battery life is affecting the performance and reliability as well as the portability of a device.

The heart of a portable electronic device is integrated circuits which consist of millions of transistors. Moore's Law states that the number of transistors on integrated circuit doubled every two years. This is due to shrinking of CMOS technology. The performance of the device is enhancing as many system component can be combined on single chip (Moradi et al., 2011). However as more transistors on a single chip, the power consumption also increases.

Generally there are two types of power that contribute to the overall power consumption which are the dynamic power and the static power as shown in Figure 1.1 (Weste and Harris, 2005). The dynamic power is the power consumed by the device during switching from one state to another state. The static power is the power consumed during inactive state. The current that flow during this state is known as leakage. As CMOS technology keeps scaling down, the leakage current has increased exponentially. According to the International Technology Roadmap for Semiconductor (ITRS), the contribution of leakage to the overall power consumption is consistently increase as the size of the device getting smaller. The static power is exceeding the dynamic power consumption as CMOS technology drop below 65 nm (Kim et al., 2003)

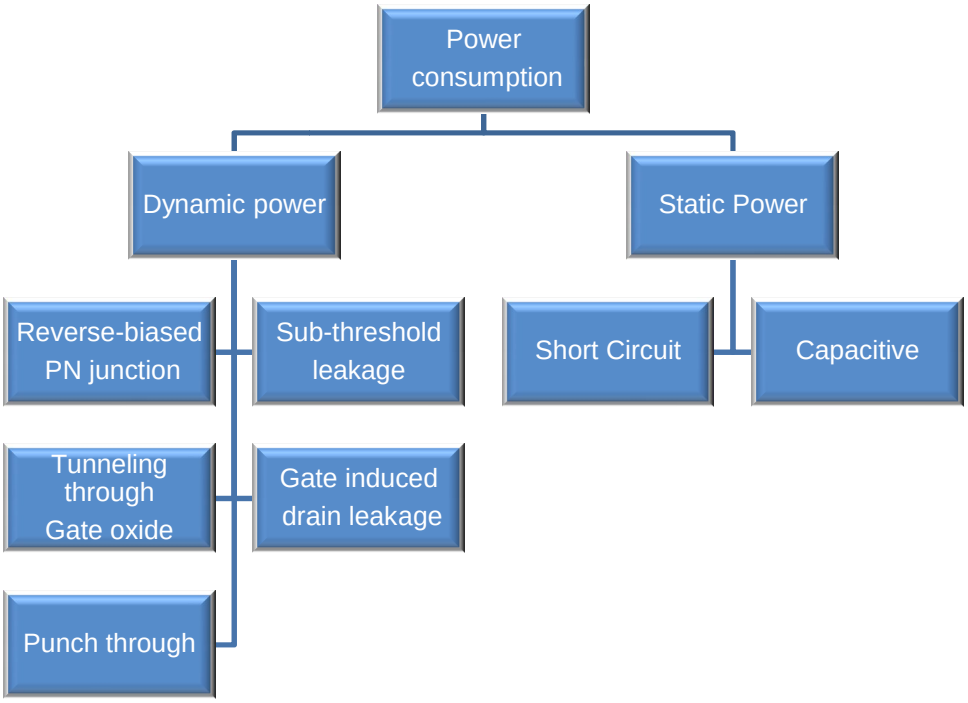


Figure 1.1: Power consumption (Weste and Harris, 2005)

Power consumption techniques can be applied at different levels such as process technology level, logic and circuit level, architecture level, algorithmic level and system level. Following are the details discussion of each level.

I. Process Technology

Technology scaling has reduced the voltage supply and threshold voltage (Baschirotto et al., 2009). Reducing the power supply is the most effective way to reduce power

consumption. However when power supply is reduced, it will cause the delay to increase. One of the power reduction techniques at gate level is gate gating.

II. Logic and circuit level

Power consumption at this level can be reduced by applying circuit technique that minimizes the count of transistors. Appropriate transistor sizing, scaling down supply voltage, use multi V_{TH} logic circuit and low V_{TH} transistor also can reduce power consumption. Besides that, power consumption also reduced when switching activity is reduced. Logic optimization is one of the ways to reduce switching activity.

III. Architecture level

At this level, parallelism, and pipelining or combination of both parallelism and pipelining can be used to reduce power consumption. Besides that, power management technique that shutting down part of the circuits on stand-by mode also a good way to reduce power consumption.

IV. The algorithmic level

Power consumption at this level is able to reduce by using algorithm that reduces the number of operations. With reducing the number of operation, the hardware is reduced as well. A good coding that taking into account the statistics of the input signal can minimize switching activity which also reduces power consumption.

V. System level

At system level, integrate analog peripherals and off-chip memories on the same chip can reduce power consumption. By using low frequency clock for system clock while use phase locked loops to generate higher frequency for internal clock also a method to reduce power consumption.

There are various techniques have been developed to reduce the static and dynamic power consumption at logic and circuit level. The most common techniques such as clock gating and multi-voltage threshold optimization are introduced to overcome both the dynamic power and static power consumption (Qureshi and Sanjeev, 2009). In clock gating, the clock is disconnected from the device during inactive state. For multi-threshold voltage optimization, the high threshold voltage cell is used instead of low threshold voltage so that the leakage current is minimized. Since few decades ago, the CMOS technology keeps scaling down. The density of integrated circuit on die is improved. However the leakage current is increased as the channel length has becomes shorter. Figure 1.2 shows the leakage current trend provided by International Technology Roadmap for Semiconductor (ITRS).

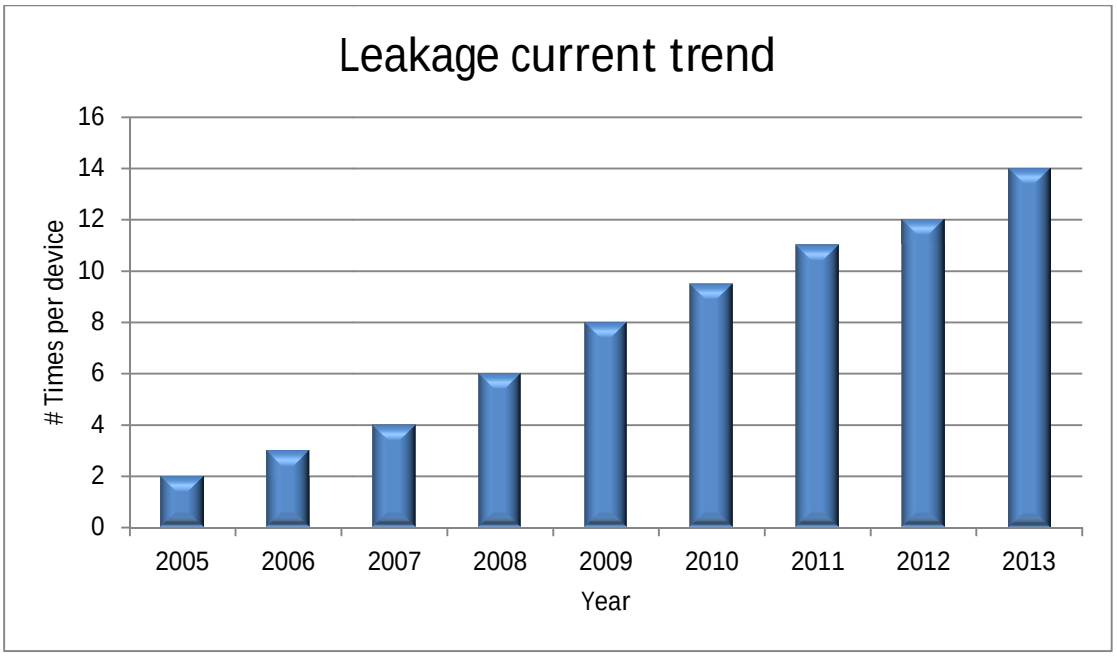


Figure 1.2: Leakage current trend (ITRS, 2005)

The advance techniques such as multi-voltage and power gating have been developed to overcome the static power issues. Different voltage levels are used for different areas in multi-voltage technique. The high voltage supply and low voltage supply are connected to area according to the supply level needed. In power gating, the supply is completely removed from the unused area. Sleep and stacked transistor are also the techniques that can reduce power consumption (Park and Mooney, 2006: Pal et al., 2010). In a power reduction study, super cut-off CMOS technique has been proposed as the most efficient leakage power saving (Anjana and Kumar, 2013). Besides that, there is body biasing technique that can be used to reduce the threshold voltage. The circuit consume less power as supply voltage is keep lower than threshold voltage in the sub-threshold region operation (Niranjan et al., 2011). Others low power techniques are such as sub-threshold, bulk driven MOSFET, floating gate MOSFET and level shifter approach can be applied to reduce static power consumption (Ibrahim, 2013).

1.2 Problem Statements

In previous works, power reduction technique is mostly applied in the digital circuit such as inverter (Park and Mooney, 2006), Schmitt trigger (Niranjan et al., 2011), full adder (Pal et al., 2010; Anjana and Kumar, 2013) and SRAM (Chowdhury et la., 2012) instead of analog circuit. This is due to the complex design of analog circuit. Among all the analog integrated circuit, comparator plays the important role in many applications such as analog to digital converter (ADC) and level shifter. A comparator compares two analog signals and produces a digital output. This behaviour makes comparator becomes the main component in ADC. Since all signals such as sound, light, pressure and temperature are exist naturally in analog. In order to make use of the analog signal in digital system, ADC is used to convert the analog input signal to digital output signal. The important of comparator is very significant in flash ADC as the number of comparator used in this flash ADC architecture increase exponentially as the resolution increase. In previous study, comparator has shown as the component that consumes the most power in flash ADC. The power consumed by comparator is 87% from the overall power consumption (Osman, 2013). Low power consumption and high speed is important feature of many ADC design to reduce energy use or to minimize heat dissipation to lower cooling and packaging costs (Halim et al., 2011).

Hence, the first part of this research is focused on the study of the available power reduction techniques. This is due to the lack of literature on power reduction technique for analog circuit. Among all analog circuit, the comparator is the most important block in flash ADC. Therefore, a

low power comparator design is proposed using super cut-off CMOS, sleep transistor and body biasing techniques

1.3 Objectives of Research

Below are the objectives of this research:

I. To study and analyze the available power reduction techniques.

II. To design a low power comparator using power reduction techniques to reduce dynamic power and static power.

III. To compare the performance of the proposed comparator with the conventional comparator.

1.4 Scope of Research

This study is focuses on power reduction techniques and applies the circuit level technique on an analog circuit which is comparator. A low power proposed comparator is designed using sleep transistor, super cut-off CMOS (SCCMOS) and body biasing technique. The schematic is carried out using Virtuoso Schematic Editor from Cadence ™ while the layout is carried out using Virtuoso Layout Editor also from Cadence ™. The technology used in this work is Silterra 0.13 μm CMOS technology.

1.5 Research Contribution

The following are the contributions of this study:

1) Contributes to the knowledge in low power reduction techniques. The circuit level techniques such as stack transistor, sleep transistor and body biasing are studied in this study. The effect of forward body biasing on NMOS and PMOS is also investigated and analysed.

2) Present method on applying low power reduction techniques for analog design. Power reduction for digital design such as sleep and stack transistor have been studied widely. These techniques are effective for digital design. Analog design is more complicated compared to digital design. Hence this study focuses on power reduction for analog design. The power reduction techniques which are sleep and stack transistor as well as body biasing have been demonstrated also effective for analog design.

1.6 Thesis Overview

This thesis consists of five chapters as describe below:

Chapter 1 provides the background and problem statement of this research. The objectives, scope and contribution of this work also have been discussed in this chapter.

Chapter 2 describes the literature review of power consumption. Each of the components in power consumption is discussed. This chapter also discussed the type as well as the advantage and disadvantage of power reduction techniques. Besides that, the characteristics and type of comparator are also discussed.

Chapter 3 focuses on the methodology used in this work. This chapter also presents the schematic of the conventional comparator and the proposed comparator as well as the explanation of the circuit operation. Besides that, this chapter also presents and explains the layout of the proposed comparator.

Chapter 4 presents the result of this study. This chapter also includes the comparison of result between conventional comparator and the proposed comparator. The results are from pre-layout simulation and post-layout simulation. Besides that, this chapter also presents the analysis and discussion of the result.

Chapter 5 contains the conclusion of this work. Further enhancement and recommendation of this work are also discussed in this chapter.

CHAPTER 2

LITERATURE REVIEW

This chapter reviews the literature on power consumption of integrated circuit which consists of static power and dynamic power. This chapter also reviews each of the components in static power and dynamic power. Then, this chapter reviews the techniques for low power design for analog and digital circuit. Last but not least, this chapter reviews the characteristics and types of comparator.

2.1 Power Consumption

There are two elements that contribute to the total power consumption of a circuit which are static power and dynamic power. The total power consumption is dominated by dynamic power. In FPGA, the dynamic power consumes as much as 90% and only 10% is consumed by static power (Vijayakumar at al., 2013). However, as the size of CMOS technology keeps shrinking to 90 nm and below, the static power has dominated the total power consumption and becomes major concern in designing integrated circuit (Patel et al., 2014).

2.1.1 Static Power

The static power is consumed during transistor in OFF state due to the leakage. Ideally there will be no current flow during OFF state. As long as $V_{IN} < V_{TN}$ or $V_{IN} > V_{DD} + V_{TP}$, the static power is zero. However, there will be significant leakage for smaller technology such as 90 nm and below (Von Armin et al., 2005). For an inverter in Figure 2.1, the leakage currents are such as gate leakage, sub-threshold current and drain junction leakage. The threshold voltage has been decreased in smaller technology which causes the leakage current increases. Hence static power which caused by leakage current becomes more significant in smaller technology then in technology that greater than 90 nm. There are few components that contribute to the leakage current which will be discussed more in the next following sub-topics. The overall of static power consumption is the product of total leakage current and supply voltage. The static power can be obtained using equation 2.1.

$$P_{static} = \sum (\text{leakage current}) \times (\text{supply voltage}) \quad (2.1)$$

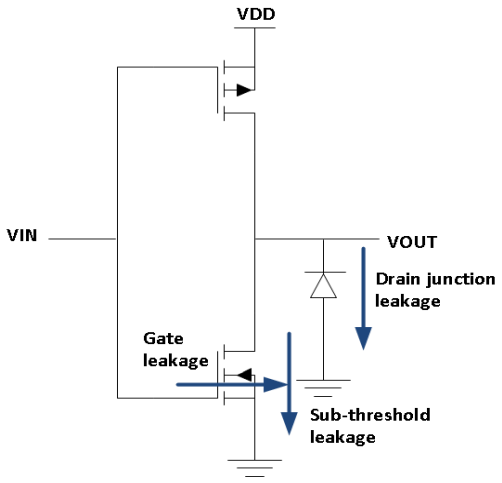


Figure 2.1: Static power of an inverter

2.1.1.1 Reverse-biased PN-junction Leakage

The reverse-biased PN-junction leakage occurs between diffused region and substrate. Figure 2.2 shows the cross section of an inverter. Parasitic diode is formed between source/drain diffusion and N-well. The parasitic diode also formed between N-well and substrate as well as between source/drain diffusion and substrate. Since the diode is reverse-biased, only its leakage current contributes to static power. The reverse-biased PN-junction leakage current is expressed as equation 2.2.

$$I_{leakage} = I_s (e^{qV/kT} - 1) \quad (2.2)$$

Where:

Is = reverse saturation current

V = diode voltage

K = Boltzmann's constant (1.38×10^{-23} J/K)

q = electronic charge (1.602×10^{-19} C)

T = temperature

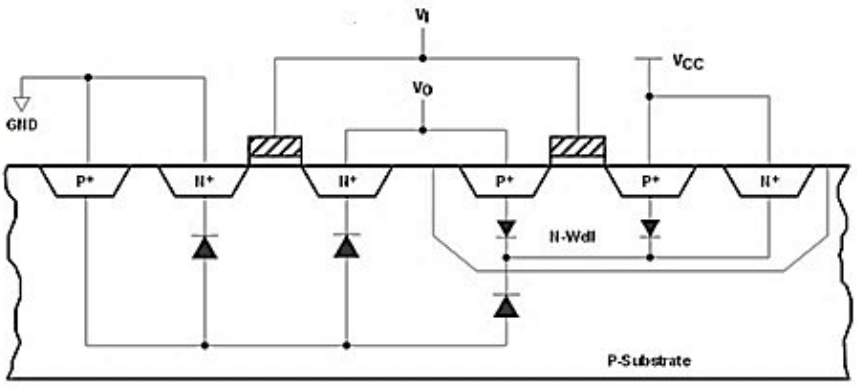


Figure 2.2: Cross section of inverter showing parasitic formation

2.1.1.2 Sub-threshold Leakage

Sub-threshold leakage occurs when transistor operates in sub-threshold region which happen when V_{GS} is below the threshold voltage. In digital circuit, current that flows during sub-threshold region is undesired and considered as weakness. However, the situation is different in analog circuit. The analog circuit is intentionally designed to operate in sub-threshold region in low power design. The advantage of using transistor operates in sub-threshold region is small voltage for biasing. From the equation, it shows that scaling down the threshold voltage increase the sub-threshold leakage current. Amongst all the leakage current sources, sub-threshold leakage contributes the most to the static power consumption (Jalan and Khosla, 2011). The sub-threshold leakage current is represented by the following equation 2.3.

$$I_{SUB} = K\,(W/L)\, e^{(V_{GS}-V_{TH})/nVT)}\,(1-e^{-V_{DS}/VT}) \qquad (2.3)$$

Where:

K = Boltzmann's constant (1.38×10^{-23} J/K)

n = technology parameter

W/L = width / length

V_{TH} = threshold voltage

V_{DS} = drain-source voltage

V_{GS} = gate-source voltage

2.1.1.3 Tunneling Through Gate Oxide

This leakage occurs when the electric field at gate is high enough to allow current tunnel through the gate oxide layer. Figure 2.3 shows the cross section of NMOS with hole/electron tunnelling through gate oxide. In smaller technology such as 60 nm and below, this phenomenon is common since the gate thickness has been reduced.

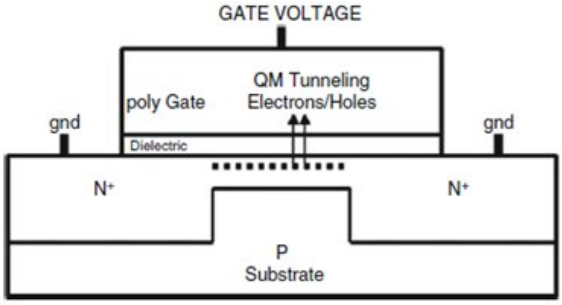


Figure 2.3: Cross section of NMOS showing gate tunnelling

2.1.1.4 Gate Induced Drain Leakage (GIDL)

The gate induced drain leakage is recognized as a major leakage component in OFF state of MOS transistor (Kim et al., 2003). The factors that affect this current are gate oxide thickness, drain concentration, doping gradient and the applied drain to gate voltage, V_{GS}. This leakage occurs when there is high electric field under the gate and drain. The phenomenon mostly occurs when V_G is low and V_D is high. The overlap region between gate and drain is deeply depleted since carriers are generated from surface traps or band-to-band tunneling into the substrate and drain.

2.1.1.5 Punch through

Punch through occurs in channel when drain and source are electrically touch. In other words, the depletion layers at drain and source merge to become a single layer depletion region. The region under the gate becomes independent on the drain –source voltage, V_{DS}. As the V_{DS} increases, the punch through current also increases. This will cause the output capacitance increase hence limit the maximum operating voltage of the device.

2.1.2 Dynamic Power

Dynamic power consists of two components which are dynamic capacitive power and dynamic short-circuit power. Dynamic capacitive power is due to charging and discharging of load capacitor. While dynamic short-circuit power is caused by direct current from V_{DD} to ground when NMOS and PMOS are ON at the same time (Archana et al., 2012).

2.1.2.1 Dynamic Capacitive Power

The dynamic capacitive power occurs during switching of transistors either from ON to OFF state or vice versa. For inverter circuit shown in Figure 2.4, PMOS is ON while NMOS is OFF when input is at logic 0. During this state, the load capacitor is charged through PMOS. Meanwhile when input is at logic 1, PMOS is OFF while NMOS is ON. The energy stored in capacitor is discharged through NMOS. The dynamic power is expressed as in equation 2.4.

$$P_{dynamic} = C_L V^2_{DD} f \quad (2.4)$$

Where:

C_L = load capacitance

V_{DD} = voltage supply

f = operating clock frequency

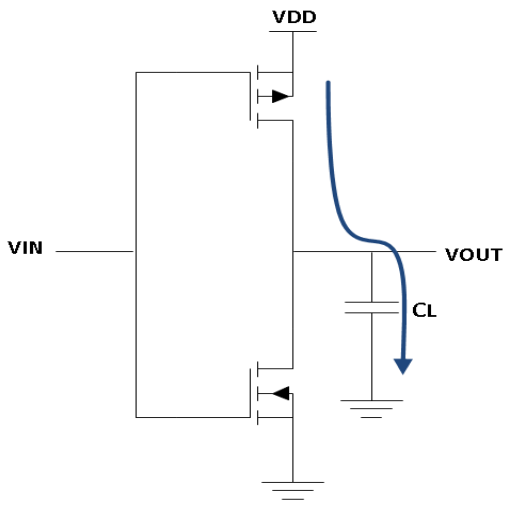


Figure 2.4: Dynamic capacitive power

There are three ways to reduce dynamic power. The first way is lowering the supply voltage. The supply voltage affects the most dynamic power since it has quadratic effect. Hence lowering supply voltage is the most effective method to reduce dynamic power. The second way is reducing capacitance. This can be achieved by using shorter interconnect length. Besides that, the capacitance is reduced when the circuit driving smaller gate load which can be small gate or small fan-out. The third way is reduce the operating clock frequency.

2.1.2.2 Dynamic Short-circuit Power

During switching time, there will be a short period when both of NMOS and PMOS are ON at the same time. When this occurs, there will be a direct current path between V_{DD} and ground as shown in Figure 2.5. This phenomenon consumes power which is called as the dynamic short-circuit power. The dynamic short-circuit power is expressed as equation 2.5.

$$P_{SC} = t_{SC} V_{DD} I_{peak} f \quad (2.5)$$

Where:

t_{SC} = slope of the input signal

V_{DD} = supply voltage

I_{peak} = short-circuit current

f = frequency

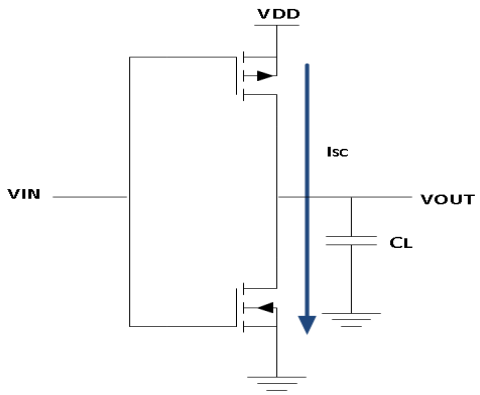


Figure 2.5: Dynamic short-circuit power

2.2 Power Reduction Techniques

The trend in reducing the size of MOSFET device has increases the device density of single integrated circuit. However with the increases of device count, the power consumption also increases (Khateb et al., 2013). Hence techniques to reduce power consumption have to be applied in circuit design so that the circuit functionality is reliable. When the size of the device keeps shrinking, the power supply is reducing. However, the threshold voltage is not reducing by the same ratio since higher threshold voltage means less noise and smaller leakage. In analog design, the most challenge part is the threshold voltage of the MOSFET (Allen et al., 2011). Threshold voltage is the gate-source voltage when channel start to form between the source and the drain that allows current to flow. The conventional analog power reduction techniques such as bulk driven MOSFET and floating gate approach decrease or even remove the threshold voltage (Khateb et al., 2013). Whereas digital power reduction techniques are such as stack forcing and multi-threshold CMOS (Jalan and Khosla, 2011). Besides that, there are body biasing and sleep transistor techniques to reduce dynamic and static power consumption.

2.2.1 Body Biasing Technique

A MOSFET consists of 4 terminals which are drain, source, gate and bulk. Figure 2.6 shows the symbol of n-type MOSFET (NMOS) and p-type MOSFET (PMOS). In typical case, the bulk of NMOS and PMOS are connected to GND and V_{DD} respectively. However, lately the bulk terminal has showing its important role in circuit design as it impacts the threshold voltage. By using body biasing technique, the MOSFET threshold voltage is altered in order to increase the

speed or reduce the leakage (Moradi et al., 2011; Narendra et al. 2001). The body biasing has reduced the leakage up to six times with respect to standard reference supply voltage configuration (Manuzatto et al., 2013).

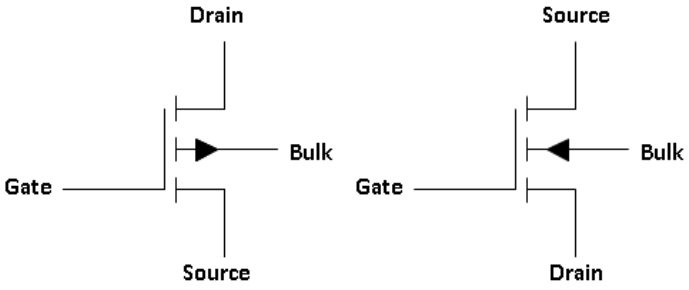


Figure 2.6: NMOS and PMOS symbol

The effect of body biasing on the threshold voltage is given by the equation 2.6.

$$V_T = V_{T0} + (\gamma\sqrt{2|\phi_F| + V_{SB}} - \sqrt{2|\phi_F|}) \tag{2.6}$$

Where:

γ = body effect coefficient

V_{T0} = threshold voltage for zero bias condition

ϕ_F = Fermi potential.

The threshold voltage can be adjusted by changing the voltage at the bulk-source voltage, V_{BS}. Since threshold voltage has impact on leakage current, hence threshold voltage play important

role in power dissipation. The relationship sub-threshold current and threshold voltage is shown in equation 2.7.

$$I_{sub} = I_0 . e^{\frac{V_{GS} - V_{th0} - \lambda V_{BS} + \eta V_{DS}}{n.V_T}} \left(1 - e^{-\frac{V_{DS}}{V_T}} \right) \quad (2.7)$$

Where:

I_0 = drain-source current (I_{DS}) when $V_{GS}=V_{th0}$

V_T = thermal voltage (kT/q)

η = drain-induced barrier lowering (DIBL)

γ = body effect coefficient

n = sub-threshold slope.

The bulk can be biased either in forward biased or reverse biased. The forward body biasing reduces the threshold voltage while the reverse body biasing increases the threshold voltage. The forward body biasing of the substrate is good in term of speed because the delay has reduced. However higher leakage current has introduced (Marin et al., 2004). Moreover, the forward biasing also has a limitation. The amount of forward bias applied must be below the PN diode built-in potential which is about 500 mV (Moradi et al., 2011). This is to prevent the junction diode from turning ON. The reverse body biasing produces smaller leakage current but introducing higher delay.

The early body biasing voltage technique suggests the input signal is driven at bulk terminal while the gate is connected to a fix voltage (Ibrahim, 2013). This technique has proved that the circuit has better amplification. However this technique only improves the trans-conductance while DC biasing of bulk is still needed. Direct application of forward bulk biasing approach has been introduced on an ultra-low ring oscillator. The basic component of ring oscillator is CMOS inverter. The design used two MOSFET transistors which are a NMOS and a PMOS. The bulk of NMOS transistor is connected to the most positive voltage of the circuit while the bulk of PMOS transistor is connected to the most negative voltage. This connection is reversed from the conventional bulk connection. The bulk biasing which is forward biasing approach is applied on Schmitt trigger circuit which is shown in Figure 2.7 (Ibrahim, 2013). The bulk of NMOS and PMOS of the first inverter are connected to the output. The bulk of NMOS and PMOS of the second inverter are connected to V_{DD} and V_{SS} respectively so that the supply voltage is reduced and improve the load driving performance. The second inverter also provides the 180 degree shift to the output of first inverter. The study also proved that the hysteresis is independent on power supply voltage. With V_{DD}=0.3 V, the power dissipated by the Schmitt Trigger circuit is equal to 5.1 nW.

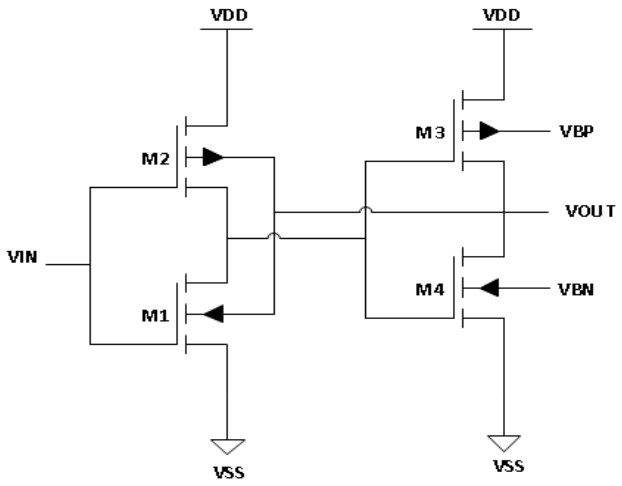


Figure 2.7: Schmitt trigger circuit using body biasing (Ibrahim, 2013)

2.2.2 Multi Threshold CMOS Technique (MTCMOS)

The power can be saved during standby mode if the supply is removed from the power rail when it is not in use state. The multi threshold CMOS (MTCMOS) technique is the example of techniques that can be used to cut off the supply during standby mode. In this technique, sleep transistor is inserted in series between the supply and the existing circuit as well as between the existing circuit and ground. In MTCMOS, high threshold voltage sleep transistors are used. The sleep transistors are turned OFF during standby mode while turn ON during active mode which allowing normal operation. Figure 2.8 illustrates the MTCMOS circuit.

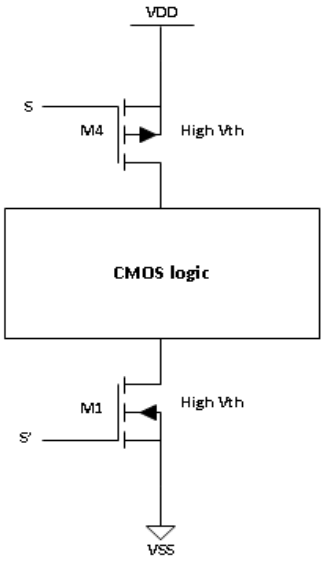


Figure 2.8: MTCMOS structure (Anjana et al., 2013)

2.2.3 Super Cut-off CMOS (SCCMOS)

Another technique to remove supply from power rail when it is not in use is super cut–off CMOS (SCCMOS). This technique is almost similar with the MTCMOS technique. However in SCCMOS, low threshold voltage sleep transistors as shown in Figure 2.9 are used which improve the delay. The delay is improved because of less time is taken for low threshold voltage transistor to ON.

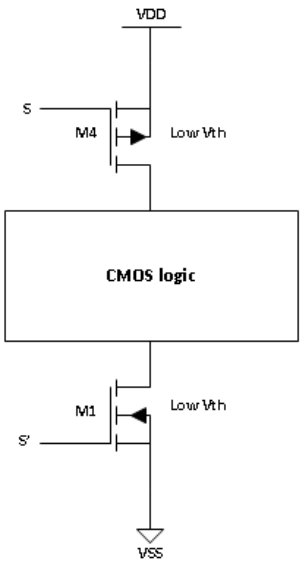


Figure 2.9: SCCMOS structure (Anjana et al., 2013)

2.2.4 Stack Transistor

During active mode, the leakage current can be reduced by dividing and stacking the circuit into two half width of the total transistor size (Anjana et al., 2013). This technique is called transistor stacking. Figure 2.10 shows the schematic of stack inverter. V_{GS} becomes negative because of the positive potential at the intermediate node of the stacked transistor. Thus the leakage current is reduced. The disadvantages of this technique are performance degraded and dynamic power consumption increases (Patel et al., 2014).

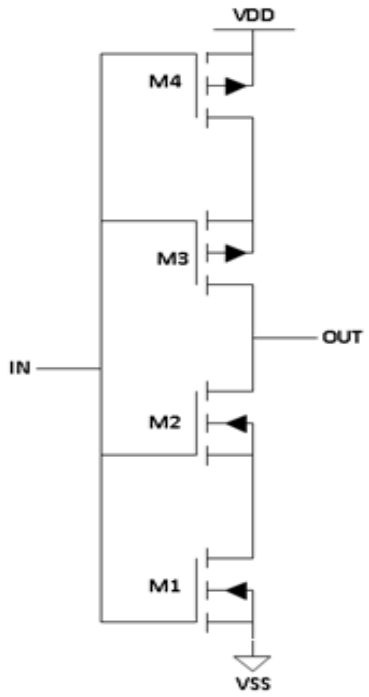


Figure 2.10: Stack transistor (Chowdhury et al., 2012)

2.2.5 Sleepy Stack Technique

Another technique that is simlilar to stack transistor technique is the sleepy stack technique. In this technique, high voltage PMOS threshold sleep transistors and high voltage NMOS threshold sleep transistors are inserted in parallel with one of the pull up and pull down stacked transistor respectively. Figure 2.11 shows the schematic of sleepy stack applied to an inverter. In active mode, the sleep transistors are always ON. Hence it has faster switching time since current always flow. Since the sleep transistor is high threshold voltage, it OFF during standby mode thus reduce the leakage current. This sleep stack technique has improved the switching time compared to stack transistor technique alone. However the area is increased since there were extra transistors used.

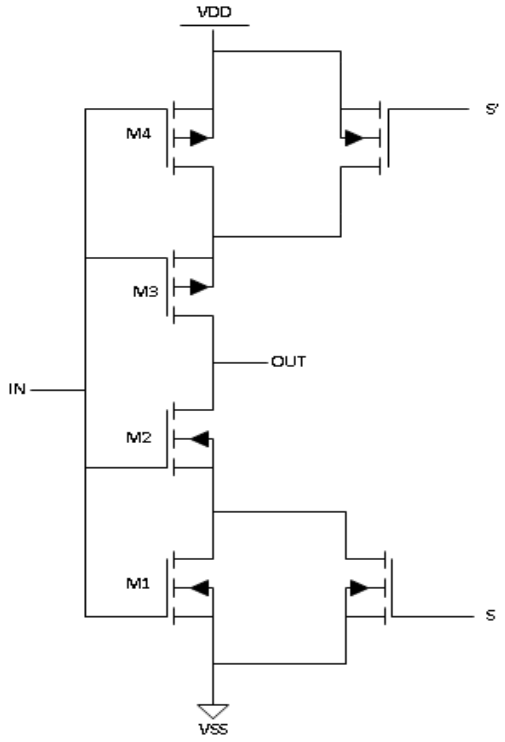


Figure 2.11: Sleepy stack transistor (Chowdhury et al., 2012)

2.3.6 Sleepy Keeper Technique

There is the impoved version of sleepy stack technique which is called the sleepy keeper technique. In sleepy keeper, high voltage NMOS threshold sleep transistors and high voltage PMOS threshold sleep transistors are inserted in parallel with one of the pull up and pull down stacked transistor respectively as shown in Figure 2.12 which is inverse of the sleepy stack approach. During sleep mode, the sleep transistors are in cut off state and the high threshold voltage transistors are the only that connect the supply to ground. The advantage of this technique is it reduces the leakage current as well as maintain the logic state of the circuit.

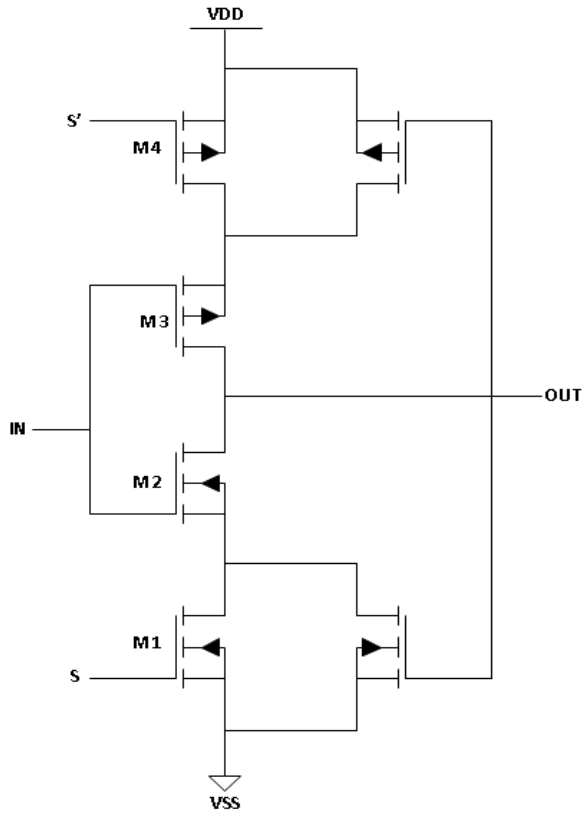


Figure 2.12: Sleepy keeper transistor (Chowdhury et al., 2012)

2.2.7 Combination of Sleepy Stack and Body Biasing Technique

The combination of sleepy keeper circuit and variable body biasing was used to reduce the leakage current (Chowdhury, et al. 2012; Anjana et al., 2013). In this circuit, the original transistor is divided into two halves and the sleep transistors are placed parallel to one of the stacked transistor. The body of the sleep transistor is connected to the source of the PMOS and NMOS transistor in the pull up and pull down network respectively as shown in Figure 2.13. Both of the sleep transistors are OFF during sleep mode. Hence the body to source voltage of the pull up PMOS is higher during sleep mode which increases the threshold voltage. During active

mode, both of the sleep transistors are turned ON which allow current to flow. The threshold voltage of the pull up PMOS is lower which provide faster switching time. The delay of an inverter is reduced as much as 48% (Anjana et al., 2013). The study also shows that even though the delay is improved but there is a need to sacrifice the area.

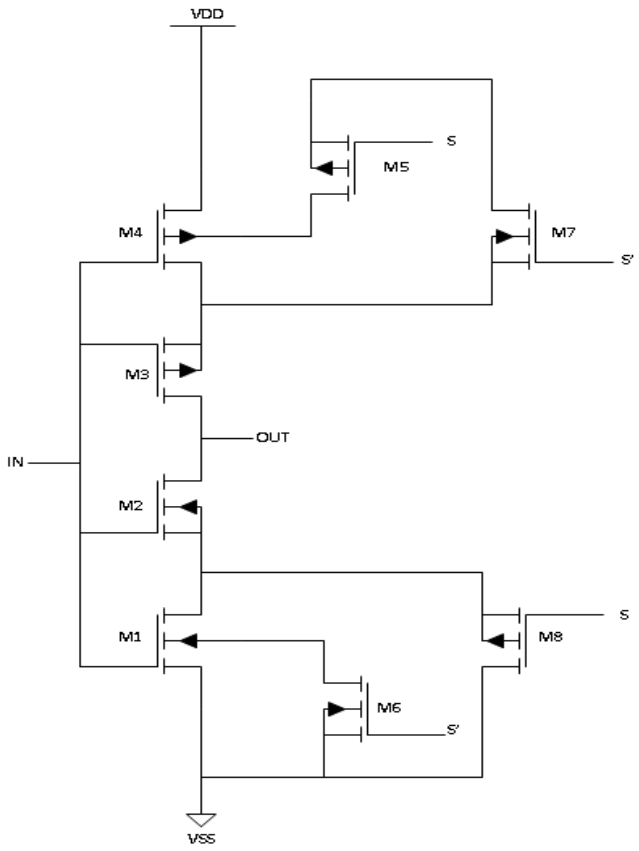


Figure 2.13: Variable body biasing and sleepy stack (Chowdhury, 2012; Anjana et al., 2013)

2.3 COMPARATOR

Comparator is a circuit that compares an analog signal with another analog signal and produces a binary output based on the comparison (Allen and Holberg, 2009). The symbol of comparator is

shown in Figure 2.14 which is similar to the symbol of amplifier. The similarity in many characteristics becomes the reason for comparator and amplifier sharing the same symbol. Even though comparator and amplifier are sharing many same characteristic, these two components cannot substitute each other in high performance design. Comparator is instable under negative feedback whereas the performance of amplifier as comparator cannot be optimized. Comparator is designed to operate in open-loop configuration without any negative feedback. The propagation delay and slew rate of comparator are designed to be maximum and the gain is usually high.

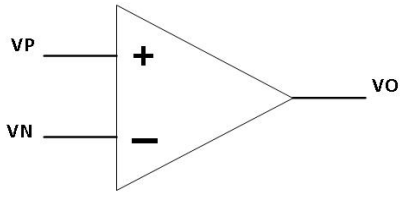


Figure 2.14: Symbol of comparator (Allen and Holberg, 2009)

Comparator can be classified by major parameters such as propagation delay, current consumption, type of output stage, input offset voltage, hysteresis, slew rate, input common mode voltage range and output current capability. Besides major parameters, comparators are classified by other parameters such as input bias current, common mode and power supply rejection ratio, sample/hold function, and start-up time. Figure 2.15 shows the ideal transfer curve of a comparator. V_{OH} is the upper limit while V_{OL} is the lower limit of a comparator. A positive difference between non-inverting and inverting input (V_P-V_N) will produces high or positive output. Whereas, a low or negative output will be produced as the difference is negative.

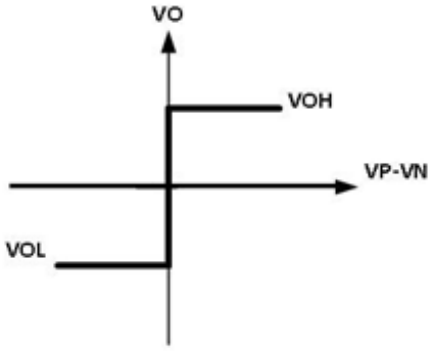


Figure 2.15: Ideal transfer curve of comparator (Allen and Holberg, 2009)

The ideal behaviour of comparator is impossible to achieve in reality. Figure 2.16 shows the transfer curve of a real comparator circuit. V_{IH} and V_{IL} represent the input voltage difference, V_P-V_N at upper and lower limit respectively. This input difference is called the resolution of comparator. In ideal comparator, the output change when the input voltage difference is zero. However due to the manufacturing process such as transistor mismatch, the output changes at non-zero input voltage difference. Offset voltage is shown in transfer curve in Figure 2.17. In this figure, the output does not change until the difference (V_P-V_N) is positive. This difference is called the offset voltage, V_{OS}. The input offset voltage sometimes can be predicted. However the problem occurs when it is unpredicted.

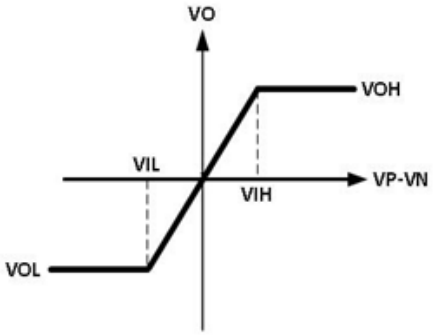


Figure 2.16: Non-ideal transfer curve of comparator (Allen and Holberg, 2009)

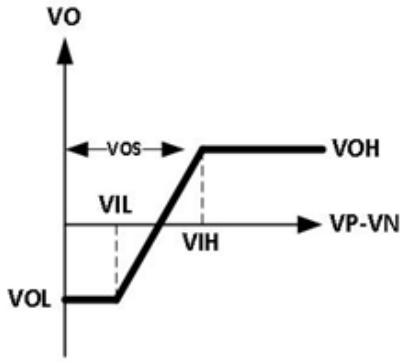


Figure 2.17: Offset voltage (Allen and Holberg, 2009)

One of the parameters in comparator is the propagation delay. It is the time response of the comparator between input excitation and output transition. Figure 2.18 shows the propagation delay time of a non-inverting comparator. The propagation delay is very important in ADCs as it limit the speed of conversion. Propagation delay is small when the input is larger. However there is a limit where any further increase in input will not affect the delay. If the comparator operates under this mode, it is called slew rate. The propagation delay still can be reduced under slew rate mode by increasing the sinking or sourcing capability of the comparator.

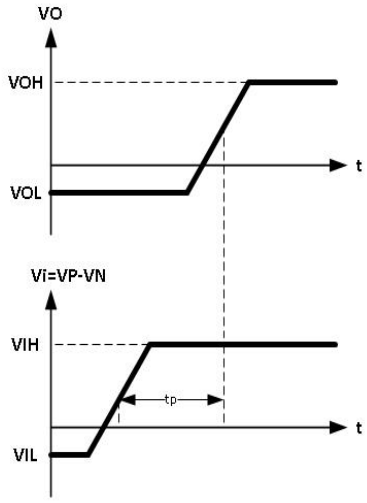


Figure 2.18: Propagation delay (Allen and Holberg, 2009)

2.3.1 COMPARATORS ARCHITECTURES

2.3.1.1 Open-loop Comparator

A comparator requires a differential input and sufficient gain in order to achieve the desired resolution. Hence most of the operational amplifiers are qualified to be implemented as comparator. Since comparator operates in open-loop mode, there is no need for compensation. This will drive the comparator to operate faster as it has wide bandwidth. Two stages amplifier is the basic circuit used in open-loop comparator. The first stage is amplifier and the second stage is current sink/source inverter. Figure 2.19 shows the two stage open-loop comparator circuit. The propagation delay for two stage comparator is due to both transition of the first stage and second stage.

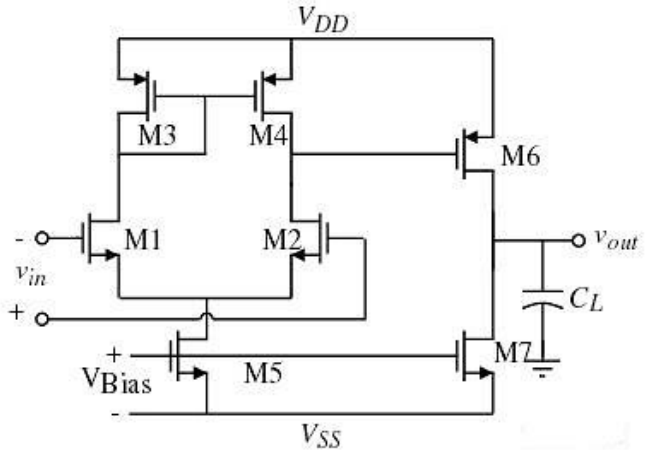


Figure 2.19: Two stage open-loop comparator (Allen and Holberg, 2009)

Besides two stage comparator, there are other open-loop comparators such as comparators with push-pull output comparator, folded-cascode comparator and comparator driving large capacitive

load. The circuit of push-pull comparator is shown in Figure 2.20. The current mirror in the first stage of two stage comparator is replaced by MOS diode. This configuration will reduce the signal amplitude hence reduce the gain. In order to get the same gain as two stage comparator, the output of push-pull comparator has to be cascoded. Even though this type of comparator is slower than two stage comparator, but it able to sink or source large current into output. Moreover, the push pull comparator with cascoded output able to compete the two stage comparator in term of performance in slew rate mode.

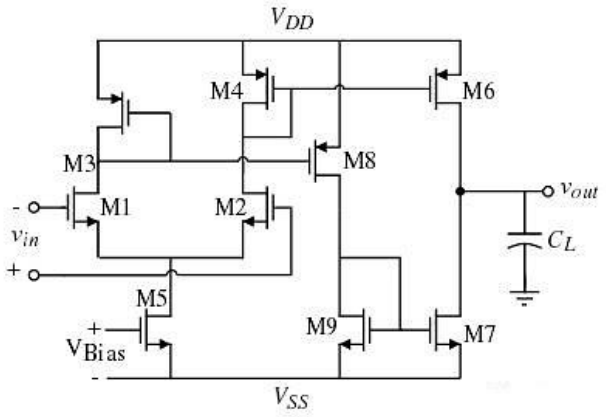


Figure 2.20: Push-pull comparator (Allen and Holberg, 2009)

The folded-cascode comparator is the improved of push-pull comparator in term of common mode voltage range. In folded-cascode comparator circuit, the first stage load is not a MOS diode. Figure 2.21 shows the folded-cascode comparator using cascade current mirror so that the gain equivalent to two stage comparator can be achieved. This method also makes folded-cascode comparator to be self-compensated. Besides common mode voltage range, power supply rejection ratio is improved as well.

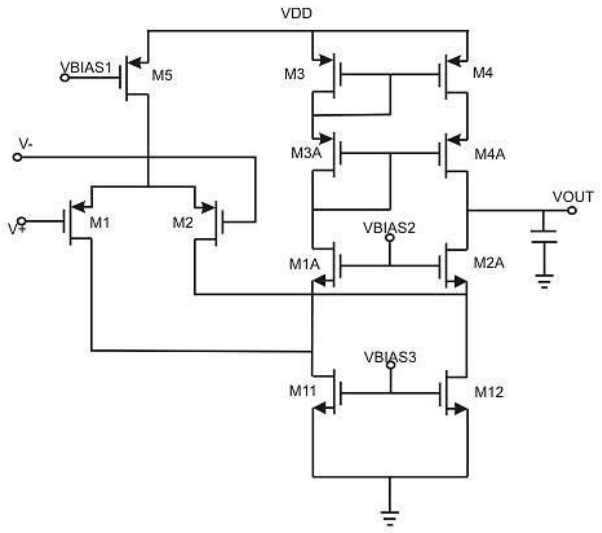


Figure 2.21: Folded-cascode comparator (Allen and Holberg, 2009)

The chance for a comparator with large capacitive load to operate in slew rate mode is limited. This is because only small current will sink/source when large capacitive load connected to the output. One of the methods to increase the capability of a comparator to drive large capacitive load is by adding several push-pull inverters in cascade with the output of two stage comparator. This method will increase the sourcing/sinking current without affecting the speed. The number of push-pull inverter stages can be reduced by increasing the W/L factor. In Figure 2.22, two stages push-pull inverter is used to drive large capacitive load. However there is limitation in increase W/L factor, else the performance will be down-graded. Other method to improve source/sink current is using overdrive techniques such as boosting the tail current and use current mirror as well as use self-biased differential amplifier.

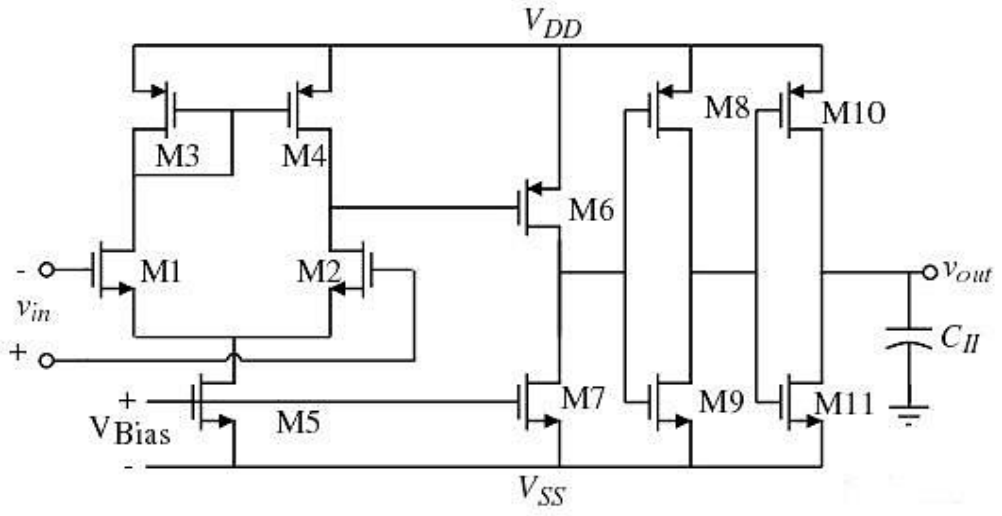


Figure 2.22: Comparator with cascode push-pull inverter (Allen and Holberg, 2009)

2.3.1.2 Open-loop with Regenerative Feedback Comparator

A regenerative comparator compares two signals using positive feedback which called as latch or bi-stable. A latch can be formed as simple as using two cross-coupled MOSFET. Figure 2.23 and Figure 2.24 show the NMOS latch and PMOS latch respectively. The latch has two mode of operations which determined by a two phase clock. The first mode disables the positive feedback. During this mode the input is applied to V_{01} and V_{02} and the initial voltages are applied to V'_{01} and V'_{02}. During second mode, the latch is enabled. The output during this mode will be V'_{01} and V'_{02}. Figure 2.25 shows the clocked comparator using latch. A comparator that contains clock is also known as dynamic comparator.

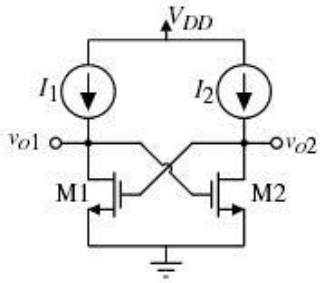


Figure 2.23: NMOS latch

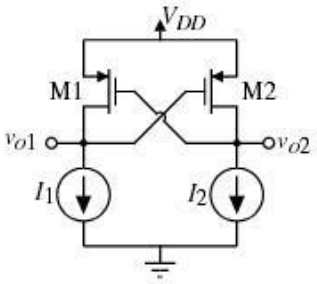


Figure 2.24: PMOS latch

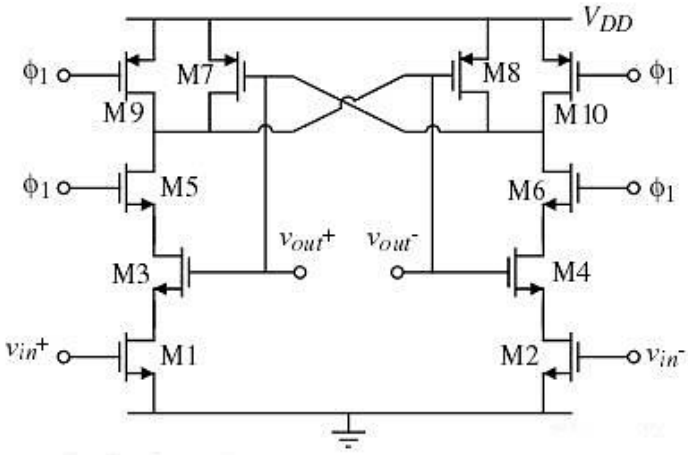


Figure 2.25: Regenerative comparator (Allen and Holberg, 2009)

2.3.1.3 High Speed Comparator

The main requirement for high speed comparator is the propagation delay must be as small as possible for example 50 ps (Gua et al., 2009). It should have high bandwidth and high slew rate as well. There are few stages in most of the high speed comparator circuit as shown in Figure 2.26. The first stage is preamplifier, followed by latch, self-biased differential amplifier and push-pull inverter as second stage, third stage and final stage respectively. The first stage in high speed comparator that is preamplifier is used to amplify input to a sufficient value. The preamplifier also used to reduce the input offset voltage of the second stage which is latch.

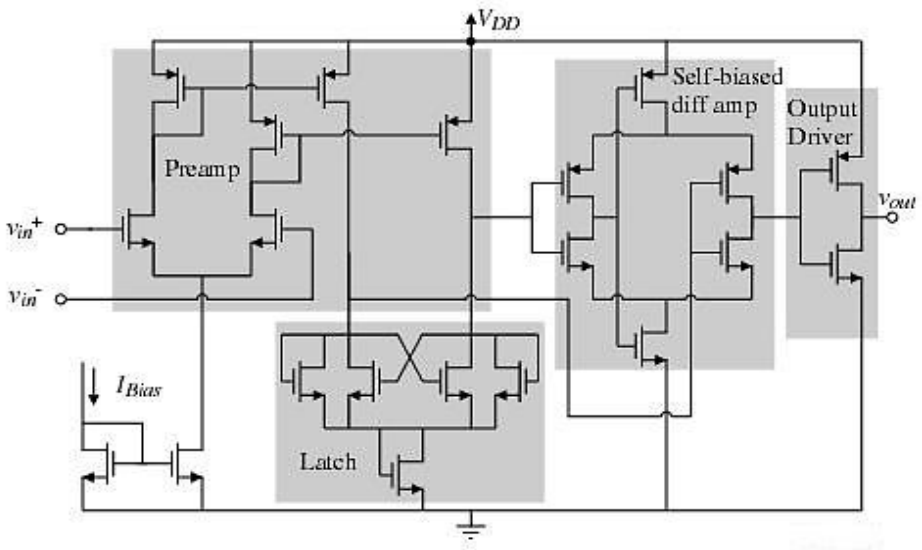


Figure 2.26: High speed comparator (Allen and Holberg, 2009)

2.4 Summary

In this chapter, static power and dynamic power that contribute to the overall power consumption have been reviewed. Then, power reduction techniques which are body biasing technique, multi-threshold CMOS, super cut-off CMOS, stack transistor and sleep transistor have been review. Super cut-off CMOS technique is the best way to reduce static power because the power rail is totally cut during sleep mode. Meanwhile body biasing technique is the best method to reduce dynamic power. The threshold voltage is adjustable using this technique. Lastly, the characteristics and the type of comparator architectures have been reviewed.

CHAPTER 3

METHODOLOGY

This chapter describes the methodology of this study. Besides that, this chapter also presents and discusses the circuit design of comparator used in this study. First, this chapter presents the circuit of conventional comparator. This chapter also presents and discusses the circuit of proposed comparator which using body biasing, sleepy stack and SCCMOS techniques are. Besides circuit design, this chapter also discusses about layout design of proposed comparator.

3.1 Research Methodology

The aim of this work is to study power reductions techniques for comparator. In order to achieve the purpose of this work, the following several steps have been done. Each of the steps is discussed below:

I. Literature Review

The work has been started with literature review which discussed in Chapter 2. Since this study is all about reducing power consumption, the first part that has been reviewed is the components in power consumption which generally can be classified as dynamic power and static power. The

second part of the literature that has been reviewed is the available power consumption techniques. Last but not least, the characteristics and architecture of comparator was reviewed.

II. Circuit Design and Pre-layout Simulation

All circuit were implemented in Cadence ™ tools CAD Virtuoso Schematic Editor using Silterra 0.13 µm CMOS technology. Firstly in circuit design, a fully function conventional comparator was designed. In this study, two stages comparator has been used. Then, the fully function conventional comparator circuit is modified and enhanced with power reduction techniques. For static power reduction, sleepy transistor and super cut-off CMOS technique have been used. Meanwhile body biasing has been used to reduce dynamic power by reducing V_{TH} which then allowing reduction of supply voltage. Two types of pre-layout simulation which are DC response and transient response were done in Analog Design Environment using SPECTRE simulator. All input signal used in this study is fixed at 10 MHz so that the effect of frequency on dynamic power for all comparator designs can be factored out. From the simulation, power consumption and propagation delay are measured.

III. Layout Design and Post-layout Simulation

In this study, only layout for the proposed comparator has been done. The layout was designed using Cadence tools CAD Virtuoso Layout Editor using Silterra 0.13 µm CMOS technology. The DRC, LVS and PEX were run using CALIBRE from Mentor Graphic. Just like in pre-layout simulation, DC response and transient response has been simulated in order to measure the

power consumption and propagation delay. The results from post-layout simulation have been used to compare with the result from pre-layout simulation.

IV. Conclusion and Recommendation

The finding of this study has been concluded in the last part of this study as well as the recommendation for future work.

The methodology of this study is summarized in the flow chart in Figure 3.1.

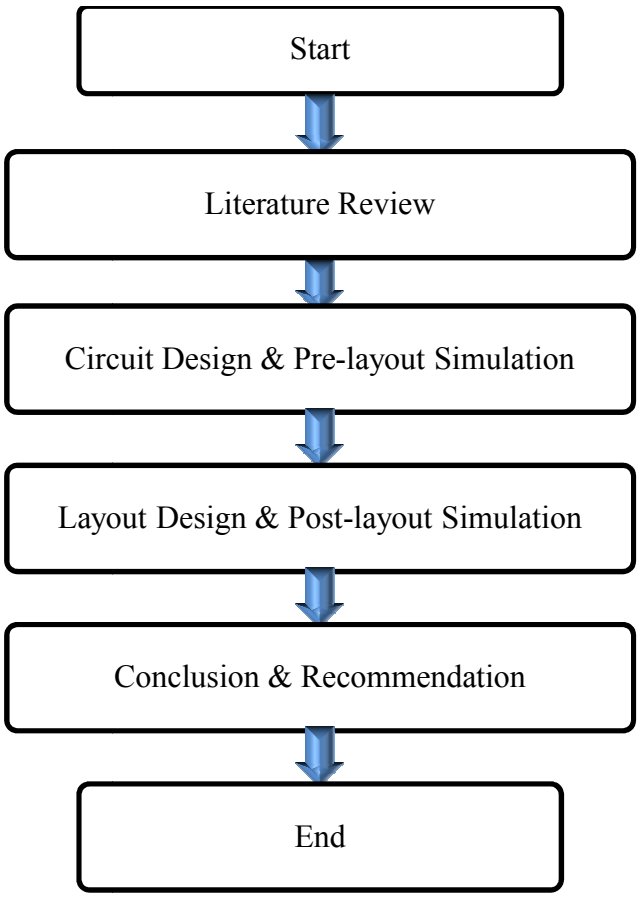


Figure 3.1: Methodology flow chart

3.2 Circuit Design

Figure 3.2 shows the schematic of conventional comparator (Chu & Current, 1997) used in this study. The circuit is divided into two stages. The first stage is NMOS input differential pair (M6 and M7) driven by the tail current transistor (M8). The bias at the gate of transistor M8 is 0.7 V. The input voltage is applied at the gate of M6 while reference voltage is applied at the gate of M7. In this study, the input voltage for this conventional comparator is in the range between 0 V to 1.2 V and the voltage reference is 0.6 V. Transistor M0 and M3 are diode load to the differential pair because the drain and gate of the transistors are tied together. In this stage there is also a positive feedback loop which is the cross coupled PMOS transistors (M1 and M2). The second stage of the comparator is a push pull CMOS inverter (M11 and M12). The inverter provides a full voltage swing to the output. Push pull inverter also produces higher gain since the both of the transistor M11 and M12 are driven by the same voltage input.

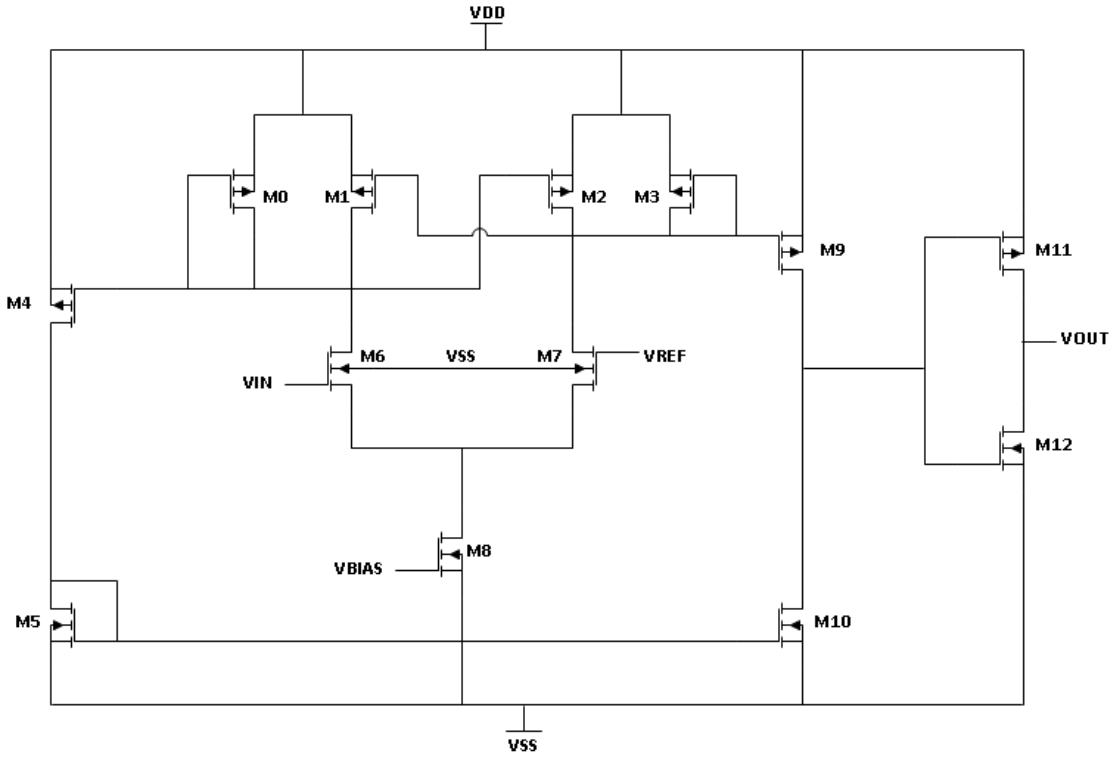


Figure 3.2: Schematic of conventional comparator (Chu & Current, 1997)

The general size of NMOS and PMOS transistor are determined by simulating DC analysis for inverter. The transistor size is optimized when the resistance of NMOS and PMOS transistor are equal. In this work, the length of both NMOS and PMOS transistor are fixed at 0.13 µm and the width of NMOS transistor is fixed at 2 µm. Parametric analysis was used to simulate different value of width for PMOS transistor. Figure 3.3 shows the voltage transfer characteristic curve of the parametric analysis. It shows that the resistance of NMOS and PMOS transistors are equal when X=Y=0.6 V which happen to be when width of PMOS transistor is 4 µm. Table 3.1 shows of length and width of all transistors used in conventional comparator circuit.

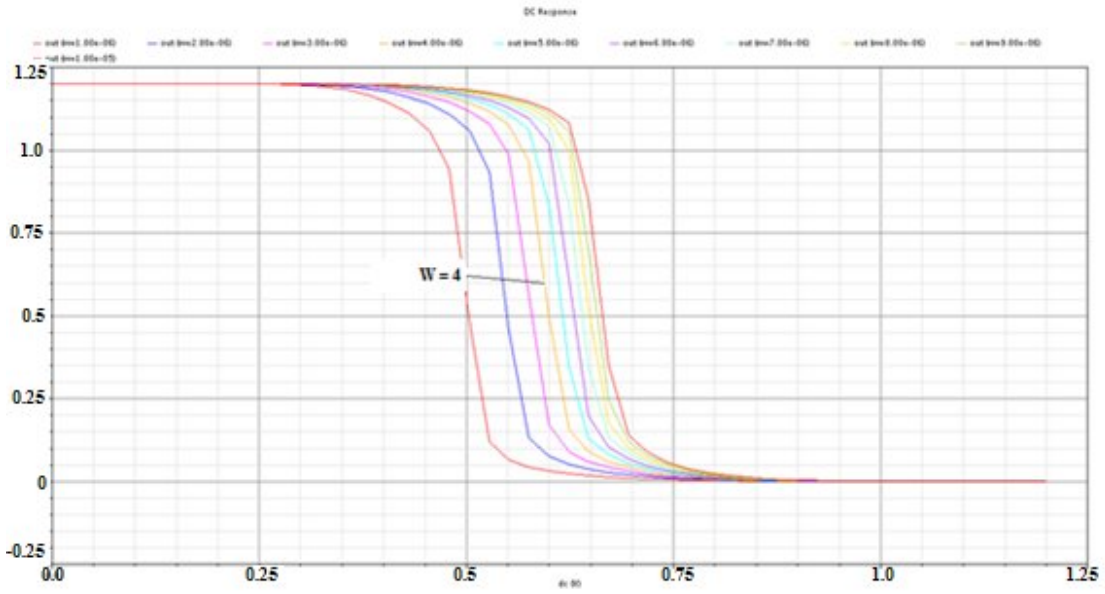


Figure 3.3: Voltage transfer characteristic curve

Table 3.1: Transistor width and length of conventional comparator

Transistor	Width	Length
M0	4u	0.13u
M1	4u	0.13u
M2	4u	0.13u
M3	4u	0.13u
M4	4u	0.13u
M5	2u	0.13u
M6	2u	0.13u
M7	2u	0.13u
M8	4u	0.13u
M9	4u	0.13u
M10	2u	0.13u
M11	4u	0.13u
M12	2u	0.13u

One of the effective ways to reduce power consumption especially dynamic power is by reducing power supply voltage (Yasufuku et al., 2012). However reducing supply voltage may degrade the performance of the circuit such as reduce speed and operating frequency. Moreover, reducing supply voltage may cause the circuit to malfunction. The conventional comparator circuit in Figure 3.2 was used to study the effect of reducing supply voltage on delay and operating frequency. Table 3.2 summaries the result when different voltages are supplied to the circuit. The table shows that delay increases and operating frequency decreases as the supply voltage keeps decreasing. For supply voltage below 0.4 V, the circuit starts to malfunction. This is because of the supply voltage is below the threshold voltage of NMOS and PMOS which is 328 mV and 392 mV respectively.

Table 3.2: Delay and frequency for supply voltage

Supply Voltage	**Delay (ns)**	**Frequency (MHz)**
0.4	235.4	2
0.5	67.6	10
0.6	21.52	10
0.7	8.11	10
0.8	3.96	10
0.9	2.44	10
1.0	1.76	10
1.1	1.38	10
1.2	1.04	10

The supply voltage can be decreased more by applying forward body biasing to the bulk to decrease the threshold voltage. In this work, the body biasing has been studied by simulating DC

analysis and observing the threshold voltage of the NMOS and PMOS transistor at different body biasing. Table 3.3 shows the threshold voltage for NMOS and PMOS transistor when different body biasing is applied at the bulk. From the graph in Figure 3.4, it shows that the threshold voltage of PMOS decrease when body biasing increase. In conventional PMOS bulk connection which is V_{DD}, the threshold voltage is about 393 mV. However the threshold voltage decreases to 121 mV when the bulk is connected to 0 V. On the other hand, the threshold voltage of NMOS is decrease when body biasing decrease. The threshold voltage of NMOS is about 328 mV in conventional NMOS bulk connection. By connecting the bulk to V_{DD}, the threshold voltage decrease to 87 mV.

Table 3.3: NMOS and PMOS threshold voltage for different body biasing

Body Biasing	**PMOS Vth (mV)**	**NMOS Vth (mV)**
0.0	-121.076	328.252
0.1	-121.546	309.861
0.2	-122.266	289.646
0.3	-123.512	267.167
0.4	-130.268	241.786
0.5	-171.044	212.526
0.6	-221.381	175.319
0.7	-261.364	130.585
0.8	-294.563	94.887
0.9	-323.241	89.211
1.0	-348.662	88.193
1.1	-371.603	87.587
1.2	-392.575	87.176

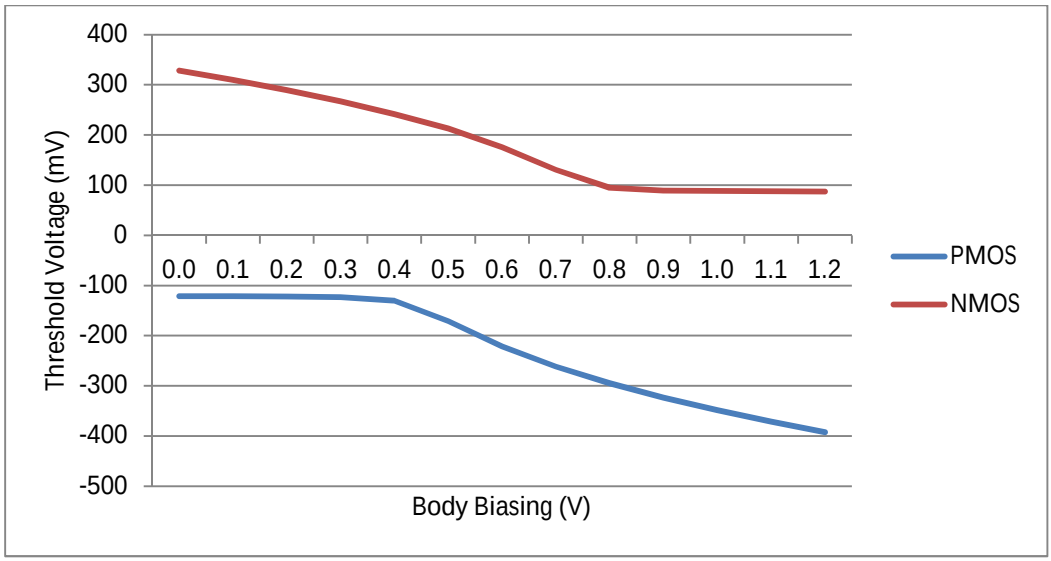


Figure 3.4: Threshold voltage of PMOS and NMOS versus body biasing

The forward body biasing cannot exceed 0.5 V which is the PN diode built-in potential (Moradi et al., 2011). The conventional comparator circuit in Figure 3.2 was once again simulated with random PMOS and NMOS body biasing in range of 0.1 V to 0.5 V. The supply voltage used for this simulation is 0.5 V. The effect on propagation delay and dynamic power consumption were observed and recorded in bar chart in Figure 3.5. It shows that the propagation delay is the smallest but dynamic power is the highest when NMOS body biasing and PMOS body biasing equal to 0.3 V and 0.1 V respectively. The dynamic power is the lowest for NMOS body biasing and PMOS body biasing equal to 0.2 V and 0.3 V respectively. For this NMOS and PMOS body biasing, the effect of supply voltage on propagation delay and and dynamic power consumption was investigated. Figure 3.6 is the log-log graph of V_{DD} versus propagation delay and dynamic power. The graph shows that the propagation delay decrease with increasing of $V_{DD.}$ Meanwhile the graph show that dynamic power increase when V_{DD} increase. The graph intersect at V_{DD} = 0.5 V. This V_{DD} value is the most optimize supply voltage because of the win win situation for both dynamic power and propagation delay. Hence V_{DD} equal to 0.5 V,

NMOS body biasing equal to 0.2 V and PMOS body biasing equal to 0.3 V were used in the proposed comparator.

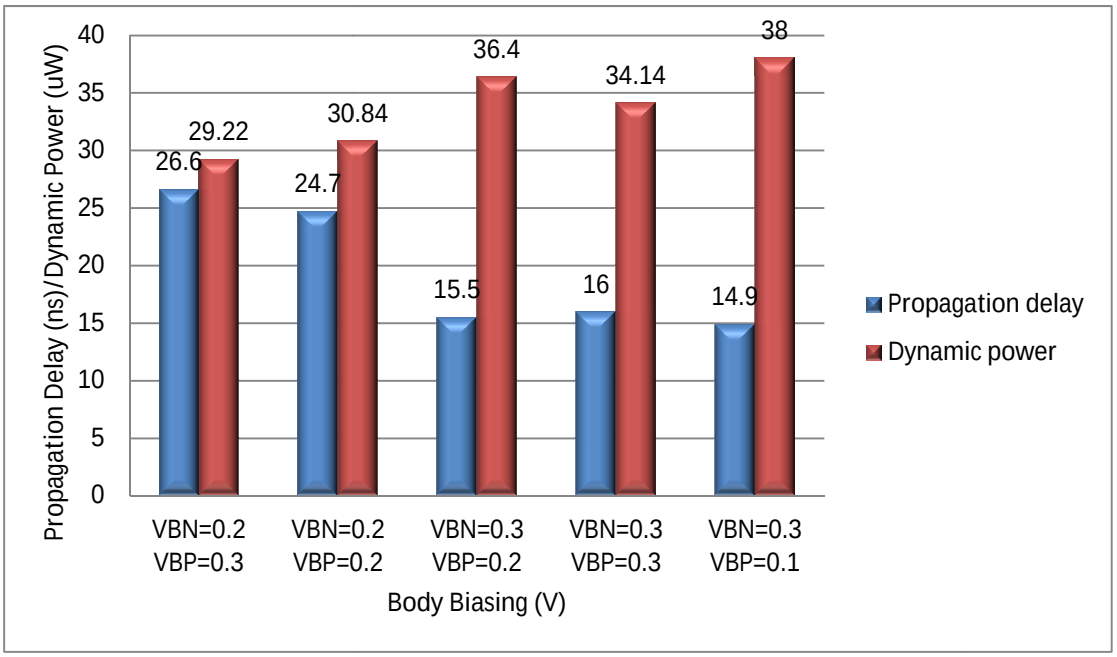


Figure 3.5: Effect of body biasing on propagation delay and dynamic power consumption

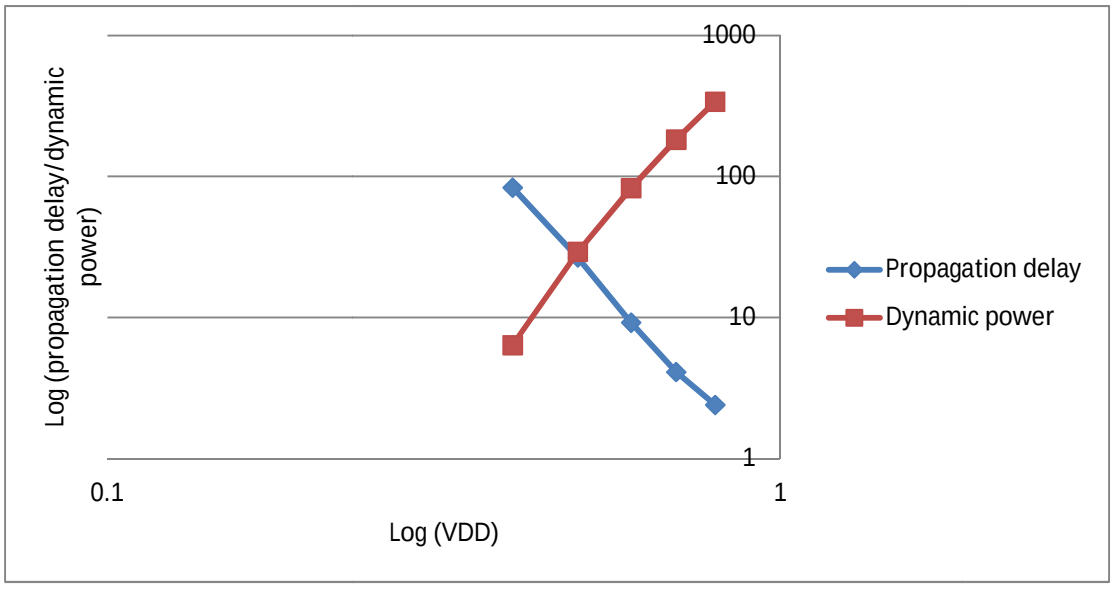


Figure 3.6: Effect of V_{DD} on propagation delay and dynamic power consumption

The forward body biasing at the bulk in the previous part is basically used to reduce dynamic power consumption. The next part is going to focus on reducing static power consumption. Eventhough the static power is not critical for 0.13 μm CMOS technology, but it is still a part of total power consumption. Hence reducing static power consumption will also help in reducing the total power consumption.

Figure 3.7 shows the circuit of comparator with super cut-off CMOS (SCCMOS) and sleepy stack approach. In this circuit, there are six extra transistors compared to the conventional comparator. The size of existing M11 and M14 transistors are divided into half as in stack approach. Then sleep transistors M15 and M16 are added parallel to transistor M11 and M14. For SCCMOS technique, transistor M17 and M18 are added. The circuit operates in two modes which are active mode and sleep mode. During active mode, transistor M11, M14, M17 and M18 are ON. Thus there will be current flow through the circuit. Meanwhile transistor M11, M14, M17 and M18 are OFF during sleep mode. Current is not flowing through the circuit during this mode. Figure 3.8 shows the static power for conventional comparator and comparator with SCCMOS and sleepy stack. The conventional comparator only operated in a single mode. The static power is reduced when SCCMOS and sleepy stack techniques are added in the comparator circuit. Moreover, the static power consumption during sleep mode is much lower than the the static power during active mode.

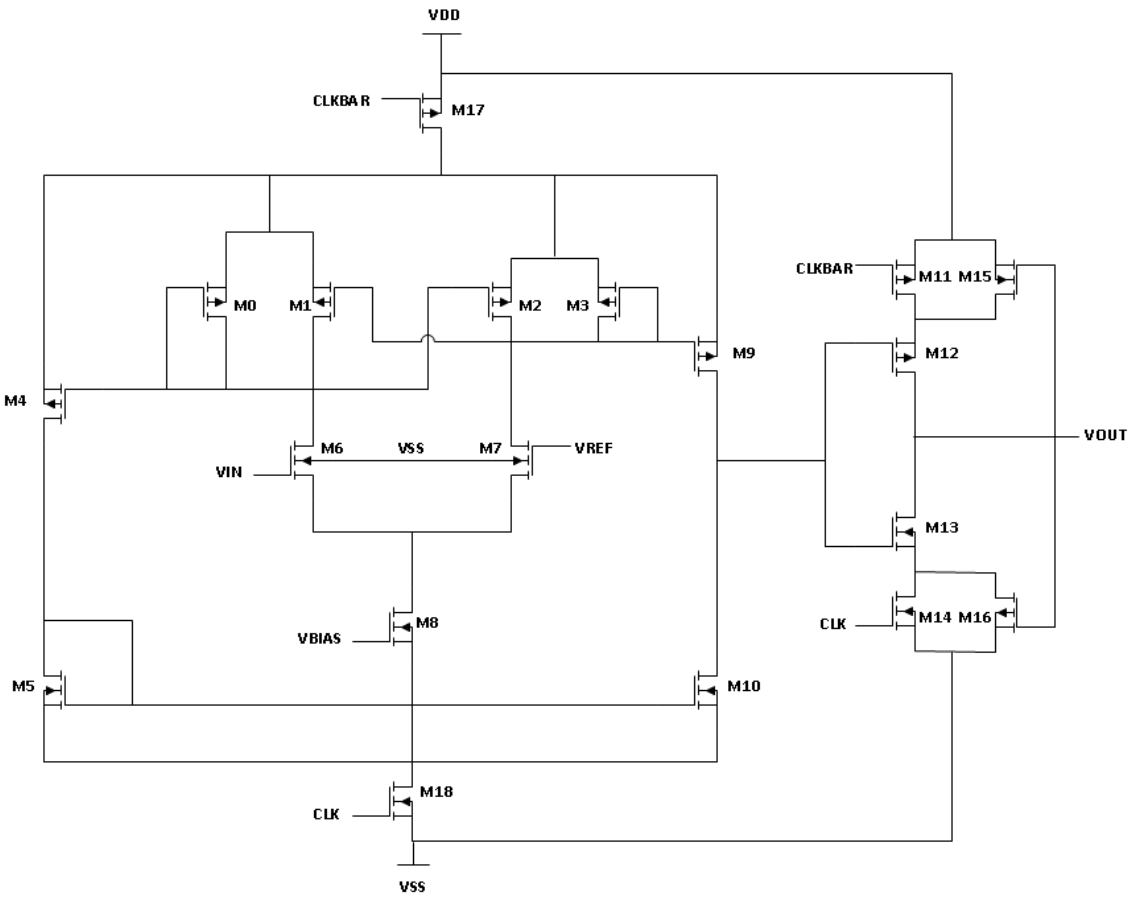


Figure 3.7: Schematic of comparator with SCCMOS and sleepy stack

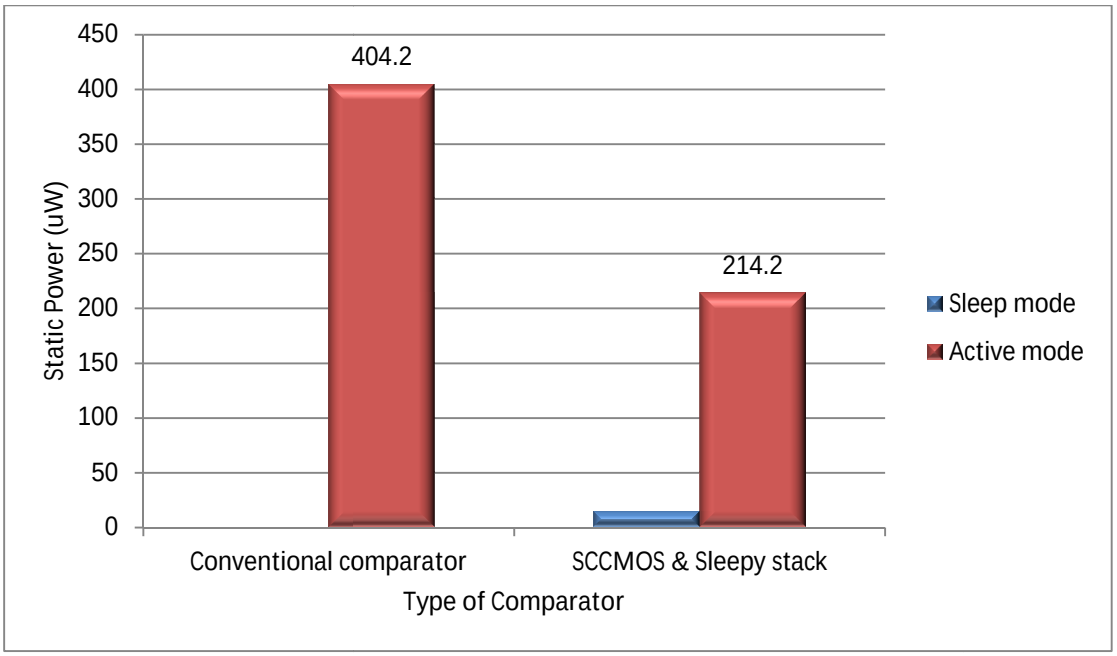


Figure 3.8: Static power for different type of comparator

Figure 3.9 shows the proposed comparator circuit. The circuit consists of forward body biasing, super cut-off CMOS (SCCMOS) and sleepy stack technique. The body biasing technique is for reducing threshold voltage. Hence reduce the supply voltage for dynamic power reduction. Super cut-off CMOS (SCCMOS) and sleepy stack technique are for static power reduction. Table 3.4 shows the transistor sizing for proposed comparator.

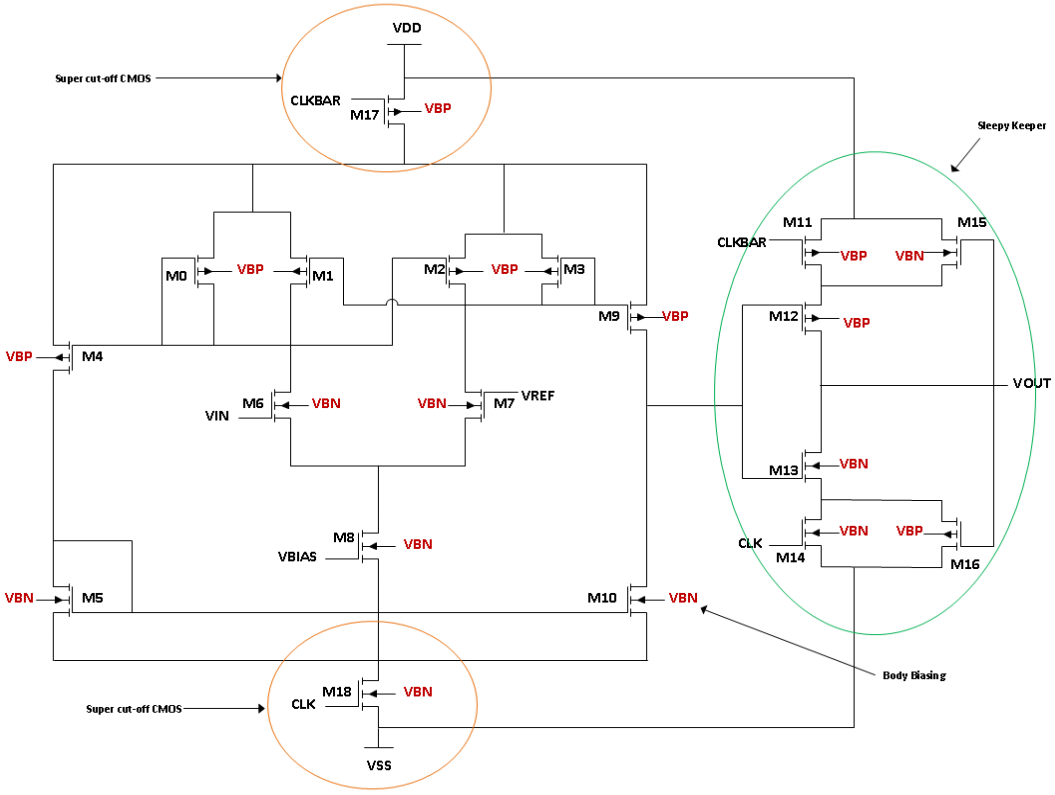


Figure 3.9: Schematic of proposed comparator

Table 3.4: Transistor width and length of proposed comparator

Transistor	Width/Length	Transistor	Width/Length
M0	4µm/0.13µm	M10	2µm/0.13µm
M1	4µm/0.13µm	M11	2µm/0.13µm
M2	4µm/0.13µm	M12	2µm/0.13µm
M3	4µm/0.13µm	M13	1µm/0.13µm
M4	4µm/0.13µm	M14	1µm/0.13µm
M5	2µm/0.13µm	M15	2µm/0.13µm
M6	2µm/0.13µm	M16	1µm/0.13µm
M7	2µm/0.13µm	M17	4µm/0.13µm
M8	4µm/0.13µm	M18	2µm/0.13µm
M9	4µm/0.13µm		

3.3 Layout Design

Figure 3.10 shows the layout of the proposed comparator. The area is not constraint in this study. Hence, the layout has been purposely drawn so that the fisrt stage and second stage of proposed comparator can be easily seen. The overall size of the proposed comparator layout is 26 µm × 18 µm. The layout which consists of 19 transistors has been designed using only two metals which are metal 1 and metal 2. The fingering technique was used in this design in order to standardize the width. In layout design, there are three stages that need to go through. The first stage is design rule check (DRC) followed by layout versus schematic (LVS) check and lastly PEX RC extraction for post-layout simulation. As shown in Figure 3.11, the layout has passed the design rule check (DRC) and the LVS also clean as showned in Figure 3.12.

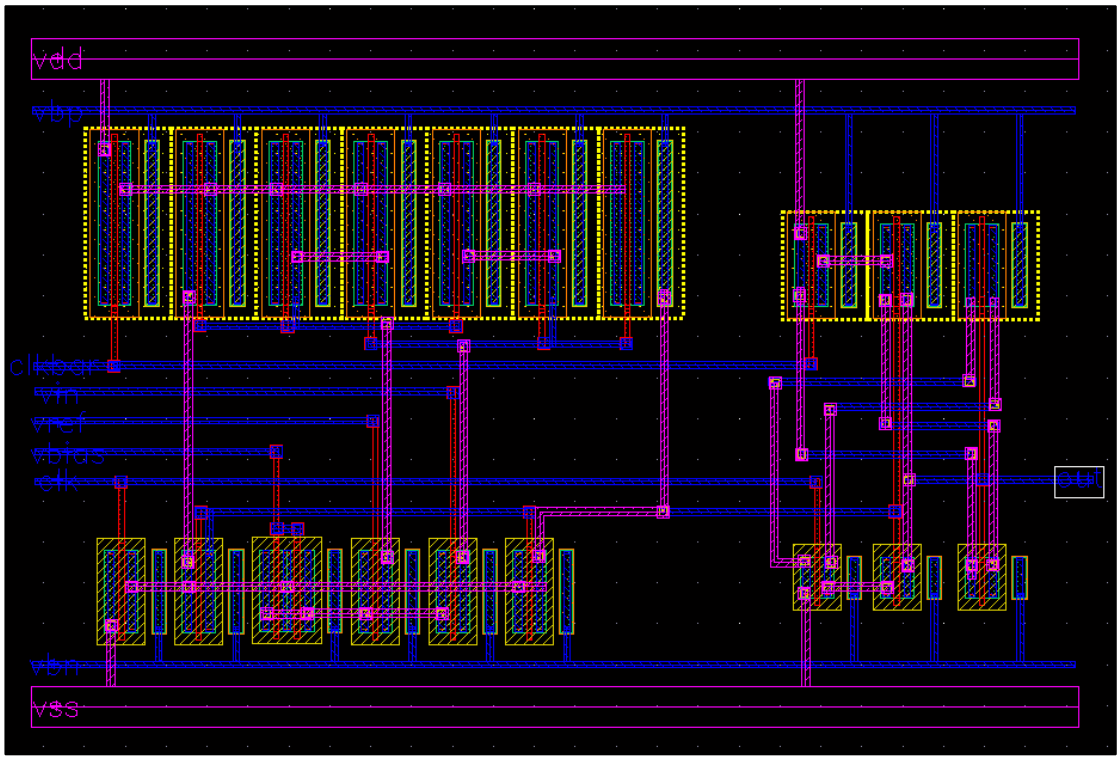


Figure 3.10: Layout of proposed comparator

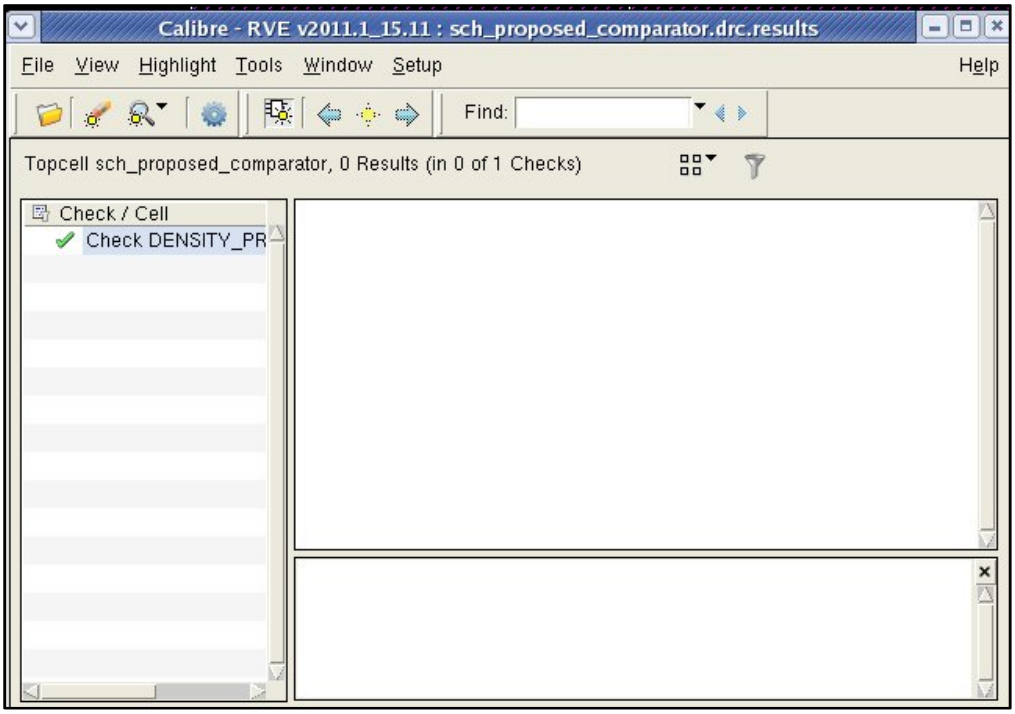


Figure 3.11: DRC report

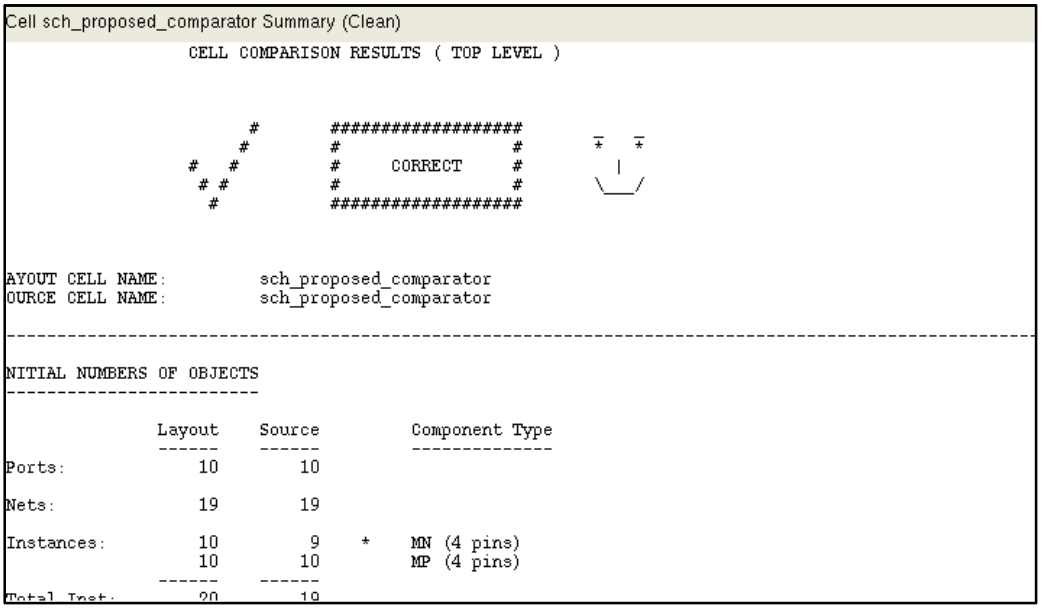


Figure 3.12: LVS report

3.4 Summary

The methodology of this study has been discussed in this chapter. There are four stages that have been through in order to complete this study. This study has started with literature review followed by circuit design, layout design and lastly the conclusion and recommendation. In this chapter also, the schematic of circuits as well as the operation of these circuits have been presented and discussed. Lastly, the layout of proposed comparator is presented and explained.

CHAPTER 4

RESULTS AND DISCUSSIONS

This chapter presents the result from pre-layout simulation as well as discussion of the result. This chapter also presents the characteristics and performances of each comparator. Then this chapter presents the post-simulation result of proposed comparator. Lastly, this chapter compares the result from pre-layout and post layout simulation of proposed comparator

4.1 Pre-layout Simulation

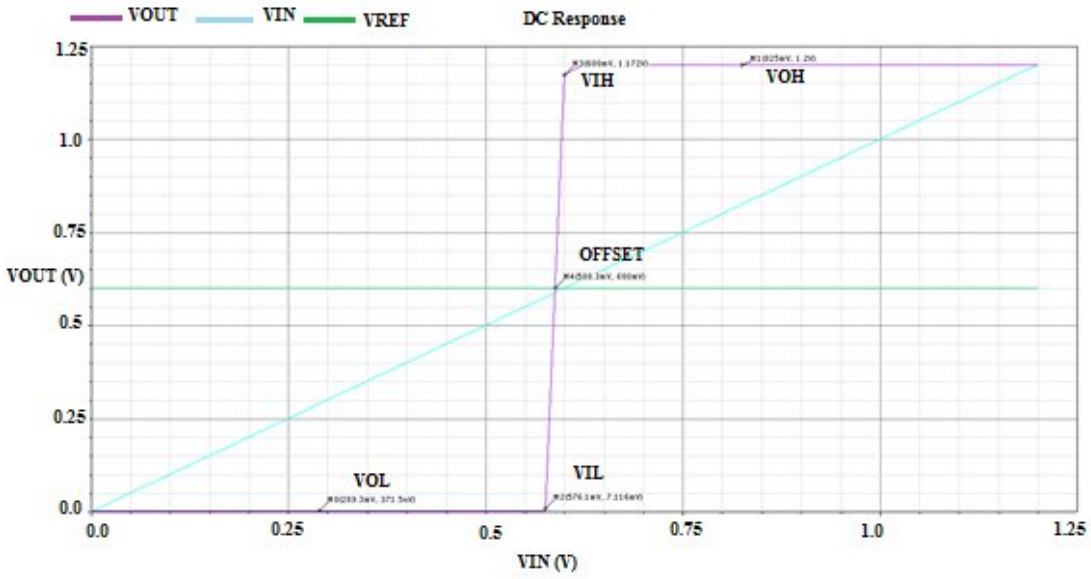
4.1.1 Static Characteristic

All the simulations were run in Virtuoso Analog Design Environment using Spectre Simulator. All input signals used for simulation in this study is 10 MHz. DC analysis was run to measure the static characteristics of comparator. During DC analysis, the input voltage was sweep. The output waveform represents the transfer curve of the comparator. From the transfer curve, the upper input (V_{IH}), lower input (V_{IL}), upper output (V_{OH}) and lower output (V_{OL}) were measured. These measurements were used to calculate the gain of the comparator which using equation 4.1 (Allen and Holberg, 2011). The resolution of comparator which is the difference of upper input

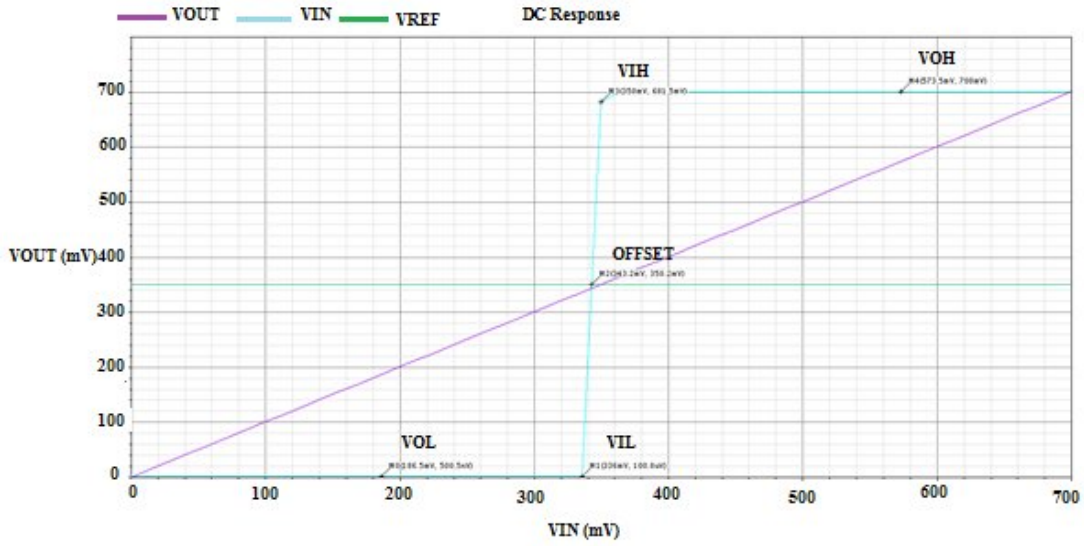
(V_{IH}) and lower input (V_{IL}) also calculated. Besides that, the transfer curve also showed the offset voltage of the comparator.

$$Av = \frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}} \tag{4.1}$$

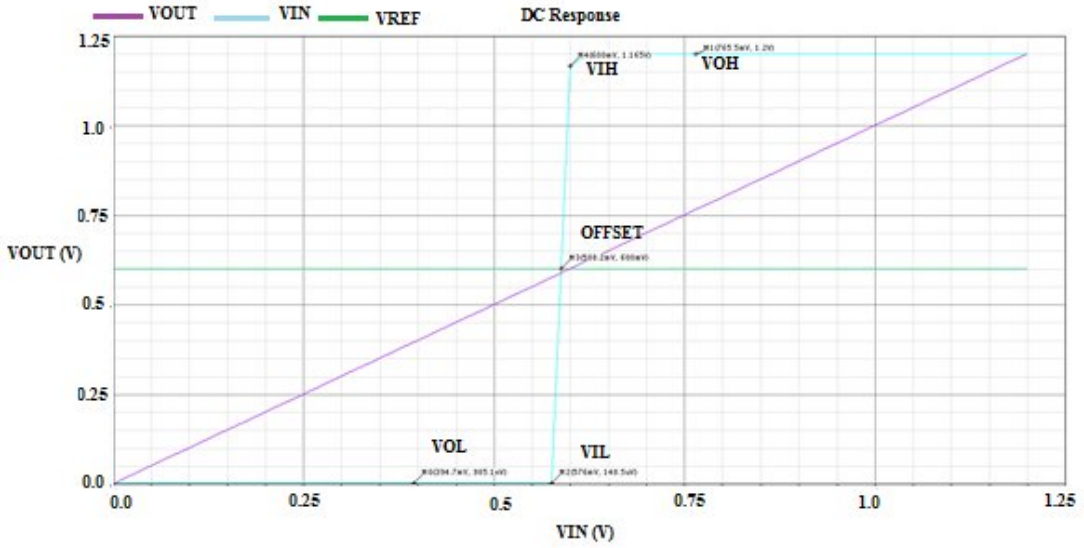
Figure 4.1 shows the transfer curve of conventional comparator, reduced V_{DD} conventional comparator, comparator with sleepy stack and SCCMOS as well as proposed comparator. The waveform shows the output signal, V_{OUT} is low when the input signal, V_{IN} is below reference voltage, $V_{REF.}$ Meanwhile the output signal, V_{OUT} goes high when input signal, V_{IN} is greater than the reference voltage, $V_{REF.}$ Table 4.1 shows the upper input (V_{IH}), lower input (V_{IL}), upper output (V_{OH}) and lower output (V_{OL}) which measured from transfer curve. These results were used to calculate the offset, resolution and voltage gain of comparator.



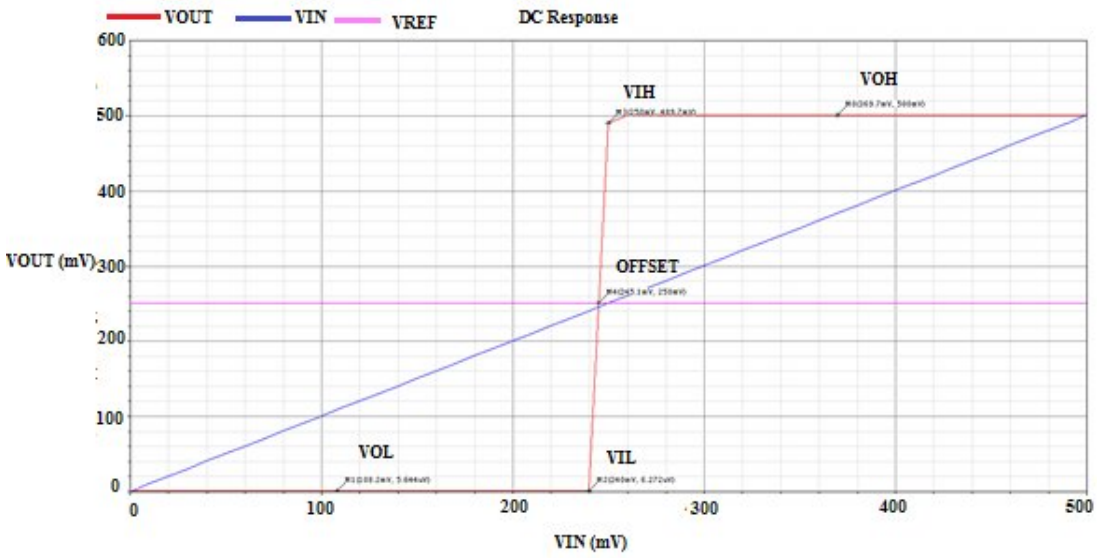
(a)


VOUT
VIN
VREF
DC Response
VIH
VOH
OFFSET
VOL
VIL
VOUT (mV)
VIN (mV)
0
100
200
300
400
500
600
700

(b)


VOUT
VIN
VREF
DC Response
VIH
VOH
OFFSET
VOL
VIL
VOUT (V)
VIN (V)
0.0
0.25
0.5
0.75
1.0
1.25

(c)



(d)

Fig 4.1: Transfer curve of (a) Conventional comparator, (b) Reduced V_{DD} comparator, (c) Comparator with SCCMOS and sleepy stack and (d) Proposed comparator

Table 4.1: Static Characteristics of (a) Conventional comparator, (b) Reduced V_{DD} conventional Comparator, (c) Comparator with sleepy stack and SCCMOS and (d) Proposed comparator

Characteristics	**(a)**	**(b)**	**(c)**	**(d)**
Output high voltage, V_{OH}	1.2 V	0.7 V	1.2 V	500.0 mV
Output low voltage, V_{OL}	371.5nV	500.5nV	985.1n V	0.0 V
Input high voltage, V_{IH}	600.0 mV	350.0 mV	600.0 mV	250.0 mV
Input low voltage, V_{IL}	576.1 mV	336.0 mV	576.0 mV	240.0 mV

Figure 4.2 show that the proposed comparator has the smallest offset followed by the reduced V_{DD} comparator. Meanwhile conventional comparator and comparator with SCCMOS and sleepy stack have the highest offset.

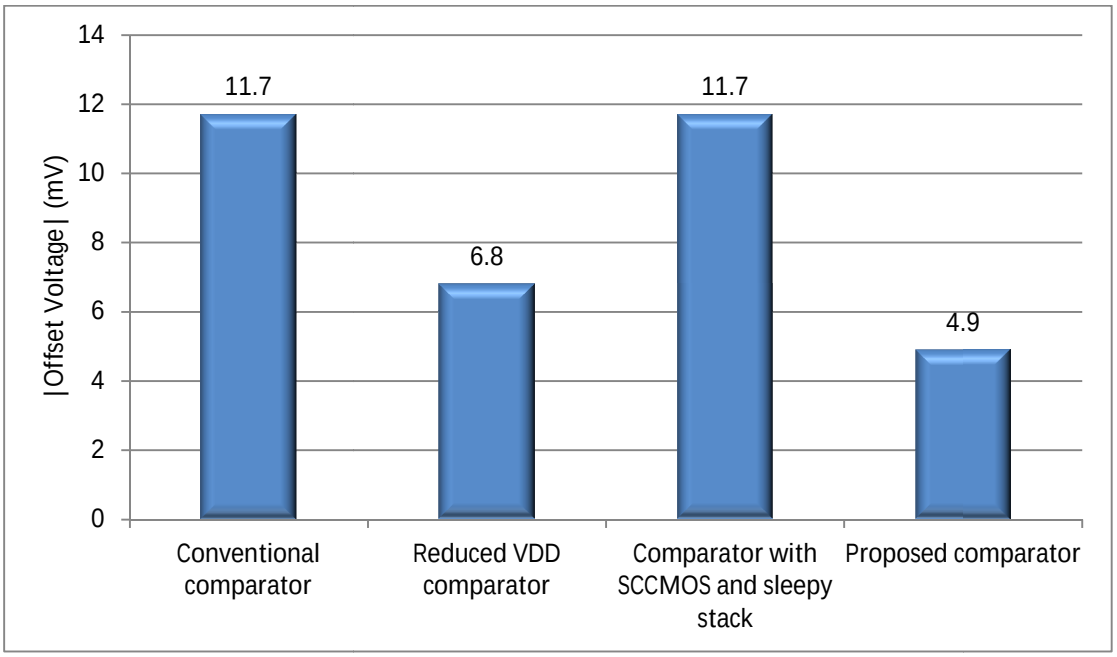


Figure 4.2: Offset

The resolution of conventional comparator, reduced V_{DD} comparator, comparator with SCCMOS and sleepy stack as well as proposed comparator is shown in Figure 4.3. The bar chart shows that the proposed comparator has the smallest resolution while the comparator with SCCMOS and sleepy stack has the biggest resolution. Reduced V_{DD} comparator has the second smallest resolution followed by conventional comparator.

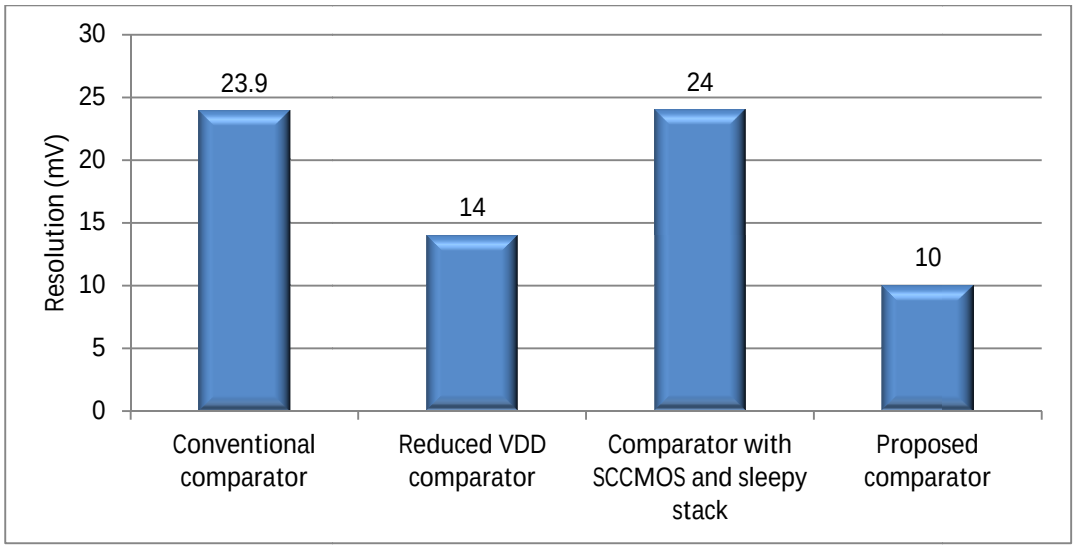


Figure 4.3: Resolution

Figure 4.4 shows that conventional comparator has the highest voltage gain and followed by the proposed comparator, comparator with SCCMOS and sleepy stack. Reduced V_{DD} comparator has the lowest voltage gain.

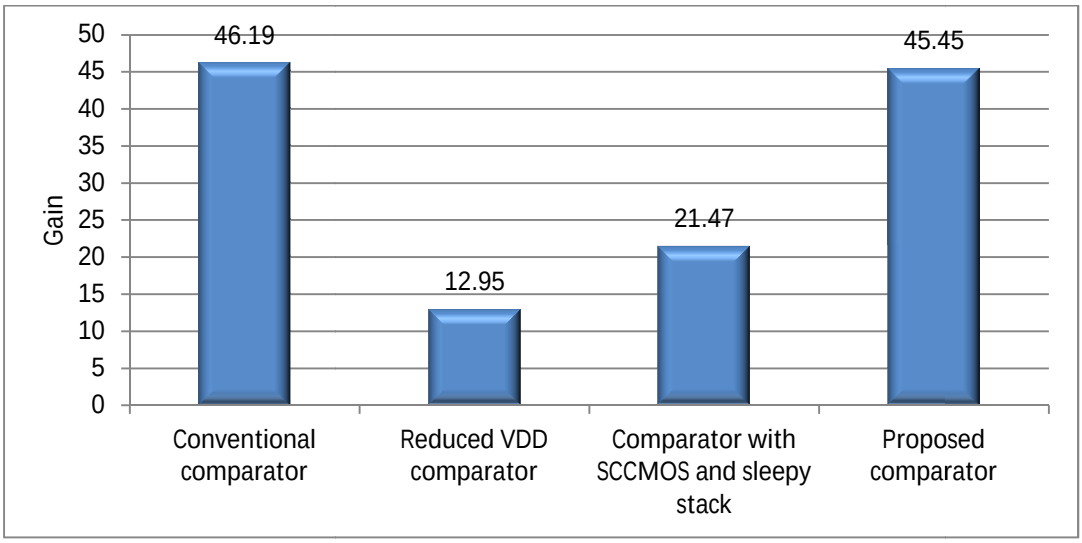
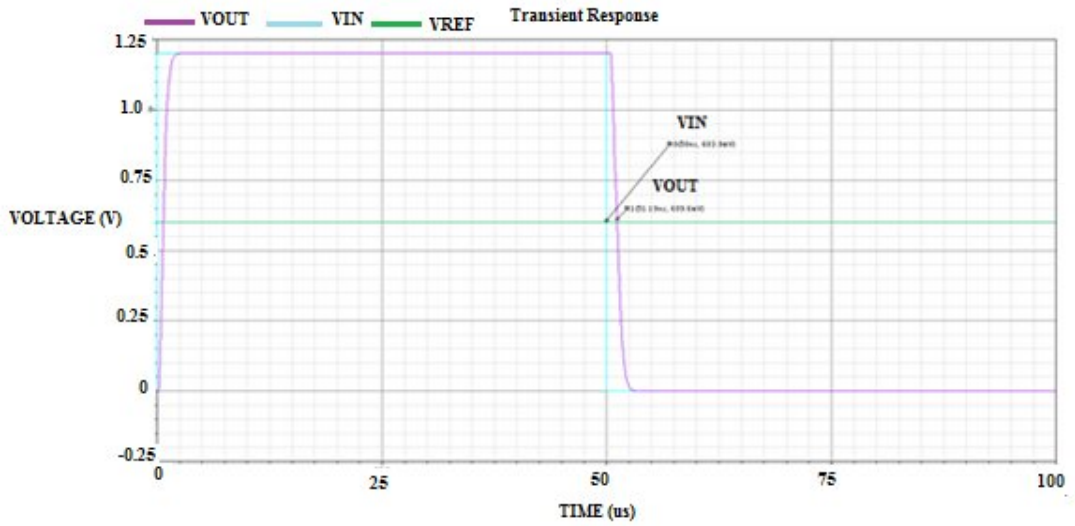


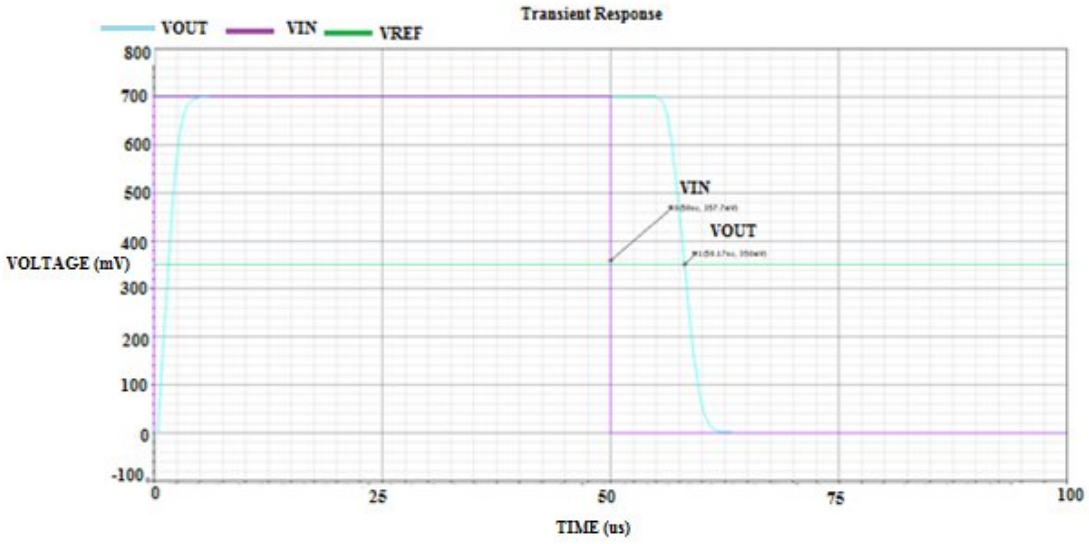
Figure 4.4: Voltage gain

4.1.2 Dynamic Characteristic

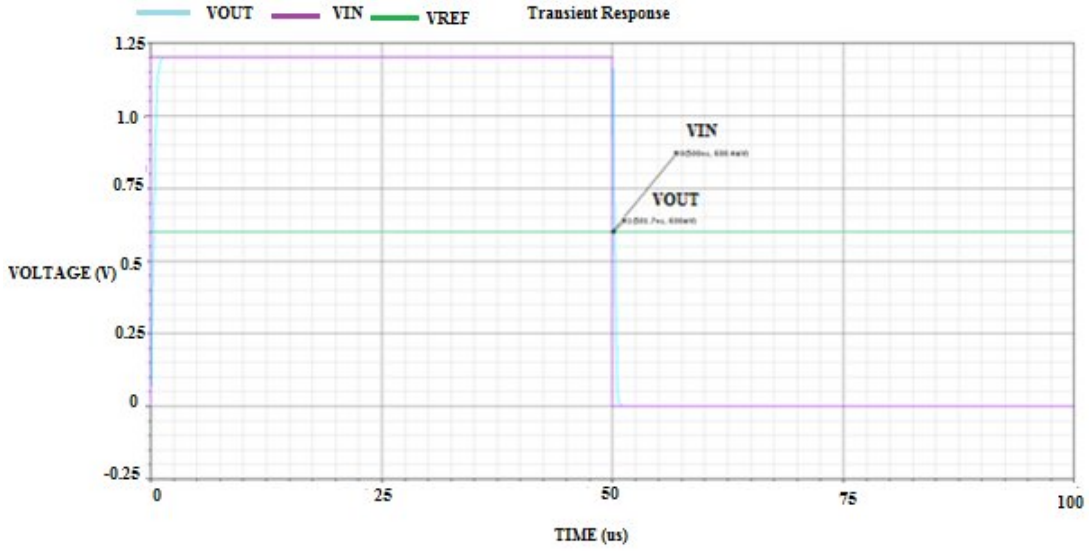
Transient analysis was run in order to calculate the propagation delay. The analysis ran for exactly one cycle. The pulse signal was used as the input signal. Propagation delay is the time taken for the input to produce changes at the output. In this study, the delay measured by calculating the difference of input and output signal at 50% transition of logic 0 to logic 1. Figure 4.5 shows transient response of conventional comparator, reduced V_{DD} conventional comparator, comparator with sleepy stack and SCCMOS and proposed comparator. From the transient response, the delay for each design was calculated. Bar chart in Figure 4.6 shows the propagation delay for conventional comparator reduced V_{DD} comparator, comparator with SCCMOS and sleepy stack as well as proposed comparator. It shows that the proposed comparator has the highest delay while the conventional comparator has the lowest delay followed by comparator with SCCMOS and sleepy stack and reduced V_{DD} comparator.



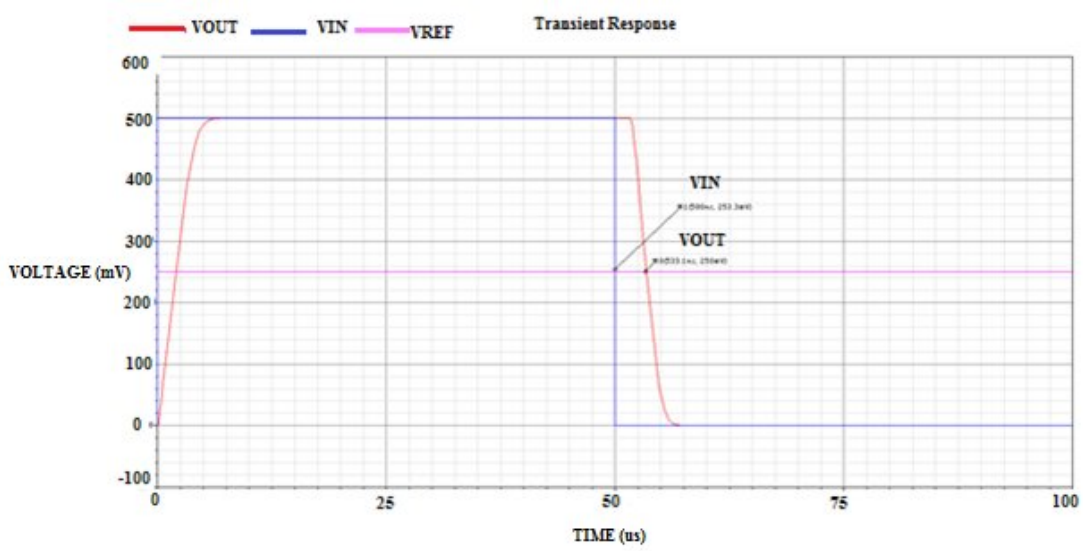
(a)


Transient Response
VOUT
VIN
VREF
800
700
600
500
400
300
200
100
0
-100
VOLTAGE (mV)
VIN
VOUT
0
25
50
75
100
TIME (us)

(b)


VOUT
VIN
VREF
Transient Response
1.25
1.0
0.75
0.5
0.25
0
-0.25
VOLTAGE (V)
VIN
VOUT
0
25
50
75
100
TIME (us)

(c)



(d)

Figure 4.5: Transient response of (a) conventional comparator (b) reduced V_{DD} conventional comparator, (c) Comparator with sleepy stack and SCCMOS and (d) proposed comparator

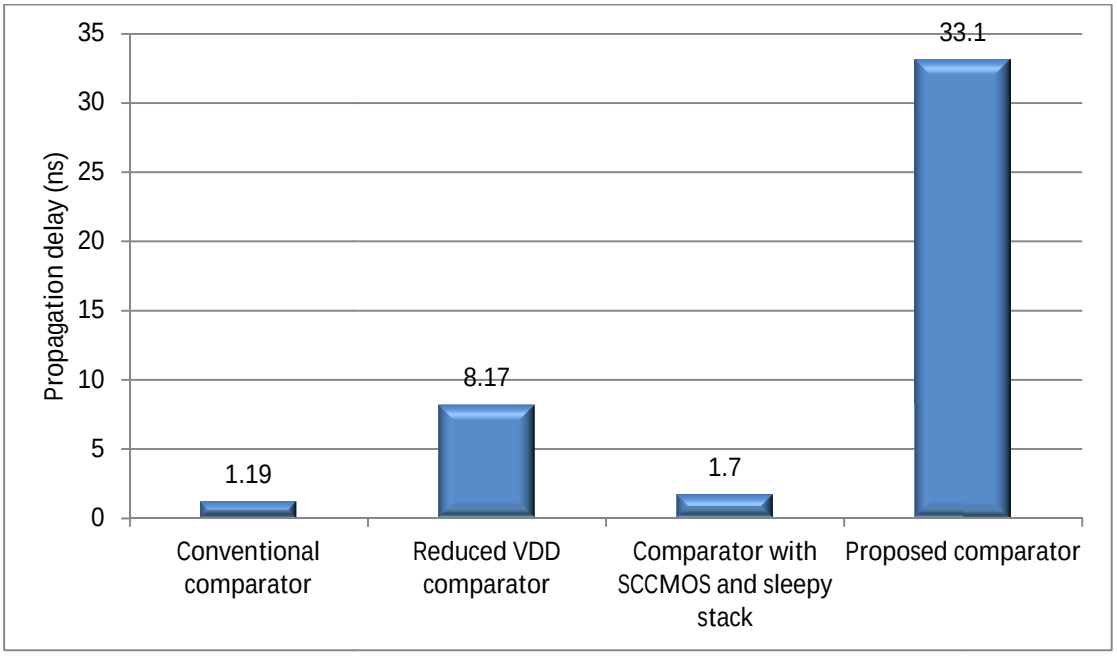


Figure 4.6: Propagation delay

4.1.3 Power Consumption

In this study, dynamic power and static power were measured. The dynamic power was measured when there was switching activity. The pulse input signal was used as the input when measuring the dynamic power. On the other hand, a static DC voltage was applied as input signal when measuring the static power. Figure 4.2 shows the static power and dynamic power of conventional comparator, reduced V_{DD} comparator, comparator SCCMOS and sleepy stack and proposed comparator. The table also shows the voltage supply as well as the NMOS body biasing and PMOS body biasing. Proposed comparator has the lowest power consumption for both dynamic and static power.

Table 4.2: Power Consumption

Type of comparator	**V_{DD}**	**V_{BP}**	**V_{BN}**	**Static power**	**Dynamic power**
Conventional comparator	1.2 V	1.2V	0.0 V	404.2 µW	1.127 mV
Reduced V_{DD} comparator	0.7 V	0.7 V	0 V	53.84 µW	138.0 µW
Comparator with SCCMOS and sleepy stack	1.2 V	1.2 V	0 V	608.6 pW	381.9 µW
Proposed comparator	0.5 V	0.3 V	0.2 V	94.66 pW	14.76 µW

Figure 4.7 shows that there are very significant reduction of dynamic power and static power for proposed comparator compared to the conventional comparator. The reduction of power for

comparator with SCCMOS and sleepy stack is more significant for static power but less significant for dynamic power. Reduced V_{DD} comparator also has outstanding significant reduction of power for both dynamic and static power compared to conventional comparator.

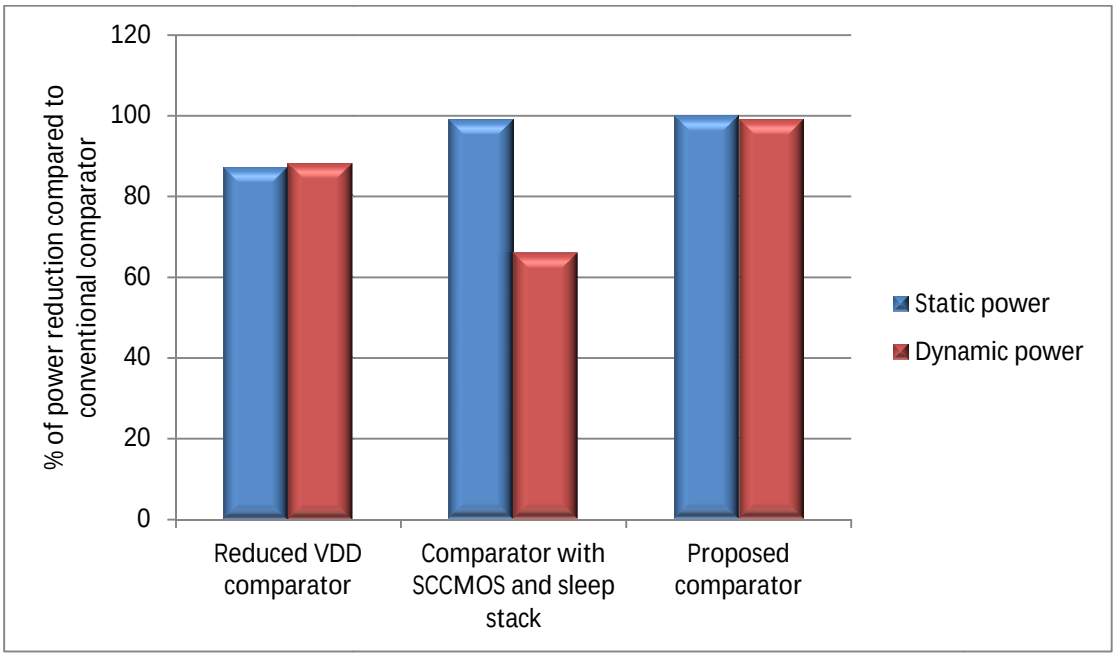


Fig.4.7: Percentage of power reduction compared to conventional comparator

4.2 Post-layout Simulation

4.2.1 Static Characteristic

Figure 4.8 shows the transfer curve from post-layout simulation of proposed comparator. From the transfer curve, the upper input (V_{IH}), lower input (V_{IL}), upper output (V_{OH}) and lower output (V_{OL}) were measured. The measured results are presented in Table 4.3. In the table, the calculated offset and resolution are also presented.

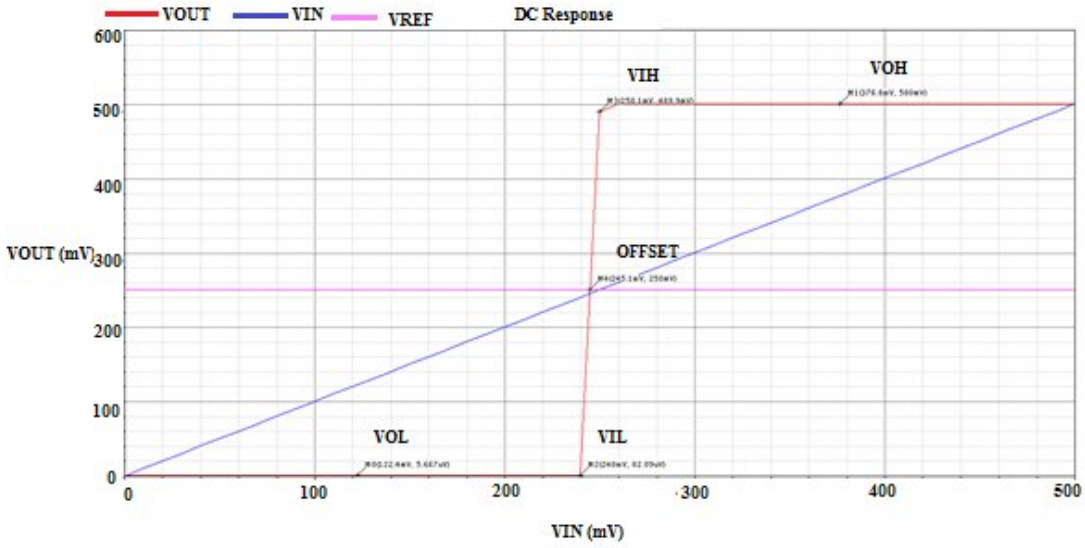


Fig. 4.8: Transfer curve of proposed comparator from post layout simulation

Table 4.3: Static characteristic of proposed comparator

Characteristics	**Proposed Comparator**
Output high voltage, V_{OH}	500.0 mV
Output low voltage, V_{OL}	0.0 V
Input high voltage, V_{IH}	250.1 mV
Input low voltage, V_{IL}	240.0 mV
Offset	-4.9 mV
Resolution	10.1 mV

4.2.2 Dynamic Characteristic

Figure 4.9 shows the transient response of proposed comparator from post-layout simulation. The measurement of V_{IN} and V_{OUT} were taken at 50% of the signal transition. As shown in Table 4.4, the propagation delay for the proposed comparator in post-layout simulation is 39.1 ns.

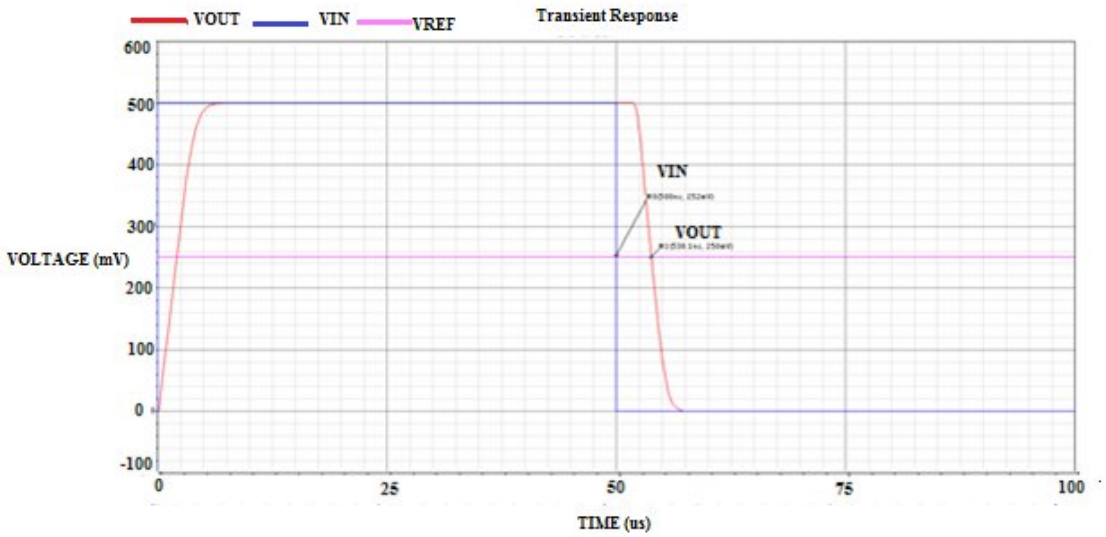


Fig. 4.9: Transient response of proposed comparator from post-layout simulation

Table 4.4: Dynamic characteristic of proposed comparator

Characteristics	Proposed Comparator
Delay	38.1 ns

4.2.3 Power consumption

Table 4.5 presents the power consumption of proposed comparator in post-layout simulation. The static power consumption is very small which about 700 pW. This is due to the super-cut off CMOS technique applied to the circuit. The technique almost totally cut off the current flow from the supply to the ground during sleep mode. The dynamic power consumption from post-layout simulation is 236.9 μW.

Table 4.5: Power consumption of proposed comparator

Characteristic	Proposed comparator
Dynamic power	236.9 μW
Static power	703.3 pW

4.3 Comparison Pre-layout Simulation and Post-layout Simulation

Table 4.6 shows the characteristic comparison between pre-layout simulation and post-layout simulation. The $V_{OH,}$ $V_{OL,}$ V_{IL} and offset are similar. Meanwhile the V_{IH} and resolution are almost similar. The propagation delay and power consumption are higher in post-layout simulation. This is due to post-layout simulation includes the parasitic RC extraction. The delay in pre-layout simulation is 33.1 ns while in post-layout simulation the delay is 38.1 ns. The delay increases only 5 ns due to parasitic. There are quite significant increases in dynamic power and static power. The dynamic power in pre-layout simulation is 14. 6 μW compared to 236.9 μW in

post-layout simulation. For static power, the increase is from 94.66 pW in pre-layout simulation to 703.3 pW in post-layout simulation.

Table 4.6: Pre-layout simulation and post-layout simulation result comparison

Characteristics		**Pre-layout**	**Post-layout**
Output high voltage, V_{OH}		500.0 mV	500.0 mV
Output low voltage, V_{OL}		0.0 V	0.0 V
Input high voltage, V_{IH}		250.0 mV	250.1 mV
Input low voltage, V_{IL}		240.0 mV	240.0 mV
Offset		-4.9 mV	-4.9 mV
Delay		33.1 ns	38.1 ns
Resolution		10 mV	10.1 mV
Power Consumption	Dynamic	14.76 µW	236.9 µW
	Static	94.66 pW	703.3 pW

4.4 Summary

This chapter has presented the result from pre-layout and post-layout simulation. In pre-layout section, the performance of conventional comparator, comparator with SCCMOS and sleepy stack, reduced V_{DD} comparator and proposed comparator were compared. The post-layout simulation section only presented the result for proposed comparator only. This is due to only layout for proposed comparator has been done. The part of this chapter has presented the pre-layout simulation and post-layout simulation result.

CHAPTER 5

CONCLUSION AND RECOMMENDATION

5.1 Conclusion

The proposed comparator with body biasing, super cut-off CMOS and sleep transistor technique shows a very significant reduction in power consumption. Dynamic power consumption is 236.9 μW and static power consumption is 703.3 pW for the proposed comparator. Compared to conventional comparator, the dynamic power consumption and static power consumption is 404.4 uW and 1.127 mW respectively. Previously, super cut-off CMOS and sleep transistor are mostly applied on digital circuit only. This work has proved that these techniques are also suitable to be implemented in analog circuit. By applying appropriate body biasing to the bulk of NMOS and PMOS devices, the threshold voltage of the device is able to be altered. The advantage of lowering the threshold voltage is allowing reduction in supply voltage. The supply voltage is well known as the effective way to reduce power consumption. Without altering the body biasing, the performance of comparator has degraded. The biggest performance that degraded when supply voltage reduced is the propagation delay.

Besides improvement in power consumption, the proposed comparator also has an outstanding performance in offset and resolution. The offset of the proposed comparator is only -

0.005 V while resolution is only 0.01 V. The resolution indicates the sensitivity of comparator for any voltage change. In other word, the proposed comparator is able to toggle even when there is voltage change as small as 0.01 V. The smaller resolution, the comparator performs better.

Even though the proposed comparator has improvement in power consumption, the proposed comparator has high delay which is 38.1 ns compared to conventional comparator delay which is only 1.19 ns. This proposed comparator design is not likely to be used in high speed design such as analog to digital converter. This proposed comparator is more suitable for portable electronic medical devices where the accuracy and reliability are more important than the speed.

5.2 Recommendation

The following are the further works that can be done to improve this work:

1. By using smaller CMOS technology, others power reduction techniques such as sub-threshold region, floating gate MOSFET and level shifter approach can be investigated. Besides that, the significance of static power in total power consumption also able to investigate comprehensively. Since this work is using 0.13 µm CMOS Technology, the effect of static leakage current is not very significant. The static leakage starts contribute the most to total power consumption for technology 65 nm and below.

2. This work is focusing on power reduction only. Others comparator performance such as delay, operation frequency, offset and resolution are the potential area to explore. The

technique such as auto-zeroing and hysteresis are example of techniques that can improve comparator performance. Besides that, the area of layout also has not been optimized. By optimizing the layout, the parasitic can be reduced. Hence improve the delay as well as the dynamic power consumption. Thus, these two areas can be explored more in future.

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APPENDICES

APPENDIX A

Pre-layout Netlist

```
// Library name: sch_comparator
// Cell name: sch_proposed_comparator
// View name: schematic
subckt sch_proposed_comparator clk clkbar out vbias vbn vbp vdd vn vp
vss
    NM0 (net88 vp net53 vbn) nm_hp w=(2u) l=(130n) as=680f ad=680f \
        ps=4.68u pd=4.68u m=1 sa=340n sb=340n sd=0 nf=1
    NM1 (net104 vn net53 vbn) nm_hp w=(2u) l=(130n) as=680f ad=680f \
        ps=4.68u pd=4.68u m=1 sa=340n sb=340n sd=0 nf=1
    NM2 (net53 vbias net73 vbn) nm_hp w=(4u) l=(130n) as=1.36p ad=760f
\
        ps=9.36u pd=4.76u m=1 sa=340n sb=340n sd=380n nf=2
    NM3 (net62 net70 net73 vbn) nm_hp w=(2u) l=(130n) as=680f ad=680f
\
        ps=4.68u pd=4.68u m=1 sa=340n sb=340n sd=0 nf=1
    NM4 (out net62 net82 vbn) nm_hp w=(1u) l=(130n) as=340f ad=340f \
        ps=2.68u pd=2.68u m=1 sa=340n sb=340n sd=0 nf=1
    NM5 (net70 net70 net73 vbn) nm_hp w=(2u) l=(130n) as=680f ad=680f
\
        ps=4.68u pd=4.68u m=1 sa=340n sb=340n sd=0 nf=1
    NM10 (vdd out net113 vbn) nm_hp w=(1u) l=(130n) as=340f ad=340f \
        ps=2.68u pd=2.68u m=1 sa=340n sb=340n sd=0 nf=1
    NM7 (net73 clk vss vbn) nm_hp w=(2u) l=(130n) as=680f ad=680f
ps=4.68u \
        pd=4.68u m=1 sa=340n sb=340n sd=0 nf=1
    NM9 (net82 clk vss vbn) nm_hp w=(1u) l=(130n) as=340f ad=340f
ps=2.68u \
        pd=2.68u m=1 sa=340n sb=340n sd=0 nf=1
    PM0 (net70 net88 net89 vbp) pm_hp w=(4u) l=(130n) as=1.36p
ad=1.36p \
        ps=8.68u pd=8.68u m=1 sa=340n sb=340n sd=0 nf=1
    PM3 (net104 net104 net89 vbp) pm_hp w=(4u) l=(130n) as=1.36p
ad=1.36p \
        ps=8.68u pd=8.68u m=1 sa=340n sb=340n sd=0 nf=1
    PM4 (net104 net88 net89 vbp) pm_hp w=(4u) l=(130n) as=1.36p
ad=1.36p \
        ps=8.68u pd=8.68u m=1 sa=340n sb=340n sd=0 nf=1
    PM1 (net88 net88 net89 vbp) pm_hp w=(4u) l=(130n) as=1.36p
ad=1.36p \
        ps=8.68u pd=8.68u m=1 sa=340n sb=340n sd=0 nf=1
    PM2 (net88 net104 net89 vbp) pm_hp w=(4u) l=(130n) as=1.36p
ad=1.36p \
        ps=8.68u pd=8.68u m=1 sa=340n sb=340n sd=0 nf=1
    PM5 (net62 net104 net89 vbp) pm_hp w=(4u) l=(130n) as=1.36p
ad=1.36p \
        ps=8.68u pd=8.68u m=1 sa=340n sb=340n sd=0 nf=1
```

```
    PM6 (out net62 net113 vbp) pm_hp w=(2u) l=(130n) as=680f ad=680f \
        ps=4.68u pd=4.68u m=1 sa=340n sb=340n sd=0 nf=1
    PM10 (net113 clkbar vdd vbp) pm_hp w=(2u) l=(130n) as=680f ad=680f
\
        ps=4.68u pd=4.68u m=1 sa=340n sb=340n sd=0 nf=1
    PM7 (net89 clkbar vdd vbp) pm_hp w=(4u) l=(130n) as=1.36p ad=1.36p
\
        ps=8.68u pd=8.68u m=1 sa=340n sb=340n sd=0 nf=1
    PM11 (vss out net82 vbp) pm_hp w=(2u) l=(130n) as=680f ad=680f \
        ps=4.68u pd=4.68u m=1 sa=340n sb=340n sd=0 nf=1
ends sch_proposed_comparator
// End of subcircuit definition.
```

APPENDIX B

Post-layout Netlist

```
// File: sch_proposed_comparator.pex.netlist
// Created: Sun Jun  8 16:15:42 2014
// Program "Calibre xRC"
// Version "v2011.1_15.11"
//
simulator lang=spectre
include "sch_proposed_comparator.pex.netlist.pex"
subckt sch_proposed_comparator (  CLKBAR CLK VBIAS VP VN OUT VSS VBN
VDD VBP )
//
// VBP     VBP
// VDD     VDD
// VBN     VBN
// VSS     VSS
// OUT     OUT
// VN VN
// VP VP
// VBIAS   VBIAS
// CLK     CLK
// CLKBAR  CLKBAR
XMNM2\@2 ( N_NET53_MNM2\@2_d N_VBIAS_MNM2\@2_g N_NET73_MNM2\@2_s
N_VBN_MNM9_b ) \
 NM_HP l=1.3e-07 w=2e-06 ad=6.8e-13 as=3.8e-13 pd=4.68e-06 ps=2.38e-06
nrd=0.17 \
 nrs=0.095 sa=3.4e-07 sb=8.5e-07
XMNM2 ( N_NET53_MNM2_d N_VBIAS_MNM2_g N_NET73_MNM2\@2_s N_VBN_MNM9_b )
NM_HP \
 l=1.3e-07 w=2e-06 ad=6.8e-13 as=3.8e-13 pd=4.68e-06 ps=2.38e-06
nrd=0.17 \
 nrs=0.095 sa=8.5e-07 sb=3.4e-07
XMNM9 ( N_NET82_MNM9_d N_CLK_MNM9_g N_VSS_MNM9_s N_VBN_MNM9_b ) NM_HP
l=1.3e-07 \
 w=1e-06 ad=3.4e-13 as=3.4e-13 pd=2.68e-06 ps=2.68e-06 nrd=0.34
nrs=0.34 \
 sa=3.4e-07 sb=3.4e-07
XMNM4 ( N_OUT_MNM4_d N_NET62_MNM4_g N_NET82_MNM4_s N_VBN_MNM9_b )
NM_HP \
 l=1.3e-07 w=1e-06 ad=3.4e-13 as=3.4e-13 pd=2.68e-06 ps=2.68e-06
nrd=0.34 \
 nrs=0.34 sa=3.4e-07 sb=3.4e-07
XMNM10 ( N_VDD_MNM10_d N_OUT_MNM10_g N_NET113_MNM10_s N_VBN_MNM9_b )
NM_HP \
 l=1.3e-07 w=1e-06 ad=3.4e-13 as=3.4e-13 pd=2.68e-06 ps=2.68e-06
nrd=0.34 \
 nrs=0.34 sa=3.4e-07 sb=3.4e-07
```

```
XMPM10 ( N_NET113_MPM10_d N_CLKBAR_MPM10_g N_VDD_MPM10_s N_VBP_MPM10_b
) PM_HP \
 l=1.3e-07 w=2e-06 ad=6.8e-13 as=6.8e-13 pd=4.68e-06 ps=4.68e-06
nrd=0.17 \
 nrs=0.17 sa=3.4e-07 sb=3.4e-07
XMPM6 ( N_OUT_MPM6_d N_NET62_MPM6_g N_NET113_MPM6_s N_VBP_MPM10_b )
PM_HP \
 l=1.3e-07 w=2e-06 ad=6.8e-13 as=6.8e-13 pd=4.68e-06 ps=4.68e-06
nrd=0.17 \
 nrs=0.17 sa=3.4e-07 sb=3.4e-07
XMPM11 ( N_VSS_MPM11_d N_OUT_MPM11_g N_NET82_MPM11_s N_VBP_MPM10_b )
PM_HP \
 l=1.3e-07 w=2e-06 ad=6.8e-13 as=6.8e-13 pd=4.68e-06 ps=4.68e-06
nrd=0.17 \
 nrs=0.17 sa=3.4e-07 sb=3.4e-07
XMPM5 ( N_NET62_MPM5_d N_NET104_MPM5_g N_NET89_MPM5_s N_VBP_MPM5_b )
PM_HP \
 l=1.3e-07 w=4e-06 ad=1.36e-12 as=1.36e-12 pd=8.68e-06 ps=8.68e-06
nrd=0.085 \
 nrs=0.085 sa=3.4e-07 sb=3.4e-07
XMNM7 ( N_NET73_MNM7_d N_CLK_MNM7_g N_VSS_MNM7_s N_VBN_MNM9_b ) NM_HP
l=1.3e-07 \
 w=2e-06 ad=6.8e-13 as=6.8e-13 pd=4.68e-06 ps=4.68e-06 nrd=0.17
nrs=0.17 \
 sa=3.4e-07 sb=3.4e-07
XMNM5 ( N_NET70_MNM5_d N_NET70_MNM5_g N_NET73_MNM5_s N_VBN_MNM9_b )
NM_HP \
 l=1.3e-07 w=2e-06 ad=6.8e-13 as=6.8e-13 pd=4.68e-06 ps=4.68e-06
nrd=0.17 \
 nrs=0.17 sa=3.4e-07 sb=3.4e-07
XMNM0 ( N_NET88_MNM0_d N_VP_MNM0_g N_NET53_MNM0_s N_VBN_MNM9_b ) NM_HP
\
 l=1.3e-07 w=2e-06 ad=6.8e-13 as=6.8e-13 pd=4.68e-06 ps=4.68e-06
nrd=0.17 \
 nrs=0.17 sa=3.4e-07 sb=3.4e-07
XMNM1 ( N_NET104_MNM1_d N_VN_MNM1_g N_NET53_MNM1_s N_VBN_MNM9_b )
NM_HP \
 l=1.3e-07 w=2e-06 ad=6.8e-13 as=6.8e-13 pd=4.68e-06 ps=4.68e-06
nrd=0.17 \
 nrs=0.17 sa=3.4e-07 sb=3.4e-07
XMNM3 ( N_NET62_MNM3_d N_NET70_MNM3_g N_NET73_MNM3_s N_VBN_MNM9_b )
NM_HP \
 l=1.3e-07 w=2e-06 ad=6.8e-13 as=6.8e-13 pd=4.68e-06 ps=4.68e-06
nrd=0.17 \
 nrs=0.17 sa=3.4e-07 sb=3.4e-07
XMPM7 ( N_NET89_MPM7_d N_CLKBAR_MPM7_g N_VDD_MPM7_s N_VBP_MPM5_b )
PM_HP \
 l=1.3e-07 w=4e-06 ad=1.36e-12 as=1.36e-12 pd=8.68e-06 ps=8.68e-06
nrd=0.085 \
 nrs=0.085 sa=3.4e-07 sb=3.4e-07
XMPM0 ( N_NET70_MPM0_d N_NET88_MPM0_g N_NET89_MPM0_s N_VBP_MPM5_b )
PM_HP \
```

```
 l=1.3e-07 w=4e-06 ad=1.36e-12 as=1.36e-12 pd=8.68e-06 ps=8.68e-06
nrd=0.085 \
 nrs=0.085 sa=3.4e-07 sb=3.4e-07
XMPM1 ( N_NET88_MPM1_d N_NET88_MPM1_g N_NET89_MPM1_s N_VBP_MPM5_b )
PM_HP \
 l=1.3e-07 w=4e-06 ad=1.36e-12 as=1.36e-12 pd=8.68e-06 ps=8.68e-06
nrd=0.085 \
 nrs=0.085 sa=3.4e-07 sb=3.4e-07
XMPM2 ( N_NET88_MPM2_d N_NET104_MPM2_g N_NET89_MPM2_s N_VBP_MPM5_b )
PM_HP \
 l=1.3e-07 w=4e-06 ad=1.36e-12 as=1.36e-12 pd=8.68e-06 ps=8.68e-06
nrd=0.085 \
 nrs=0.085 sa=3.4e-07 sb=3.4e-07
XMPM4 ( N_NET104_MPM4_d N_NET88_MPM4_g N_NET89_MPM4_s N_VBP_MPM5_b )
PM_HP \
 l=1.3e-07 w=4e-06 ad=1.36e-12 as=1.36e-12 pd=8.68e-06 ps=8.68e-06
nrd=0.085 \
 nrs=0.085 sa=3.4e-07 sb=3.4e-07
XMPM3 ( N_NET104_MPM3_d N_NET104_MPM3_g N_NET89_MPM3_s N_VBP_MPM5_b )
PM_HP \
 l=1.3e-07 w=4e-06 ad=1.36e-12 as=1.36e-12 pd=8.68e-06 ps=8.68e-06
nrd=0.085 \
 nrs=0.085 sa=3.4e-07 sb=3.4e-07
//
include
"sch_proposed_comparator.pex.netlist.SCH_PROPOSED_COMPARATOR.pxi"
//
ends SCH_PROPOSED_COMPARATOR
//
//
```