ANALYSIS OF PARTIAL BINARY TREE NETWORK (PBTN) FOR DYNAMIC ELEMENT MATCHING (DEM) DIGITAL TO ANALOG CONVERTER (DAC)

by

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LIST OF ABBREVIATIONS

ADC	Analog to Digital Converter
BTN	Binary Tree Network
DAC	Digital to Analog Converter
DEM	Dynamic Element Matching
DNL	Differential Non-Linearity
GCN	Generalized Cube Network
INL	Integral Non-Linearity
LSB	Least Significant Bit
MSB	Most Significant Bit
PBTN	Partial Binary Tree Network
SFDR	Spurious Free Dynamic Range

ABSTRAK

Dalam banyak sistem digital, DAC prestasi tinggi adalah penting untuk memastikan pengendalian yang baik. Komponen dipadankan diperlukan untuk mencapai penukaran data yang betul. Banyak faktor seperti perubahan proses dan suhu boleh menyebabkan komponen menjadi tidak berpadanan, oleh itu ia adalah mustahil untuk mereka komponen sempurna dipadankan sepanjang masa. Komponen tidak berpadanan akan membawa kepada perbezaan dalam nilai direka dan nilai yang sebenar. Salah satu teknik untuk mengurangkan kesan komponen tidak berpadanan adalah dengan menggunakan Pemadanan Elemen Dinamik (DEM) rangkaian untuk rawakkan kod input digital kepada DAC. Perawakan ini boleh membantu menjadikan masa purata komponen bersamaan pada setiap kedudukan untuk menjadi hampir sama. Masalah dengan pelaksanaan DEM sedia ada adalah prestasi kelinearan daripada DAC tidak begitu sesuai dan mempunyai gangguan disebabkan oleh peralihan pelbagai suis pada masa yang sama. Dalam kajian ini, pelaksanaan 2 MSB rawak adalah dicadangkan pada Rangkaian Pokok Sebahagian Perduaan (PBTN) DEM DAC dan prestasinya dinilai dari segi gangguan, penggunaan kuasa, DNL dan INL. Perbandingan telah dilakukan untuk 4-bit BTN, 4-bit PBTN dan 4-bit (2 MSB) PBTN. Satu lagi perbandingan yang telah dilakukan kepada prestasi untuk 6-bit & 8-bit (1 MSB) PBTN dan 6-bit & 8-bit (2 MSB) PBTN DEM DAC. Simulasi telah dilakukan dan 8-bit (2 MSB) PBTN DEM DAC menghasilkan gangguan maksimum 259.4 mV, DNL bersamaan 2.46 LSB dan INL bersamaan 31.00 LSB.

ABSTRACT

In many digital systems, high performance DACs is essential to ensure proper operations. Matched components are required in order to achieve proper data conversion. Many factors such as process variation and temperature can cause components to be mismatched therefore it is impossible to fabricate perfectly matched components all the time. Mismatched components will lead to difference in designed values and actual values. One of the techniques to reduce the effect of mismatched components is to use Dynamic Element Matching (DEM) network to randomize the digital input codes to a DAC. This randomization can help to make the time averages of the equivalent components at each position to be nearly equal. The problem with existing DEM implementations is the linearity performance of the DAC is not as ideal and has glitches due to transitions of multiple switches at the same time. In this research, the implementation of 2 MSB randomization is proposed on a Partial Binary Tree Network (PBTN) DEM for a current-steering DAC and its performance evaluated in terms of glitches, DNL and INL. Comparison was done for 4-bit BTN, 4-bit PBTN and 4-bit (2 MSB) PBTN. Another comparison was done for performance for 6-bit & 8-bit (1 MSB) PBTN and 6-bit & 8-bit (2 MSB) PBTN DEM DAC. Simulation was done and the 8-bit (2 MSB) PBTN DEM DAC yields maximum glitch of 259.4 mV, DNL of 2.46 LSBs, and DNL of 31.00 LSBs.

CHAPTER 1: INTRODUCTION

1.1 Background Overview

Electronic devices, commonly found in our daily lives, use both digital and analog signals depending on its function. Mostly, analog signals such as temperature, pressure, sound, images etc., are converted to digital signals in order for simpler processing in digital systems. In these systems, the converted digital signals are processed and will required to be converted back to analog signals to perform some real-world function *(Figure 1-1)*. The conversion of digital to analog is done by a digital-to-analog converter (DAC), which outputs are used to drive other devices. Devices that use DAC include loudspeakers, motors, temperature controls, motors, video displays and radio frequency (RF) transmitters (Douglas, 2014).

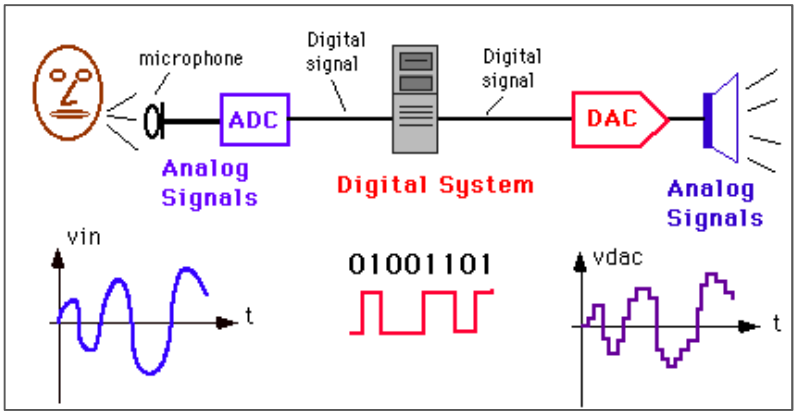

Figure 1-1: Digital systems with an ADC and a DAC

Image from: http://www.seas.upenn.edu/~ese206/labs/adc206/adc206.html

In many digital systems, high performance data convertors are essential. DAC architectures rely highly on matched components to perform data conversion. However,

it is rather impossible to fabricate perfectly matched components. There are always errors due to mismatched components between the designed and actual values. These mismatch errors contribute to the static errors of a DAC due to process variations which causes deviations of component values.

There are several techniques that can help to reduce the effects of mismatched components in a DAC. Laser trimming, self-calibration, VLSI layout techniques, and dynamic element matching are a few of the techniques that may help to reduce the errors caused by mismatched components. In this research, the focus is on implementing a new methodology for the Dynamic Element Matching (DEM) technique. The aim is to implement 2 MSB randomization on a Partial Binary Tree Network DEM.

DEM works by randomly selecting appropriate codes for each of the digital input value before it is being routed to the DAC block as shown in *Figure 1-2*. The purpose of the random selection is to reduce the effects of component differences in the circuits. This is done to make the time averages of equivalent components at each of the component positions equal or nearly equal (Bruce, 2000).

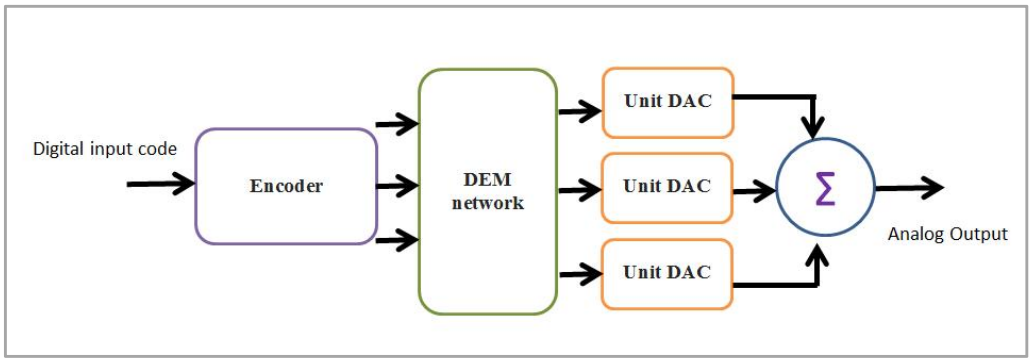

Figure 1-2: DEM Network connection to DAC

There are different methodologies in implementing DEM DACs. These will be further discussed in the following chapters.

1.2 Problem Statement

As mentioned previously, DEM can be implemented to reduce the effects of errors caused by mismatched components. There are many types of DEM DACs that have been published using different properties and methodologies. However, the downside of implementing the DEM network is the DAC would then have excessive digital hardware complexity which will lead to high hardware cost. In a conventional DEM network, many switch transitions occur at the same moment in high speed applications. Glitches are generated when too many switch transitions occur at the same time in a DEM network (Wei Su, 2012). In the case of a Full Random DEM (FRDEM), glitches are noticed at the output signal due to high number of switches are being randomized at the same time (Henrik, 1998). Glitches are due to the mismatch in switching times across different switches (Andersson, 2000).

Ideally an optimized balance between hardware complexity and DAC performance is desired to reduce hardware cost without sacrificing on the performance of the DAC.

1.3 Objective

The main objectives for this research are:

1. Implement 2 MSB randomization on an 8-bit PBTN DEM DAC.
2. Analyze and compare the performance of 1 MSB versus 2 MSB randomization on PBTN DEM DAC.

1.4 Scope

The scope of this research covers the design of the switchable current source unit of a current-steering DAC. Design of a 4-bit BTN DEM, a 4-bit PBTN DEM and a 4-bit PBTN DEM with 2 MSB randomization was done, and a comparison of their performance is done. This research also covers the implementation of 2 MSB randomization on the PBTN DEM for a 6-bit DAC and an 8-bit DAC and their performances analyzed.

The design is designed using the Silterra's CL130G technology which is a 0.13 µm CMOS technology. The design of the system will be using 1.8V for its V_{dd} and a full-scale voltage DAC output of 1V. The proposed methodology was designed and simulated using Cadence Virtuoso software. The body effect caused by connecting the source to the bulk of the transistors are not taken into account in this research as the design is only done on the schematic level and layout implementation effects are not considered.

In this research, the DAC architecture that is being used is the current-steering DAC which applies most commonly for high speed application. The implementation of 2 MSB randomization is done on the Partial Binary Tree Network (PBTN) DEM as proposed to evaluate the performance of the DAC in an effort to improve the linearity of the existing PBTN 1 MSB randomization methodology.

1.5 Thesis Outline

This chapter is an overview of the research to understand the background and introduction to the research. The problem statement points to component mismatch and its impact on the performance of DACs. The objective of the research is to implement a new methodology of 2 MSB randomization on a PBTN DEM DAC in order to evaluate its performance.

Chapter 2 is the literature review. Various types of DAC architectures are introduced to identify the suitable architecture to be used for this research. The introduction of existing methodologies of DEM network implementation is also discussed. Measurement metrics to evaluate DAC performance are also studied in this chapter. The outcome of this chapter is to establish the requirement of this research.

Chapter 3 discusses the methodology for designing of switchable current source unit that makes up a current-steering DAC. This chapter also discusses the design of the transmission gate which is the element used to build the binary tree network for the DEM.

Chapter 4 showcases the results of the simulation and performance of the DACs in terms of its DNL and INL. Simulation is done for 4-bit BTN DEM DAC, 4-bit PBTN DEM DAC, 4-bit PBTN (2 MSB) DEM DAC, 6-bit PBTN DEM DAC, 6-bit PBTN (2 MSB) DEM DAC, 8-bit PBTN DEM DAC and 8-bit PBTN (2 MSB) DEM DAC.

Chapter 5 concludes the results and discusses the findings and outcome of this research. Future work to improve this work is also proposed.

CHAPTER 2: LITERATURE REVIEW

2.1 Introduction

A DAC produces a discrete step analog output in response to the binary digital input code given. The digital input of a DAC may be in the form of voltage or current. The output is generated based on a reference quantity which is divided into binary and/or linear fractions. Switches are then driven to combine an appropriate number of these fractions to output. The performance of a DAC can be determined based on several parameters. The common parameters used are:

- **Resolution:** it is normally given in bits. This indicates the smallest increment of its output, corresponding to a 1 LSB input code change.
- **Full scale range (FSR):** the maximum output signal specified as current or voltage. This can be negative, positive or both.
- **Offset error:** the difference between an ideal and actual DAC output when zero digital code is applied to the output.
- **Gain error:** the difference between an ideal and actual output when full scale digital code applied to the input. This is dependent on the stability of Vref.
- **Differential Nonlinearity (DNL):** this is measured with a ramp code applied to the input of DAC. The step between every pair of the adjacent codes should not exceed 1 LSB (1 LSB is calculated from gain and offset measurements).

- **Integral Nonlinearity (INL):** this shows how the output differs from an ideal line. It is measured in LSB where 1 LSB is an acceptable value.
- **Signal to Noise Ratio (SNR):** measured with digital code representing sine wave applied to the input. The fundamental and harmonic components of the sine wave are filtered out and the remaining signal at the output of the DAC is considered as noise. SNR is a ratio of the full scale sine wave output to the noise level.
- **Total Harmonic Distortion (THD):** this is measured with digital code representing sine wave applied to the DAC input continuously. The output (specified in dB) is analyzed in the frequency domain to find harmonic components related to the fundamental output signal.

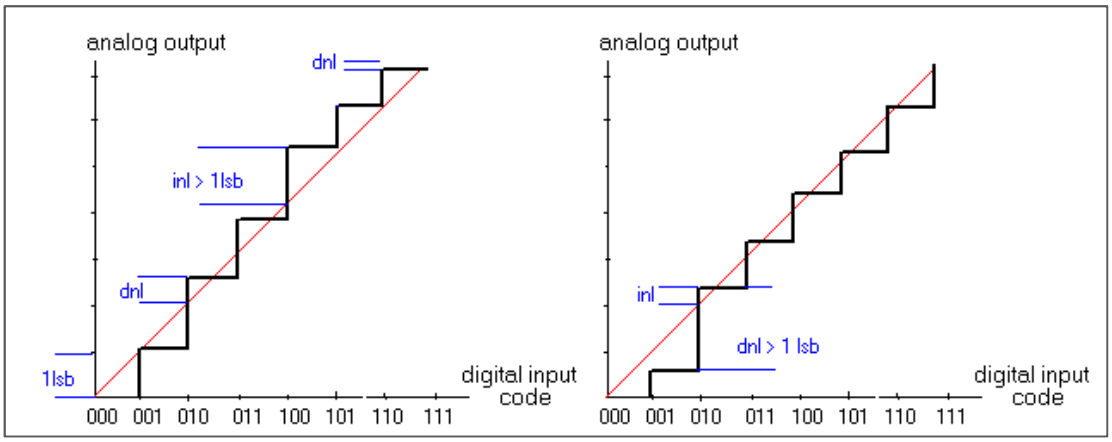

Figure 2-1: (a) DNL less than 1 LSB & INL more than 1 LSB (b) DNL more than 1 LSB & INL less than 1 LSB

Image from: http://www.hitequest.com/Hardware/a_dac.htm

Figure 2-1 illustrates the difference of INL and DNL. The hierarchy of importance for these two parameters is dependent on the DAC's application. In the case of imaging application, DNL is more important as it is necessary to distinguish between slightly

different color densities in adjacent pixels. Whereas in the case of an application in which the readings are widely varied and must be continuously monitored, INL is more important.

2.2 Digital to Analog Converter (DAC) Architectures

There are several types of DAC architectures available. Each of these architectures has its own pros and cons. Generally DAC architectures can be categorized into flash and algorithmic (cyclic). Flash type converters typically take in a parallel input code that will instantaneously control a number of switches in parallel that in turn select a number of weights that should be summed. Flash converters are typically faster but occupy larger chip area. Algorithmic type converters on the other hand take in a serial input to control the weights whose contributions are accumulated in order to generate the output amplitude level after a certain number of clock cycles. Algorithmic converters require smaller chip area but produces lower throughput (Tsai, 2005). For the case of this research, the focus is placed on flash converters.

2.2.1 Binary-Weighted DAC Architecture

Current sources, resistors or capacitors are binary weighted in this architecture (Wikner, 2001). For example, in a binary-weighted resistor scenario, a number of resistors are connected in series and a digital input is weighted on these resistors. When the digital input weighted is increased, the value of these resistors will be decreased exponentially. This architecture is rather straightforward and easy to design but it is only useful for small digital inputs. For larger number of bits, the difference between the MSB and the LSB needs to be significantly larger and this is not practical. The differences in

resistances make the circuit more susceptible to mismatch errors and thus compromising the monotonicity of the DAC (Wikner, 2001).

2.2.2 Current Steering DAC Architecture

This architecture type depends on current-sources which are switch controlled. Two types of 'weight' can be used for this: the binary-weighted and the unary-weighted (Maloberti, 2008).

The binary-weighted uses the number of current sources based on the number of bits intended for the resolution. This approach allows design on a smaller area and lower power consumption but may be lacking in terms of accuracy. This is due to the number of switches are not proportional to the change of the input code where the mid-scale transition have all the switches exercised while all but one switch is exercised at quarter or three quarter of the full scale therefore resulting in large glitches (Maloberti, 2008).

In a unary-weighted scenario, all current sources provide a unity current value which is associated with the LSB. Current-steering DACs are made up of current sources that are summed. The advantage to this architecture is its high-current drive inherent in the system (Baker, 2010). Unary-weighted designs are generally better at higher resolution but costs more in terms of design area size. Putting aside the design area size of the unary-weighted architecture, it is considered superior to the binary-weighted design. Unary selection gives better switching performances as the magnitude of a glitch is proportional to the number of switches that are actually switching (Maloberti, 2008).

A mixture of both binary-weighted and unary-weighted approach leads to a segmented current steering topology (Maloberti, 2008). Weighted current steering architecture

generally has a faster response compared to the voltage switching method as the reference current is not interrupted and no significant voltage appear across all switches but only at the output.

2.2.3 Thermometer-Coded DAC Architecture

Thermometer-coded DAC uses a binary-to-thermometer decoder circuit. Generally, the digital input needs to be converted to the thermometer code which consists of $2^N - 1$ thermometer bits where *N* refers to the number of bits for the digital input (Wikner, 2001). The reference elements for this design are all of equal size which in turn makes component matching much simpler as compared to binary-weighted method. This architecture is well known for its monotonic transfer and low glitch noise. This is so because whenever the input value increases, the bits are only turning from 0 to 1. This architecture is usually used for low resolution implementation else the encoding circuit will be too large to be practical (Wikner, 2001).

2.2.4 Summary of DAC Architectures

For this research, the unary-weighted current-steering architecture is preferred as it is suitable for higher resolution and it does not require designing of the binary-weighted segment of the circuit. The selection was done after considering the comparison of each architecture as shown in *Table 2-1*.

Table 2-1: Comparison of DAC Architectures

	Binary-Weighted	Current-Steering	Thermometer-Coded
Ease of Design	Easy	Moderate	Moderate
Resolution	Low	High	Low
Area of Design	Large	Small	Large
Power Consumption	--	Low	--

2.3 DAC Performance Measurements

DAC's performance can be analyzed based on static and dynamic performance. Static performance measurement parameters include the offset errors, gain errors and linearity. There are two types of linearity analysis that can be done: Differential Nonlinearity (DNL) and Integral Nonlinearity (INL). Dynamic performance measurement parameters of a DAC include settling time, glitch impulse area and distortion.

2.3.1 Static Performance Measurements

Offset errors and gain errors are relatively easier to overcome as compared to the linearity. Linearity is the most important aspect to consider of the types of static performance of DAC. It is more complicated and costly to ensure the linearity of a DAC design.

Differential Nonlinearity (DNL) is defined as the difference between the actual step width and the ideal step width of 1 LSB as shown in *Figure 2-2*. An ideal DNL is desired where each bit has the same step. DNL that is <1 LSB will cause DAC to behave as non-monotonic therefore causing loss of data after the conversion.

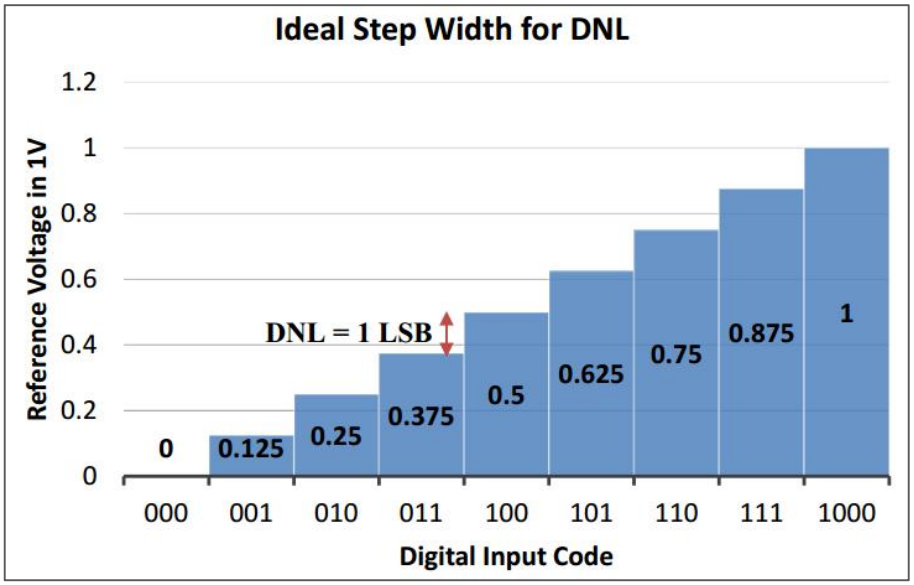

Figure 2-2: Ideal Step Width for DNL

Integral Nonlinearity (INL) is defined as the difference between the ideal output and the actual output. The ideal output refers to a straight line drawn through the actual zero and the full scale of the DAC as shown by the red line in *Figure 2-3.*

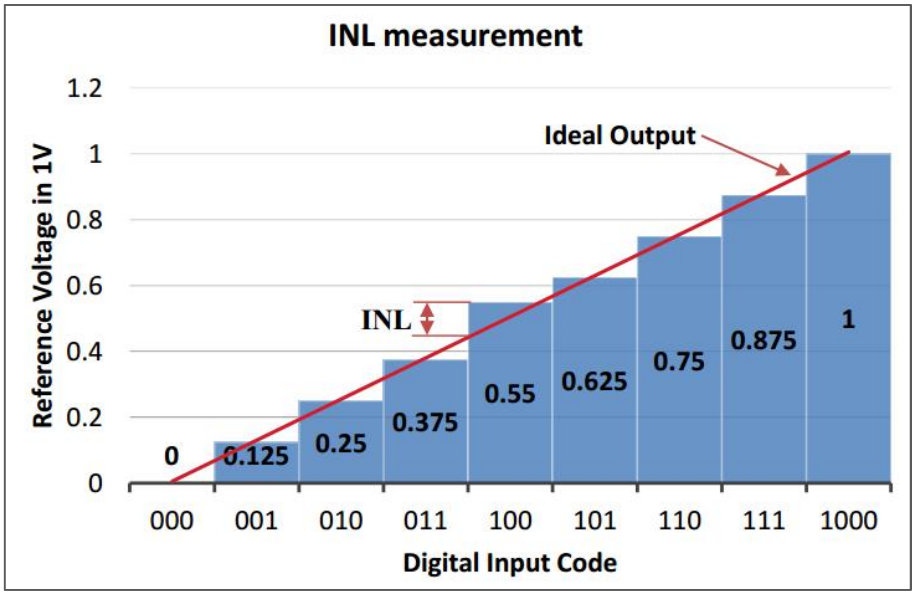

Figure 2-3: INL Measurement

DNL and INL of a DAC can be measured using the superposition method for binary-weighted DACs (Kester, 2005). This method is applicable to DACs which the individual output or resultant responses is added to determine the true operation of the circuit. As shown in *Figure 2-4*, a 3-bit DAC is with superposition. The offset and gain errors have been removed from the data points so that the zero and full-scale errors are zero. As can be seen in *Figure 2-4*, the DAC has an error in the first and second bit weights. The value of the DNL is calculated for each of the eight possible output voltages. The transfer function has a non-monotonicity at the 100 code with a DNL of negative 3 LSBs. The INL for any output of the DAC is the algebraic sum of the DNLs leading up to that particular output. For the instance of this 3-bit DAC:

$$INL_{101} = DNL_{001} + DNL_{010} + DNL_{011} + DNL_{100} + DNL_{101}$$

$$= 0 + 1.5 + 0 - 3 + 0 = -1.5\ LSBs$$

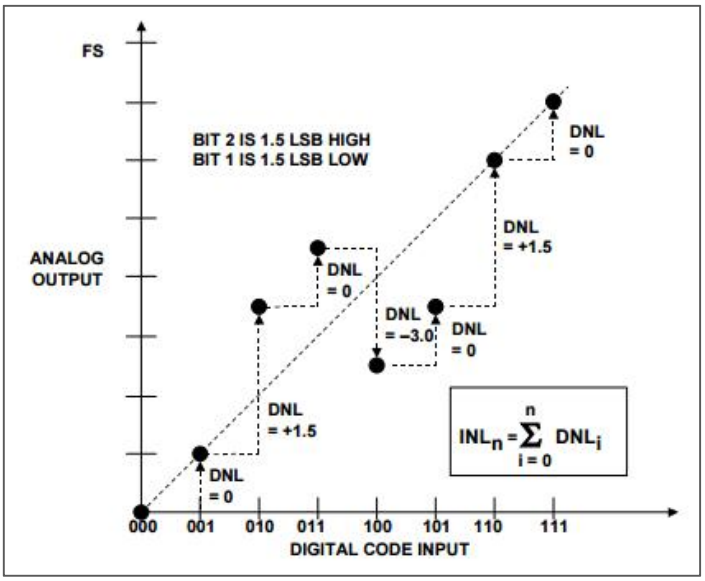

Figure 2-4: 3-bit DAC Transfer Function where Superposition is used

Image from: http://www.analog.com/library/analogDialogue/archives/39-06/Chapter%205%20Testing%20Converters%20F.pdf

Superposition method may not hold for DAC architectures such as resistor string DACs. This is due to the varying individual bit weights. In this case a non-superposition method is used to measure the DNL and INL (Kester, 2005).

2.3.2 Dynamic Performance Measurements

Dynamic performances of a DAC are commonly measured using oscilloscopes and spectrum analyzers. Parameters measured by oscilloscopes include settling time and glitch impulse area. Spectrum analyzers are used to measure various distortion and noise-related parameters such as Spurious-Free Dynamic Range (SFDR), Total Harmonic Distortion (THD), Signal-to-Noise Ratio (SNR) and Signal-to-Noise and Distortion Ratio (SINAD) (Kester, 2005).

Settling time is a crucial parameter to consider when designing DAC for high speed application such as video displays. Settling time refers to the amount of time required for the output to settle within the specified error band measured with respect to the 50% point of the time when the input data to the switches changes (Kester, 2005). There are four periods that made up the total settling time as can be seen from *Figure 2-5*. The dead time or switching time is during digital switching but not changing in output; slew time is during the rate of change of the output; recovery time is referring to the time where DAC is recovering from its fast slew and overshoot; and linear settling time is when DAC output approaches its final value in an exponential or near exponential manner (Kester, 2005).