DESIGN AND IMPLEMENTATION OF LOW POWER AND HIGH PERFORMANCE 4 BIT CARRY LOOKAHEAD FULL ADDER USING FINFET TECHNOLOGY

By

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LIST OF SYMBOLS

ASIC	-	Application Specific Integrated Circuit
ALU	-	Arithmetic Logic Unit
DSP	-	Digital Signal Processing
MOSFET	-	Metal Oxide Semiconductor Field-Effect Transistor
RCA	-	Ripple Carry Adder
CLA	-	Carry Look-Ahead
CSlA	-	Carry Select Adder
CSkA	-	Carry Skip Adder
CSA	-	Carry Save Adder
CIA	-	Carry Increment Adder
PDP	-	Power Delay Product
PFA	-	Partial Full Adder
LEF	-	Library Exchange Format
MW	-	MilkyWay
DRC	-	Design Rule Check
LVS	-	Layout Versus Schematic
CCS	-	Composite Current source
CPL	-	Complementary Pass-Transistor Logic
LER	-	Line-Edge Roughness

REKA BENTUK DAN PELAKSANAAN 4 BIT PENAMBAH BAWA LIHAT KE DEPAN YANG BERKUASA RENDAH DAN BERPRESTASI TINGGI DENGAN MENGGUNAKAN TEKNOLOGI FINFET

ABSTRAK

Unit Aritmetik Logik (ALU) adalah litar digital dan ia digunakan untuk melaksanakan semua operasi aritmetik dan operasi logik. Selain itu penambah adalah bahagian yang paling penting di kalangan ALU kerana ia telah digunakan dalam operasi aritmetik lain. Sekarang terdapat tiga parameter prestasi utama iaitu Dimensi, Kelajuan dan Kuasa tertumpu oleh pereka VLSI untuk penambahbaikan reka bentuk mereka. Maka, peningkatan kelajuan di penambah akan mempercepatkan pelaksanaan semua operasi aritmetik lain. Penambah Bawa Lihat Ke Depan (CLA) telah dipilih kerana ia mempercepatkan pengiraan dengan mengurangkan jumlah masa dalam penentuan bit untuk menjalankan operasi penambahan dengan lebih cepat. 4-bit CLA boleh dilaksanakan dengan pelbagai jenis transistor, seperti FinFet dan Transistor Kesan Medan Separuh Pengalir Oksida Logam (MOSFET). Di project ini, CLA yang menggunakan teknologi 14nm FinFET dalam Penghantaran Pintu (TG) telah mengesahkan kebolehan teknologi baru ini di dalam reka bentuk penambah penuh terdapat pengurangan kira-kira 52% dalam nilai parameter pelesapan kuasa berbanding teknik 22nm CMOS. Kesimpulannya, ia telah menunjukkan bahawa litar CLA yang dicadangkan dalam 14nm FinFET dalam TG dapat menyediakan kelajuan yang lebih baik dengan kuasa pelesapan-kurangnya berbanding dengan kerja-kerja sebelumnya.

DESIGN AND IMPLEMENTATION OF LOW POWER AND HIGH PERFORMANCE 4 BIT CARRY LOOKAHEAD FULL ADDER USING FINFET TECHNOLOGY

ABSTRACT

An Arithmetic Logic Unit (ALU) is a digital circuit and used to perform all arithmetic operations and logic operations. Addition is the most important part among of the ALU since it has been used in other arithmetic operation. Now there are three main performance parameters i.e. area, speed and power are focused by VLSI designer to optimize their design. Therefore, improving the speed of addition increase the performance of all other arithmetic operations. The Carry Look-Ahead Adder (CLA) has been chosen because it speeds up the carry computation by reducing the amount of time to determine carry bits. The 4-bit CLA Full Adder can be implemented with different types of transistor, such as FinFET and Metal Oxide Semiconductor Field-Effect Transistor (MOSFET), which may have difference performance in supply voltage variation. In this project, the analysis of the simulated results confirm the feasibility of the 14nm FinFET techniques in Transmission Gate (TG) style full adder design and shows that there is reduction of approximately 52% in the value of power dissipation parameter as compared to CMOS 22nm technique. In conclusion, it has been shown that the proposed CLA circuit in 14nm FinFET in TG provides better speed with the least power dissipation compared to the previous works.

CHAPTER 1

INTRODUCTION

1.1 Overview

An Arithmetic Logic Unit (ALU) is a digital circuit and used to perform all logic operations and arithmetic operations, namely addition, subtraction, multiplication and division. The ALU has been used in microprocessor, digital signal processing (DSP) and data processing system.

Addition is the most important part among of the ALU since it has been used in other arithmetic operation. Many processing operation like counting, filtering and etc. usually involve addition. It involves a carry propagation step which propagates a carry signal from each bit to next higher bit position. In the past, the major challenge for VLSI designer is to reduce the area of chip. Now there are three main performance parameters i.e. area, speed, power are focused by designer to optimize their designs.

Carry Look-Ahead Adder (CLA) is a very important building block for digital circuit. Most of other arithmetic operations are implemented using addition therefore, improving the speed of addition able to speed up the performance of all other arithmetic operations. The Carry Ripple Adder (CRA) is the simplest adder but the carry propagation time is the major speed limiting factor. In the CRA, the result in the next stage is obtained after the carry generated by the previous stage is produced. The sum of the most significant is only available after the carry-out of the full adder has rippled from the least

significant stage to the next most significant stage. Thus, the final sum and carry bits will be valid after a considerable delay. Therefore, the CLA has been chosen because it speeds up the carry process by reducing the amount of time to determine carry bits. The CLA is able to generate carries before the sum is produced using propagate and generate logic to make addition much faster.

FinFET is a new alternatives structure for MOSFET which allows transistors to be scaled down to smaller sizes. It has been reported that FinFET devices has more advantages over conventional MOSFET such as lower gate leakage current [1], excellent control of short-channel effects [2], and also relative immunization to the gate line-edge roughness (LER) [4].

A standard cell library contains the high quality timing, power, parasitic models that accurately and efficiently capture behaviors of standard cell. These metrics are written in a different files format since it is widely used in many design tools for various purposes, such as static timing analysis, power analysis, logic synthesis and so on. The Synopsys Liberty-format (.lib) is one of the important kits which is widely utilize for static timing analysis and logic synthesis [3].

The contribution of this project is in three-fold. Firstly, the 4-bit Carry Look-ahead (CLA) Full Adder standard cell has been created by using 14nm FinFET devices. Next, full adder has been characterized in Liberty format at two type of supply voltage to get the behaviors of standard cell such as timing, power, delay and parasitic models. Finally the delay and power consumption of 14nm CLA have been compared with the previous work using Synopsys Design Compiler and the results indicate that the proposed 4-bit CLA circuit have lower power and delay values as compared to previous work.

1.2 Problem Statements

Carry Look-Ahead (CLA) and Ripple Carry Adder (RCA) is a type of adder used in digital logic. In the previous work [22], designers have designed three different 4-bit Transmission Gate Based Full Adders namely Ripple Carry Adder (RCA), Adder, Carry Look-Ahead Adder (CLA) and Carry Select Adder (CSA). The average power consumption, delay and number of transistors have been compared among three different adders in the project. In the project, the result shows that the delay in CLA is less than RCA and CSA. Although the RCA is the simplest adder but the carry propagation time is the major speed limiting factor. So, to defeat the speed limitation in CRA, the CLA Full Adder design solves this problem by calculating the carry signals in advance.

According to Moore's law, the number of transistors in an area should double every months [26]. When scaling down the device channel length, the short channel effects are raised and these effects are captured by new technology FinFET. FinFET able to reduce the short channel effect of the scale down devices because of their better electrostatic control over the channel[26]. Besides, FinFET has more advantages than MOSFET technology in term of leakage power, operating power, transistor gate delay and leakage current [26]. Based on the previous paper [26], Jency proposed a 4-bit full adder using FinFET at 45nm technology with power supply of 0.7V. The target of the project is to reduce the leakage power of a 4-bit full adder using FinFET.

Furthermore, the performance of a full adder circuit depends greatly on the type of design used for implementation and also on the logic function realized using the particular design style. In the previous work [28], different logic styles have been used by designers to analyze the performance of a full adder such as conventional CMOS full adder, parallel prefix adders, hybrid full adders, and mirror full adders, adders using transmission gates and multiplexer logic. Based on the performance analysis, designers concluded that the Transmission Gate logic style provides better speed and the least power dissipating adder compared to the Mirror logic style.

Therefore, the low power of 4 bit Carry Look-Ahead Full Adder using Transmission Gate (TG) logic style in 14nm FinFET Technology will be designed and developed to improve the efficiency and performance of power management.

1.3 Aims and Objectives

The aim of the research as follow:

i. To design a low leakage power and high performance of the 4 bit CLA full adder digital standard cell in generic 14nm FinFET technology.

ii. To verify the 4 bit CLA full adder digital standard cell to ensure the proposed adder cell is good choice in low power design.

1.4 Scope of Study

The project is focused on development of low power 4-bit Carry Look-Ahead Full Adder using Transmission Gate (TG) logic style. All the circuits presented in the project are designed using Cadence Virtuoso environment and have been done on 14nm FinFET technology. The range of supply voltage is 0.40V-1.80V. The parameter of width of both n-type and p-type is tabulated in Table below.

Table 1.1 Optimized Parameters for PMOS and NMOS Transistor

Transistor	Width (um)	Length (um)
	Technology = 14nm	
PMOS	0.084	0.014
NMOS	0.084	0.014

Schematic of 1-bit Transmission Gate (TG) Full Adder and 1-bit Mirror Style Full Adder have been design and comparison with the existing design for power and performance are undertaken in this phase to study and evaluate the effectiveness of the proposed design. Then, 4-bit Carry Look-Ahead Full Adder is developed using Transmission Gate (TG) Logic style based full adder and evaluate the circuit to analyze the result in order to meet the objectives of the project.

1.5 Thesis Outline

This thesis is organized into five chapters.

The first chapter contains overview, problem statements, aims and objectives, scope of the study and thesis outline.

The chapter two consist literature review of the topology used in implement the full adder design. Literature review basically contained all the concept, theory, basic operation and designs of Carry Look-Ahead Full Adder. Besides, the characterization process will be discussed in this chapter. Finally,

the chapter will address the better strategy aimed at improving previous existing design to provide the low power and high performance for full adder circuit.

The next chapter outlines the design and implementation of the 4-bit CLA full adder and also including the reason for choosing the type of CLA used in the full adder circuit. A flow chart is used to describe the flow of project and block diagram of the system is also discussed in this chapter. The flow starts from the schematic design until characterization process.

In the chapter four, the result of 1-bit Transmission Gate (TG) Full Adder and 1-bit Mirror style Full Adder have been analyze and compared. Then, 4-bit Carry Look-Ahead Full Adder is developed using Transmission Gate (TG) Logic Style Based Full Adder and the result is evaluated and analyze. The strategy is benchmark against the previous existing design to evaluate its effectiveness in low power and high performance analysis.

In the chapter five, it consists of conclusions of the project as well as the findings or contribution of the project. It also highlighted the future work that can be done by other peoples as a continuation of this research.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

This chapter discusses the fundamental knowledge of MOS technology and Full Adder. In the adder circuits' design, the design of high performance and low-power adder can be addressed at different levels, such as adder architectures, logic styles and the process technology. Apart from that, previous works have been reviewed and discussed in this chapter.

2.2 MOS technology

The MOS transistor and the symbol of N and P-MOS transistors are shown in Figure 2.1 and Figure 2.2 respectively [29]. Ideally a transistor consist three regions, Source, Drain, and Gate. The source is the main source of charge carriers which is called terminal or node. The charge carriers leave will leave from the source and travel to the drain. In the case of a P channel device (PMOS), the source is the more positive of the terminals whereas in the case of an N channel device (NMOS), the source is the more negative of the terminals. There is the channel formed under the gate oxide. But it needs voltage to form the channel, normally the voltage at which the transistor start conducting which a channel starts to form between the source and the terminal is called the threshold voltage, the transistor is said to be in the 'linear region'. When there is no channel formed under the gate oxide, the transistor at this point is called to

be in the ‘cut off region’. The transistor is said to be in the ‘saturation region’ when no more charge carriers leave from the source and travel to the drain [5].

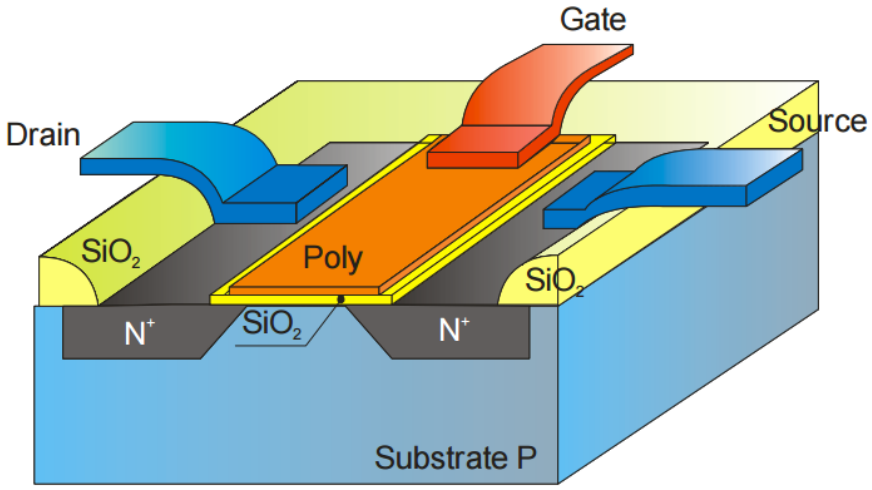

Figure 2.1 MOS Transistor [29]

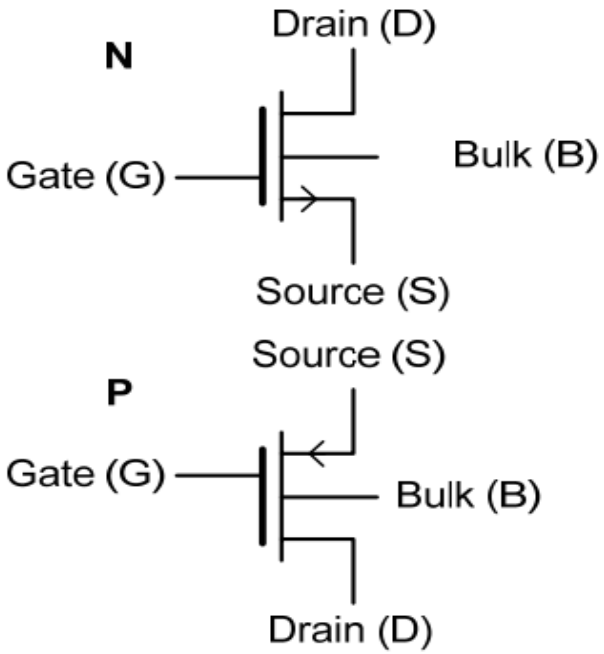

Figure 2.2 Symbols of N and P-MOS transistors [29]

The goal of the transistor is to work as a high speed electrical switch. The switch must be on (conducting) to allow current flows from the source to the drain. There are three functions of the transistor included allow as much

current to flow when it is on(active current), allow as little current to flow when it is off(leakage current), and switch between on and off states as quickly as possible(performance).

FinFET is a new alternative structure for Metal Oxide Semiconductor Field-Effect Transistor (MOSFET). The FinFET and Planar FET are shown in Figure 2.3. A FinFET is new type of multi-gate 3D transistor where the mode of operation is same as the planar MOSFET [6] [7]. The gate of the device wraps over the conducting drain-source channel as Figure 2.3 with the purpose of forming several gate electrodes on each side. This help in providing lower threshold voltages, better electrical properties and improve the performance as well as reduction in both leakage and dynamic power compared to the existing planar CMOS devices.

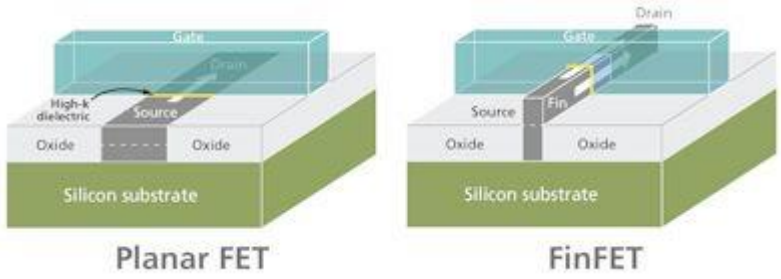

Figure 2.3 FinFET and Planar FET [29]

Moving on the capabilities and specification on the 14nm process, Intel had provided the minimum feature size data for three main critical feature size measurements included transistor fin pitch, transistor gate pitch, and interconnect pitch. These features have been reduced in size between 22% and 35% from 22nm to 14nm. In the 14nm node, there are 35% reduction in the minimum interconnect pitch which is better than normal interconnect scaling as Figure 2.4 and Table 2.1[8].