DESIGN AND SIMULATION OF LOW POWER COMPARATOR USING DTTS AND MTSCSTACK TECHNQUES

By

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TABLE OF CONTENTS

CONTENT	PAGE
ACKNOWLEDGEMENT	iii
TABLE OF CONTENTS	iv
LIST OF TABLES	viii
LIST OF FIGURES	ix
LIST OF ABBREVIATIONS	xii
LIST OF SYMBOLS	xiii
ABSTRAK	xv
ABSTRACT	xvi

CHAPTER 1 INTRODUCTION

1.1 Background 1

1.2 Problem Statement 7

1.3 Objectives of Research 8

1.4 Scope of Research 8

1.5 Research Contribution 9

1.6 Thesis Overview 9

1.7 Chapter Summary 10

CHAPETR 2 LITERATURE REVIEW

2.1 Power consumption 11

2.2 Dynamic Power Dissipation 12

2.2.1 Dynamic Capacitive Power 12

2.2.2 Short circuit Power Dissipation 13

2.2.3 Glitch Power Dissipation 13

2.3 Static Power Dissipation

2.3.1 Reverse Biased pn-junction Current 14

2.3.2 Sub-threshold Leakage 15

2.3.3 Gate Tunelling 16

2.3.4 Gate Induced Drain Leakage 16

2.3.5 Punch Through 17

2.4 Power Reduction Technique 17

2.4.1 Body biasing 18

2.4.2 Multi Threshold CMOS technique (MTCMOS) 20
2.4.3 Super Cut-Off CMOS(SCCMOS) 21
2.4.4 Stack transistor 22
2.4.5 Dual threshold transistor stacking technique 23
2.4.6 Sleepy Stack Transistor Technique 24
2.4.7 Sleepy Keeper Approach 25
2.4.8 MTSCStack Technique 26

2.5 Comparator 27
2.5.1 Comparator Architectures 32
2.5.1.1 Open –loop Comparator 32
2.5.1.2 Regenerative comparator 34
2.5.1.3 High Speed Comparator 35
2.6 Chapter Summary 36

CHAPTER 3 METHODOLOGY
3.1 Research Methodology 37
3.2 Comparator Circuit Design 40
3.3 Comparator Layout Design 51
3.4 Chapter Summary 51

CHAPTER 4	RESULT AND DISCUSSION	
	4.1 Pre-Layout simulation	52
	4.1.1 Static Characteristic	52
	4.1.2 Dynamic Characteristic	59
	4.1.3 Power Consumption	65
	4.2 Post-Layout simulation	67
	4.2.1 Static Characteristic	69
	4.2.2 Dynamic Characteristic	71
	4.2.3 Power Consumption	72
	4.3 Comparison Pre-Layout Simulation and Post-layout Simulation	72
	4.4 Chapter Summary	74
CHAPTER 5	5 CONCLUSION AND RECOMMENDATION	75
	5.1 Conclusion	75
	5.2 Recommendation	76
REFRENCES		78
APPENDICES		82
APPENDIX A	Pre-Layout netlist	83
APPENDIX B	Post-Layout netlist	85

LIST OF TABLES

TABLE	DESCRIPTION	PAGE
3.1	Transistor width and length of conventional comparator	43
3.2	Effect of supply voltage on delay and power consumption	45
3.3	Transistor width and length of proposed comparator	52
4.1	Static Characteristic of a) Conventional comparator, b) Reduced V_{DD} conventional Comparator, c) Comparator with DTTS d) Comparator with MTSCStack and e) Proposed Comparator	60
4.2	Power consumption of conventional comparator, comparator with reduced VDD, comparator with MTSCStack, comparator with DTTS and Proposed comparator.	67
4.3	Static Characteristic of post layout proposed comparator	70
4.4	Delay of post layout proposed comparator	71
4.5	Power consumption of post layout proposed comparator	72
4.6	Comparison Pre-Layout Simulation and Post-layout Simulation	74

LIST OF FIGURES

FIGURE	DESCRIPTION	PAGE
1.1	Microprocessor transistor count	2
1.2	Overall Power consumption Flow Chart	3
2.1	NMOS and PMOS symbol	18
2.2	Multi Threshold CMOS technique (MTCMOS)	21
2.3	SCCMOS Schematic (SCCMOS)	22
2.4	transistor stacking technique	23
2.5	Dual threshold transistor stacking technique	24
2.6	Sleepy stack transistor technique	25
2.7	Sleepy keeper Technique	26
2.8	MTSCStack Technique	27
2.9	Symbol of Comparator	28
2.10	Comparator Ideal Transfer Curve	29
2.11	Comparator Non-Ideal Transfer Curve	30
2.12	Offset Voltage	30
2.13	Two stage open-loop comparator	33
2.14	Push pull output open-loop comparator	33
2.15	Fully differential amplifier and Latch	34
2.16	Preamplifier Comparator	35
2.17	High speed Comparator	36
3.1	Methodology Flow chart	39
3.2	Conventional Comparator schematic	41

3.3	Comparator Parametric analysis	42
3.4	Conventional Comparator Transfer curve	43
3.5	Schematic of comparator with dual threshold Transistor stacking technique	46
3.6	Schematic of comparator with MTSCStack Approach	48
3.7	Schematic of proposed comparator	49
4.1a	Transfer curve of Conventional comparator	53
4.1b	Transfer curve of Reduced V_{DD} conventional Comparator	54
4.1c	Transfer curve of comparator with DTTS	54
4.1d	Transfer curve of comparator with MTSCStack	55
4.1e	Transfer curve of Proposed Comparator	55
4.2	Voltage Gain	57
4.3	Offset	58
4.4	Resolution	58
4.5	Effect of VDD on delay and Power consumption	60
4.6a	Transient analysis of conventional comparator	61
4.6b	Transient analysis of comparator with reduced VDD	62
4.6c	Transient analysis of comparator with DTTS	62
4.6d	Transient analysis of comparator with MTSCStack	63
4.6e	Transient analysis of proposed comparator	63
4.7	Propagation delay	64
4.8	Percentage of Static power reduction compared to conventional comparator	67
4.9	Layout of proposed comparator	68

4.10	DRC report of proposed comparator	68
4.11	LVS report of Proposed Comparator	69
4.12	Transfer curve of proposed comparator of post layout simulation	70
4.10	Transient analysis of proposed comparator of post layout simulation	71

LIST OF ABBREVIATIONS

ABBREVIATIONS	DESCRIPTION
ADC	Analog to digital memory
CAD	Computer aided design
CMOS	Complementary metal oxide semiconductor
DC	Direct current
DRC	Design rule check
DTTS	Dual threshold transistor stacking
FPGA	Field programmable gate array
GIDL	Gate induced drain leakage
GND	Ground
ITRS	International Technology Roadmap for semiconductor
LVS	Layout versus schematic
MOS	Metal oxide semiconductor
MOSFET	Metal oxide semiconductor field effect transistor
MTCMOS	Multi threshold CMOS
NMOS	N channel MOSFET
PEX	Parasitic extraction
PMOS	P channel MOSFET
RC	Resistance capacitance
SCCMOS	Super cut-off CMOS
SRAM	Static random access memory
TPD	Total Propagation delay

TPH	Rising time difference of the output and input
TPL	Falling time difference of the output and input

LIST OF SYMBOLS

SYMBOL	DESCRIPTION
V_{BS}	Bulk Source voltage
V_{D}	Drain voltage
V_{DD}	Drain supply
V_{DS}	Drain source voltage
V_{G}	Gate voltage
V_{GS}	Gate source voltage
V_{IH}	Input upper limit
V_{IL}	Input lower limit
V_{IN}	Input voltage
V_{N}	Inverting input
V_{OH}	Output upper limit
V_{OL}	Output lower limit
V_{OS}	Offset voltage
V_{OUT}	Output voltage
V_{P}	Non-inverting input
V_{SS}	Source supply
V_{TN}	NMOS threshold voltage
V_{TP}	PMOS threshold voltage
V_{BN}	NMOS bulk biasing
V_{BP}	PMOS bulk biasing

REKABENTUK DAN SIMULASI PEMBANDING KUASA RENDAH MENGGUNAKAN TEKNIK-TEKNIK DTTS DAN MTSCSTACK

ABSTRAK

Permintaan untuk pembanding berkuasa rendah dan berkelajuan tinggi dalam penukar analog ke digital (ADC) sedang berkembang dengan pesat. Pembanding adalah blok yang penting dalam ADC. Penggunaan kuasa yang rendah telah menjadi perhatian utama teknologi terkini bagi alat-alat elektronik yang beroperasi pada kelajuan tinggi dengan pelbagai fungsi. Oleh yang demikian, keperluan semakin meningkat untuk peranti elektronik berkuasa rendah tanpa menjejaskan prestasinya. Dalam kajian ini, pembanding konvensional, pembanding dengan VDD rendah, pembanding dengan MTSCStack (*Multi Threshold Super Cut of Stack*) dan pembanding dengan DTTS (*Dual Threshold Transistor Stacking*) telah direka dan disimulasi dengan mengunakan teknologi 0.13 μm proses CMOS. Berdasarkan kajian ini, pembanding berkuasa rendah telah dicadangkan menggunakan gabungan teknik-teknik MTSCStack dan DTTS. Teknik MTSCStack mengurangkan kuasa kebocoran dalam mod aktif dan mengekalkan keadaan logik pada mod senyap. Manakala teknik DTSS bagi mengurangkan arus bocor tanpa memberi kesan kepada kelajuan. Di samping itu, jumlah penggunaan kuasa terutamanya kuasa dinamik telah dikurangkan pada jumlah yang besar melalui pengurangan VDD. Berdasarkan keputusan pasca susun atur, kuasa statik dan dinamik pembanding yang dicadangkan ialah 797 pW dan 17.55 μW.

DESIGN AND SIMULATION OF LOW POWER COMPARATOR USING DTTS AND MTSCSTACK TECHNQUES

ABSTRACT

The demand for high speed and low power comparator in Analog to Digital converter (ADC) is growing rapidly. Comparator is an important building block in ADC. Power consumption tends to be a major concern in today's technology especially the electronic devices that are operating at high speed with multi functionality. Thus, the need is increasing for low power electronic devices without compromising its performance. In this study, conventional comparator, comparator with reduced VDD, comparator with MTSCStack (Multi Threshold Super Cut of Stack) and comparator with DTTS (Dual Threshold Transistor Stacking) have been designed and simulated in 0.13 µm CMOS process technology. Then, based on the study a low power comparator is proposed with MTSCStack and DTTS techniques. MTSCStack is proposed in order to decrease the leakage power in active mode and retaining the logic state of the comparator during the idle state. In other hand, DTSS is proposed to decrease the leakage current with less impact on the delay. In addition, the total power consumption especially dynamic power has been reduced by large amount by decreasing the VDD of the comparator. The static power and dynamic power of the post-layout proposed comparator is 797 pW and 17.55 µW respectively.

CHAPTER 1

INTRODUCTION

This chapter presents the background of this study as well as the problem statement. Furthermore, this chapter also presents the contribution and the overview of this thesis. The objective and the wide scope of this study are included in this chapter.

1.3 Background

Today, there are various portable electronic devices such as smart phone, tablet and laptop are very demanding in today's market. This is because the size is small and easily carried from one place to another. In addition, the portable electronic devices are also been developed in medical field. Examples of portable healthcare electronic devices are Physical Therapy Devices, Diagnostic Imaging Equipment, Respiration Monitors and other medical electronic devices shown rapid development in current healthcare industry. The sizes of the portable devices are shrinking but the performance of the battery is still disappointing for today consumer. This is because the devices are consuming high power which caused the battery life to be short. The performance of battery heavily influenced the characteristic and reliability of the portable electronic devices.

The main component of the portable electronic devices is integrated circuit or known as IC that act as the heart of the devices. IC consist of million to billion transistors. As stated by Moore's Law the number of transistor on IC is doubled every two year or approximately eighteen months.

The Figure 1.1 shows the increasing transistor count exponentially every 18 months or approximately every two years.

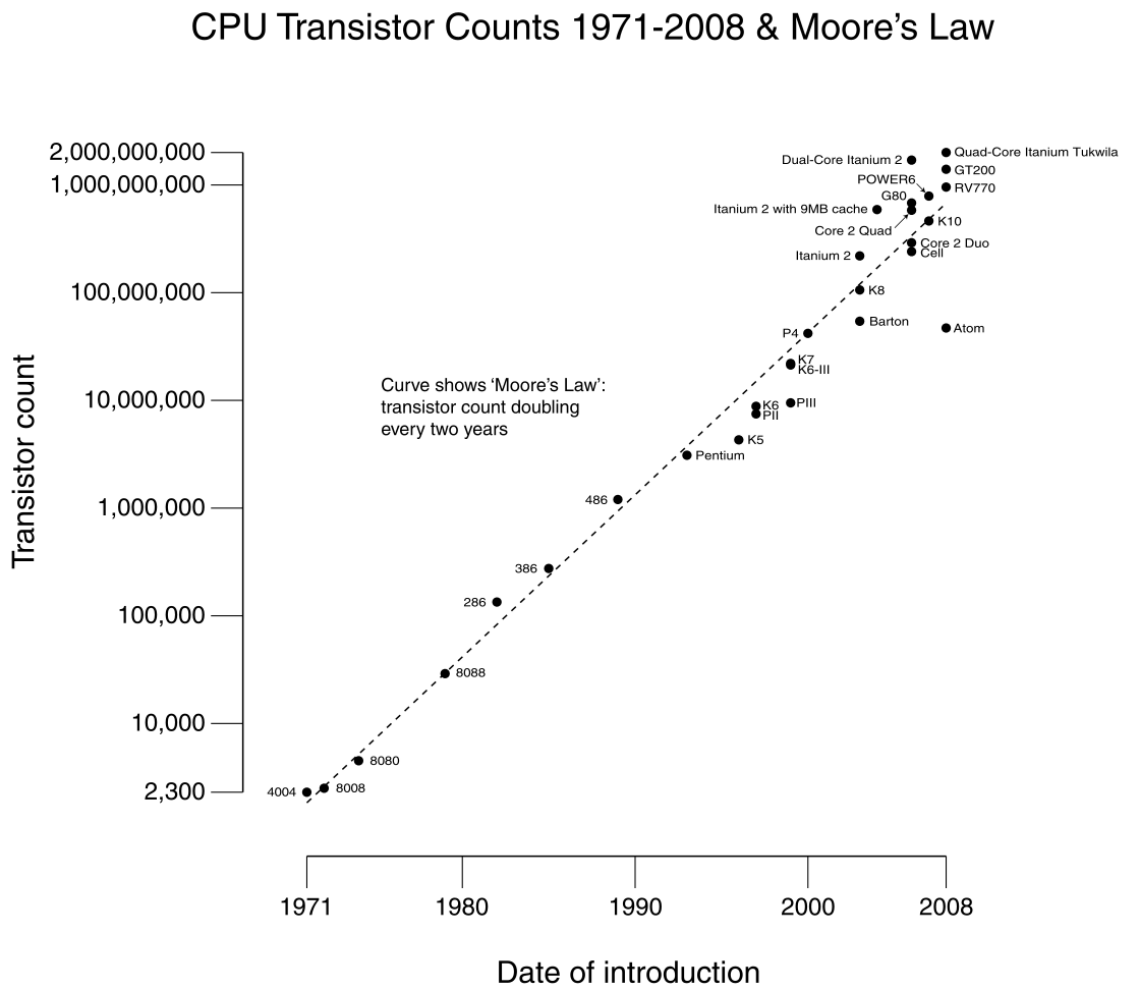

Figure 1.1: Microprocessor transistor count (Wikipedia, 2011)

As more transistors are embedded in a single chip, the power consumption tends to be increasing rapidly. Two types power that contribute to the power consumption of the integrated circuit are the dynamic and static power. Dissipation of power during active state due to switching activity of input signal is known as dynamic power (Jingwei Lu et al., 2012). The dynamic power is consumed when switched from one state to another state. In other words, static power is the power consumption where power dissipated by a gate when it is inactive or standby (Neelam et al., 2013). Current that flow during the inactive state is known as leakage.

The overall power consumption of the integrated circuit is summarized in Figure 1.2.

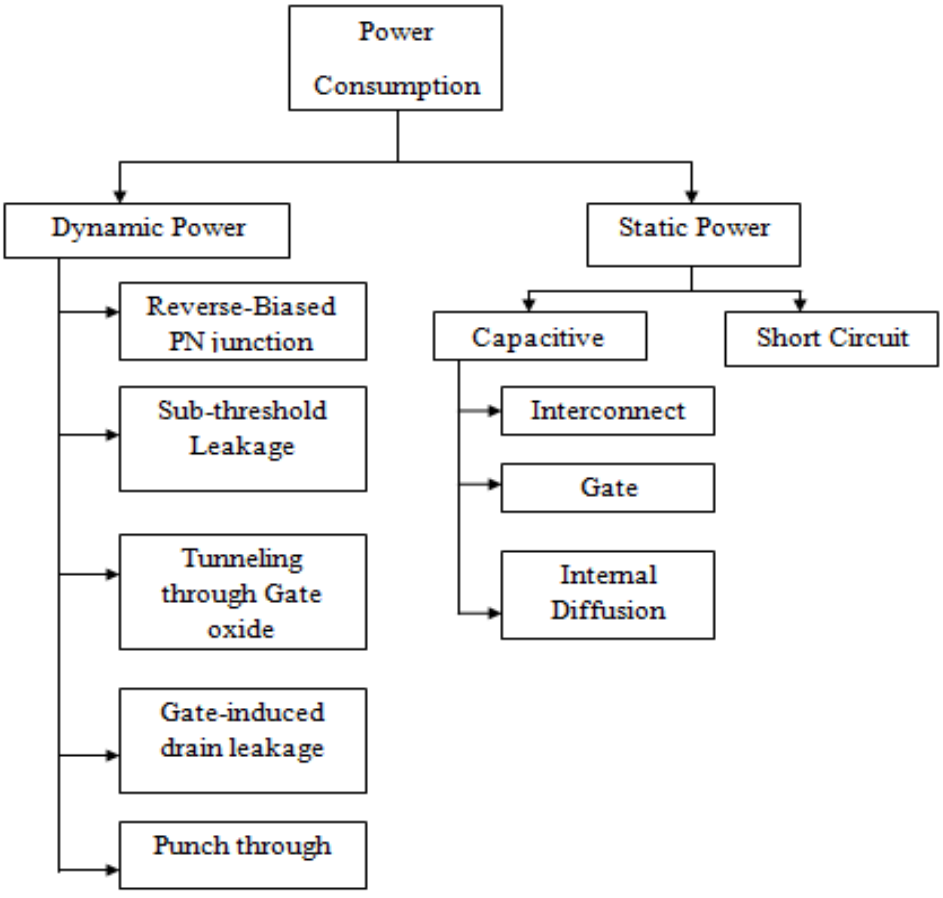

Figure 1.2: Overall Power consumption Flow Chart

The dynamic power consumption has been the main power consumption in integrated circuit design. However, in today advanced technology, the static power consumption tend to be an important factor for the total power consumption. As the matter of fact, in International Technology Roadmap for Semiconductor (ITRS) predicted that the static power will control the power consumption below the 65 nm CMOS technology (ITRS, 2005).

In order to reduce the total power consumption, the techniques should be applied at all abstraction levels which are process technology, system, algorithm, architecture as well as logic and device. The techniques are discussed as follows for all abstraction level as follows:

I. Process technology

Supply voltage and threshold voltage has reduced due to technology process being scaled down. One of most effective way of decreasing the power consumption is by reducing the power supply of integrated circuit. However, this technique may increases the delay in circuit. Gate gating is one of the power reduction techniques at gate level.

II. Logic and circuit level

Power consumption at logic and circuit level can be reduced by minimizing the transistor count. Moreover, power consumption can be reduced by decreasing the switching activity of the transistor by using logic optimization technique. Low power supply voltage, multi threshold voltage (V_{TH}) and low threshold voltage (V_{TH}) can apply to reduce the power consumption.

III. Architecture level

Parallelism and pipelining or the combination of both technique can be used to reduced the overall power consumption at this level. The most effective power management techniques that can be used to reduce the power consumption are by shutting down block that are not used.

IV. Algorithmic Level

The number of operations can be optimized to reduce the power consumption at this level. Hardware's are decreased by optimizing the number of operation and a good coding can reduce the switching activity which delivers better power consumption.

V. System Level

Integrating analog peripheral and off-chip memories at the system level can reduced the power consumption. Low frequency clock or phase locked loop for higher frequency for internal clock can decreases the power consumption.

To reduce the static and dynamic power consumption, there are many techniques have been developed at logic and circuit level. The most famous techniques that have been applied to reduced power consumption are clock gating and multi threshold voltage. Clock gating is a method to minimize the switching activity as much as possible where the clock is disabling from the device during idle state. Clock gating techniques are mainly to reduce the dynamic power of the circuit (Kirti and Surendra Waghmare, 2011).

Meanwhile, in multi-threshold voltage technique, the high threshold voltage is used instead of low threshold voltage in order to decrease the leakage current. Nowadays, the CMOS technology is keeping scaling down but increased in leakage current is noticed as the channel length have been become shorter. Thus, more advanced techniques have been developed such as power gating and multi- voltage to overcome the static power issue. Different voltage levels are used for different block depending on the functionality of the areas in multi voltage technique.

In power gating technique, the supply voltage is not supplied to the unused area. Other techniques that can reduce the power consumption are sleep and stacked transistor (J.C.

Park et al., 2004). On the other hand, super cut-off CMOS technique has been introduced as one of the most efficient way of reducing leakage for low power and high performance circuit (Hiroshi Kawaguchi et al., 2000) .Furthermore, threshold voltage can also reduced by using body biasing technique. Other techniques that contribute to low power consumption are sub-threshold, bulk driven MOSFET, floating gate MOSFET and level shifter approach that are used to decrease the static power consumption (Yaacoub Ibrahim ,2013).

1.2 Problem Statement

In today advanced technology, consumer are expecting long life battery life in all their portable electronic devices. This is because power source are not easily available everywhere as the portable electronic devices are carried from one place to another.

Power reduction techniques are mostly applied in the digital circuit instead of analog circuit. This is because analog circuit are very complicated and complex. One of the rapidly growing building blocks of analogue circuit is flash ADC which tends to be one of most developed ADC to be used in high speed and low power design. In flash ADC, the number of comparator increased exponentially as the resolution of the ADC is increases. Thus, low power and high speed comparator accuracy is important to deliver a good ADC performance (Panchal S D et al., 2012).As the CMOS technology is shrinking, power consumption has been major concern. Besides that, high power consumption leads to high cost of packaging and cooling in order to minimize the heat dissipation from the circuit. This is because there have been few power reduction techniques on analog circuit has been studied so far.

In addition, power consumption also has been a critical issue as the size of transistor is scaling down. Thus, this thesis is mainly concentrate on the designing and simulating a low power comparator without compromising the speed of the comparator.

1.3 Objective of Research

Below are the objectives of this research

I. To study and investigate the suitable power reduction techniques for comparator

II. To design and simulate a comparator with chosen low power techniques

III. To design a comparator that gives the best performance in low power

1.4 Scope of Research

The main focus of this research is on designing low power comparator at circuit level. The schematic is designed using Virtuoso Schematic Editor from Cadence and the layout is designed using Virtuoso Schematic from Cadence. Silterra 0.13 um CMOS technology is used to design the comparator circuit.

1.5 Research Contribution

The following are the contributions of this study

I. Provide a study of low power reduction methods at circuit level such as MTSCStack, dual threshold transistor stacking (DTTS), body biasing and others.

II. Proposed design of low power comparator using a combination of MTSCStack and DTTS techniques.

1.6 Thesis Overview

Chapter 2 provides the literature review of power consumption. The benefits and disadvantages of each techniques of power reduction are described in this chapter. In addition, the various kind of comparator performance are discussed

Chapter 3 describes the methodology used in this study. The schematic and circuit of the conventional comparator, comparator with power reduction techniques and the proposed comparator are also discussed in this chapter. This chapter also explains the layout of the proposed comparator.

Chapter 4 presents the result of this research and included the analysis between comparators that have been studied. Pre layout and post layout simulation are included and result of different type of comparator are discussed.