DESIGN OF FPGA ADDRESS REGISTER IN 28NM PROCESS TECHNOLOGY BASED ON STANDARD CELL BASED APPROACH

By

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List of Abbreviation and Nomenclature

Abbreviation	Meaning
AND	AND gate
AR	Address Register
ASIC	Application Specific Integrated Circuit
CAD	Computer Aided Design
CTS	Clock Tree Synthesis
DRC	Design Rules Check
dsp	Digital signal processor
ECO	Engineering Change Order
EDA	Electronic Design Automation
EM	Electromigration
ESD	Electro Static Discharge
FF	Fast fast corner
FPGA	Field Programmable Gate Array
IC	Integrated Circuit
I/O	Input/Output
IP	Intellectual Property
LEC	Logic Equivalency Check
LVS	Layout versus Schematics
mV	Mili Volt
M1	Metal 1 layer
M3	Meta 3 layer
M5	Metal 5 layer

M6	Metal 6 layer
MHz	Mega Hertz
nm	Nano meter
PTPX	PrimeTime PX
PVT	Process, Voltage, Temperature
QA	Quality Assurance
RCXT	RC extration
SDC	Synopsys Design Constraints
SI	Signal Integrity
SPICE	Simulation Program with Integrated Circuit Emphasis
SS	Slow slow corner
STA	Static Timing Analysis
TAT	Turn Around Time
TT	Typical corner
um	Micron meter
VLSI	Very Large Scale Integration
vccl_pr	Power netname
vss_pr	Ground netname
Vth	Voltage Threshold
XOR	Exclusive OR gate

Rekabentuk FPGA Address Register dalam Teknologi Proses 28nm

berasaskan Pendekatan Sel Piawai

Abstrak

Secara tradisinya, “Field Programmable Gate Array” (FPGA) “Address Register” (AR) direka menggunakan “full custom”. Dengan keadaan geometri yang mengecut pada awal proses nod, maka keperluan untuk menimbang semula pendekatan reka bentuk yang digunakan untuk mereka bentuk FPGA AR diperlukan kerana kitaran reka bentuk meningkat dan merumitkan yang membawa kepada masa lelaran lanjut ke atas penutupan masa blok. Terdapat pelbagai jenis cabaran yang terpaksa dihadapi dalam proses 28nm dan seterusnya sekiranya pendekatan “full custom” masih digunakan untuk merekabentuk FPGA AR. Oleh itu, pendekatan berasaskan sel piawai digunakan untuk reka bentuk FPGA AR. Kitaran reka bentuk FPGA AR dapat dikurangkan dari bulan ke minggu dengan penggunaan kaedah sel piawai. Selain itu, penutupan masa dapat mengawal senario masa yang lebih. Keputusan menunjukkan bahawa FPGA AR menggunakan pendekatan berasaskan sel piawai adalah memenuhi spesifikasi reka bentuk yang diberikan. Di samping itu, jatuhan IR untuk kuasa dan bumi adalah di bawah 2mV, frekuensi adalah 330 MHz dan keluasan kawasan adalah 0.975mm2. Sebagai kesimpulan, pendekatan berasaskan sel piawai memberi pereka lebih banyak masa untuk menyelesaikan isu yang berkaitan dengan rekabentuk. Di samping itu, perubahan yang disebabkan oleh proses, voltan dan suhu dapat diperbaiki melalui kaedah pelbagai sudut dan senario ke atas FPGA AR.

Design of FPGA Address Register in 28nm Process Technology

Based on Standard Cell Based Approach

Abstract

Traditionally, Field Programmable Gate Array (FPGA) Address Register (AR) is designed using full custom approach. With geometries shrink on advance process node, there is a need to reconsider the design approach used to design FPGA AR because of increased design cycle and complexity that lead to more iteration time on closing block timing. Significant design effort and challenges are required in 28nm and beyond when using full custom approach. Therefore, standard cell based approach is used to design the FPGA AR. Design cycle of FPGA AR is reduced from months to weeks with the automated standard cell based approach. Besides that, timing closure is able to cover more timing scenarios. Results show that FPGA AR using standard cell based approach is meeting the given design specification. IR drop on both power and ground is achieving less than 2mV per rail, frequency of 330MHz is obtained on FPGA AR and area size is 0.975mm2. In summary, standard cell based approach gives designer more time to focus on resolving design issues, and close the design in more timing scenarios which cover more design corners to improve variation due to process, voltage and temperature.

CHAPTER 1

INTRODUCTION

1.1 Background

One of the classical predictions in Very Large Scale Integration (VLSI) transistor counts and densities is known as Moore's Law. The law is named after Gordon Moore, one of the cofounders of the Intel Corporation, who described the trend in 1965 (Gordon Moore, 1998). He projected that the number of transistors on integrated circuits (IC) doubles approximately every two years. Although there have been variations due to technological problem or economic slowdowns, Moore's Law has proved amazingly close to actual trends.

A transistor is a basic electronic switch the chips. It is invented at Bell Labs in 1947. Every chips need a certain numbers of transistor, the more there are, the more chips can do. With the latest generation technology of 28nm, more transistors are fabricated in a chip compare to previous generation technology of 40nm with same die size. This is because the transistor size geometries shrink with every advanced generation technology. Most of semiconductor devices and chips are created with silicon. Wafer fabrication processes provide repeated different layer on material by stacked up and design pattern was imposed to the layer to form interconnection for the semiconductor devices.

VLSI can be categorized into two main stream such as Application Specific Integrated Cicruit (ASIC) and Field Programmable Gate Array (FPGA). ASIC is IC customized for a specific function. For example, digital voice recoder is an ASIC. Advantages of ASIC is providing lower unit costs for very high volume design, full custom capability and smaller form factor since the device is manufactured to design specs. Besides that, ASIC provide higher performance and higher logic density. Disadvantages of ASIC on design errors are requiring expensive and time-consuming ASIC re-spin.

FPGA is an integrated circuit designed to be configured by a customer or a designer after manufacturing. It is a programmable chip for multi-purpose function. An ASIC development cost is raising which make FPGA attractive and advantageous alternative solution. FPGA provides shorter time to market and software programming flexibility for customer compare to ASIC. For smaller design and/or lower production volumes, FPGAs may be more cost effective compare to ASIC design even in production.

FPGA contains programmable logic components called “logic blocks”, and a hierarchy of reconfigurable interconnects that allow the blocks to be connected together. Logic blocks can be configured to perform complex combinational functions, or merely simple logic gates like AND and XOR. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory. Figure 1-1 shows the layout of a FPGA. In this figure, FPGA is divided into sections such as I/O interface, Core and Analog.

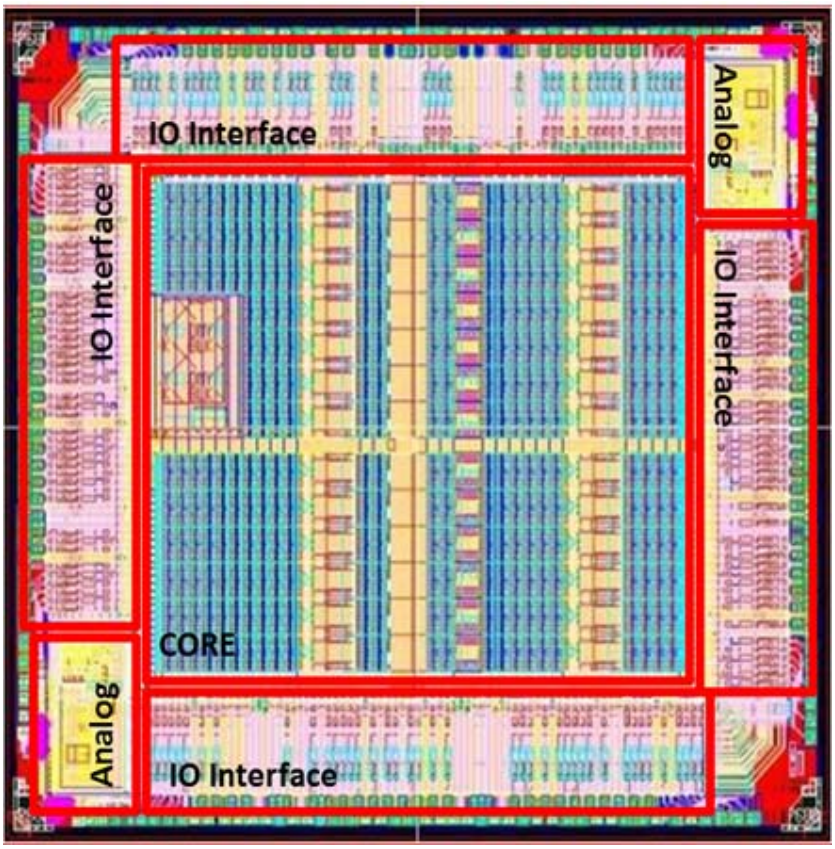

Figure 1-1 The layout of a FPGA

Figure 1-2 shows location of a FPGA Address Register (AR) in the FPGA Core section. It is being placed at the center of Core FPGA. FPGA AR acted as address mapping for memory cell in FPGA. Size of an address register is determined by the configuration memory cells count in horizontal Mx-axis as shown in Figure 1-2 (Yabin W. et.al 2007).

The configuration memory of Figure 1-2 is an 8-bit by 8-bit array that includes 64 configuration memory cells. In general, each of the configuration memory cells is identified by a reference number character Mx-y, where x and y correspond to the row and column of the configuration memory cells. The array of Figure 1-2 is much smaller than is typically used in a commercial embodiment which has the order of 20,000 to one million memory cells. Since the configuration bitstream is so big, the configuration is broken up into frames. Frames are groups of configuration data spanning entire devices vertically that are readback together.

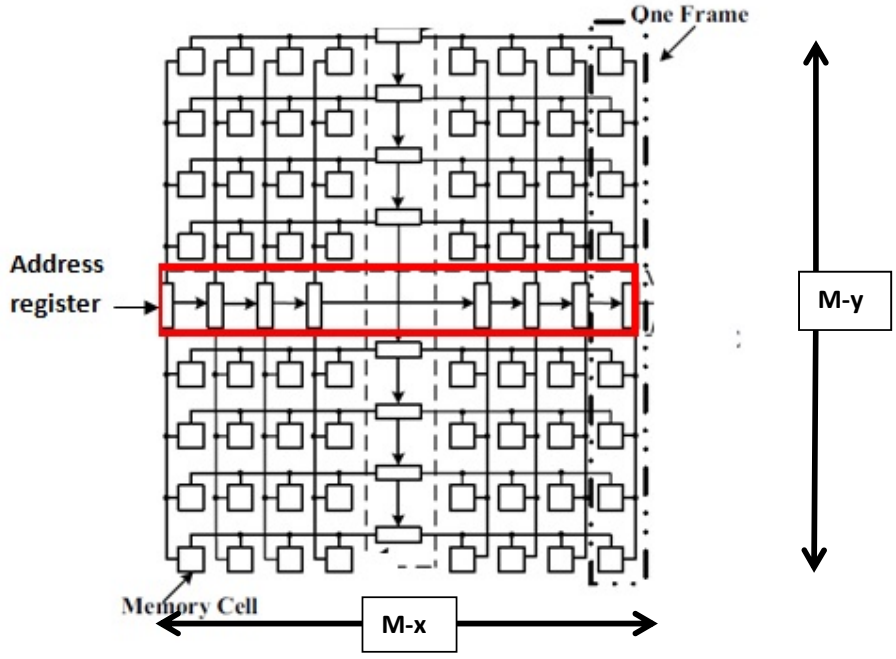

Figure 1-2 FPGA AR in the FPGA Core section, Yabin W. et.al (2007)

Conventionally, FPGA address register is designed based on full custom design technique. When the process technology node becomes smaller, and FPGA configuration memory cells grow up to few million memory cells, caused the block size of FPGA address register scale linearly. It is more challenging to design a FPGA

AR based on full custom approach. We cannot afford to have longer design cycle on turn-around-time (TAT). This will impact the time to market. Besides that, processes of closing FPGA AR block timing takes longer iteration in full custom approach because of the number of memory cells are increased. Upfront planning for full custom like power grid, routing track, ports counts, floorplan size, power consumption and timing is planned in details to ensure no rework process causing major schedule delay.

Ferrrandi, F. et.al. 2007 have demonstrated that interconnection costs have to be taken into account since area of multiplexers and interconnection elements has by far outweighed area of functional units and registers. This is especially true for FPGA (field programmable gate-array) designs because a larger amount of transistors have to be provided in the wiring channels and logic blocks or memory cells to provide programmability for signal transmission. Interconnection allocation should be taken into account by each methodology that tries to minimize time and resource of FPGA address register design.

The impact of interconnect on FPGA address register mostly contributed from the gate delay and also the delay of long nets. The gate delay depends mostly on the output capacitance it drives, of which the net capacitance becomes the largest contributor. The delay of long nets, which depends on their capacitance and resistance, becomes larger than gate delays. Moreover, coupling capacitance is become more dominant over inter-layer capacitance with every new process technology. This is because the nets are getting much closer to each other and the

wire aspect ratio of height to width is increasing. Coudert, O. claimed that in 2002, the coupling capacitance is more than four times larger than the inter-layer capacitance, and the ratio is projected to increase to six by 2010. This means that the capacitance of a net cannot be determined without knowing both its route and that of its neighbors'. The coupling capacitance will lead to routability and noise effect when the process node becomes smaller especially on 28nm onwards. With design rules continue grow in 28nm process technology, routability is an issue that need special attention and checks to ensure physical design in polygon is able to meet the design rules and without violation.

Besides that, signal electromigration (EM) is the metal ions movement occurs which cause violation either a void (open) or a hillock (short), which eventually leads to circuit malfunction. EM decreases the reliability of integrated circuits (ICs). At 28 nm, there are significantly more EM violations on signal interconnects compared to those at 65 and 40 nm. Metal widths are shrinking because of geometry scaling, resulting in thinner interconnects. Interconnect lengths are also increasing to meet the complex device integration demands. A clear indication of this trend can be seen in Figure 1-3 that plots EM violations seen on a sample block across varying technology nodes and clock frequencies (Geetha R., et.al 2013).

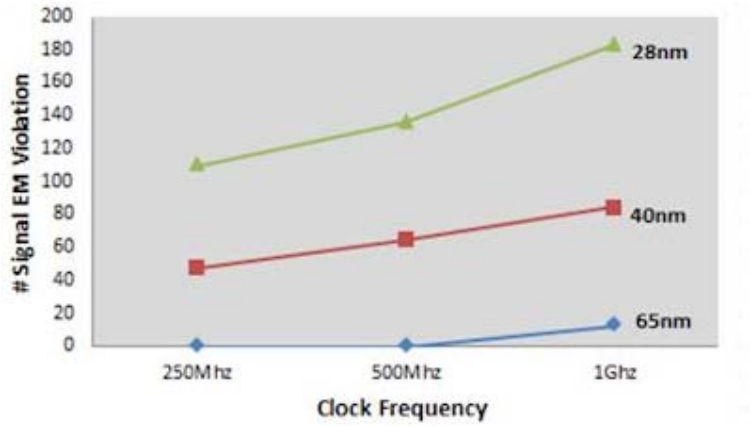

Figure 1-3 Signal EM violation plot using sample block, Geetha R., et.al (2013)

With an increasing number of interconnects exposed to EM effects, fixing techniques must be automatic, accurate, and timing and design-rule check (DRC) aware. Standard cell based approach would be better to use to cope this signal EM in 28nm compare to full custom approach for designed FPGA AR. Full custom approach would be iterative, require user expertise and can adversely affect performance.

1.2 Problem Statements

Fast times to market and reduced design development time are very important for producing a chip. FPGA AR design using full custom approach tends to have longer iteration time and upfront planning. Most of full custom step are customized and manual design by designer. Designer gets to control manually place and route FPGA AR. Although there is an advantage on performance and area being achieved by full custom approach but it will lead to longer design cycle. Normally, the design cycle

takes up to several months it depends on the design complexity. The design development time is expected to be increased exponentially if there is no precaution step taken when upfront planning the design.

There are few possibilities that designer will faces on FPGA AR integration stages: Design Rules Checks (DRC) errors or signal shorts. Besides that, FPGA AR timing convergence is mainly min-max situation of I/O to flop paths especially for the flops that sit far away from the clock port. These paths have stringent hold requirement set in timing constraints. To meet the hold requirement, the data path delay has to be equal or longer than the clock path delay. However, the data and clock path delay skew difference is very huge across process, voltages, temperature (PVT), mainly due to clock derate charged for hold and the noise effect. Therefore, for this reason, in 28nm, standard cell based approach is consider to design a FPGA AR, in order to achieve fast turn-around-time and signoff the block timing in multiple timing scenarios.

1.3 Research Objectives

The objectives of the research are

i. To minimize FPGA AR design cycle and provide fast turn-around time (TAT).
ii. To design and implement FPGA Address Register (AR) in 28nm based on standard cell based approach.

1.4 Scopes

Design FPGA AR using standard cell based approach start with given gate-level netlist, design constraints and physical constraints. The scopes on this research are to cover FPGA AR physical design (standard cell) flow from floorplan, place and route, static timing analysis, power analysis, functional verification and physical verification.

1.5 Research Contribution

The contributions from this research are:-

1. FPGA AR which was designed in 28nm process technology based on standard cell based approach.
2. Reduction of Turn Around Time in the designing of FPGA AR.
3. Designer has more time to focus on critical design issue.
4. Standard cell based approach provide the flexibility to FPGA AR to migrate between technology generation and different processes.

1.6 Thesis Organization

This thesis is organized into five chapters. The rest of the thesis is organized as follows.

Chapter 2 describes the current strategy to design FPGA AR. The chapter begins with the introduction of FPGA AR and design strategy differences between full custom approach and standard cell based approach.

Chapter 3 outlines the design methodology use for FPGA AR based on standard cell based approach. Overview of the standard cell based approach and each step in the methodology will be discussed in detail with examples.

Chapter 4 shows results of designed FPGA AR using standard cell based approach in terms of design times, area, power and timing. Briefly compares the results to full custom approach. Each steps of the result is shown to better capture the outcomes.

The final chapter, Chapter 5 consists of conclusion and future works. Conclusion will cover the key highlights of the findings and contributions of the research while some recommendation and ideas for future works are proposed.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

The objectives for this project are to reduce the design cycle time using standard cell based approach and produce a layout of FPGA AR in 28nm based on standard cell design flow where the given design specification is fulfilled. In order to achieve these objectives, this chapter will elaborate on the literature studies done.

First and foremost, an overview of FPGA AR will be described. Continue with the differences between full custom approach and standard cell based approach to build FPGA AR. Conclude that, in this project will be using standard cell based approach to implement FPGA AR.

2.2 FPGA AR

FPGA AR consists of a combinational of a series shift registers and counters. Address Register is one of the core blocks for FPGA system. The function of FPGA AR is to switch on and off of each memory cell in the core of FPGA based on the inputs pattern.

Figure 2-1 shows an overview of a FPGA address register block. This block contains macro IP (Intellectual Property), combinational circuits and sequential elements. Block size of address register for this project is given as approximately 5000um by 195um. Macro IP is implementing by using full custom design flow. There are various types of macro IP used in an address register.

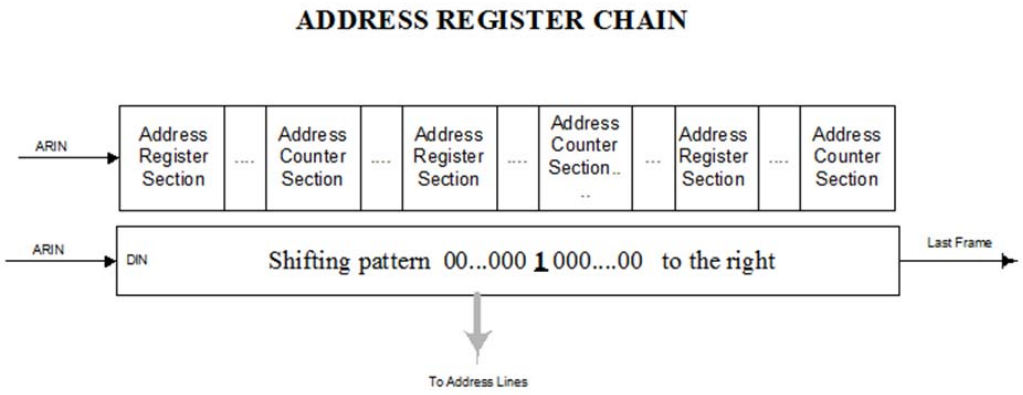

Figure 2-1 Overview of an Address Register block

For standard cell based approach designed for 28nm FPGA Address Register block has planned the floorplan to be three portions in physical design such as top, middle and bottom. Top and bottom are dedicated placement for macro IP and middle portion consist of standard-cell placement, control signal and clock system design. Each macro IP is being placed in column based floorplan.

2.3 Full custom versus Standard cell based approach

IC designers have two options to implement an integrated digital circuit:

- Standard cell based approach

  Design using standard cells. Standard cells come from library provider. There are many different choices for cell size, delay and leakage power in standard cells. Many EDA tools have automated this flow. Provides shorter design time compare to full custom approach.

- Full custom approach

  Design all by designer (hand-crafted). This gives designer flexibility to customize their block and can achieve higher performance.

Generally, the following criteria are used to choose which type of implementation is the best method to design a digital integrated circuit. (Eleyan, N.N et.al, 2009)

- Design complexity –Depends on amount of cells and gates. Need special handling like manual place and route certain module.

- Timing requirements –High speed design or critical timing to deal with.

- Area requirements -Tight area budget is being given to work on. Need special handling on certain area.

- Power requirements -Power consumption on low power method.

- Project Schedule and Resources -Consider design cycle and human resource to work on specific block as highest priority.

Normally, designer is in dilemma to get all the above requirements in the design plate as higher priority. In actual case, there are some tradeoffs in order to achieve designer goals. As long as the tradeoff is within the design specification and not too far off, designer will accept the design result. Typically, designer will choose to use standard cell based approach when project schedule and resources is the highest priority and design complexity is hard to solve in manpower which need to rely on electronic design automation (EDA) tools. He/she will choose to use full custom approach when the design is needed to achieve a specific performance speed and area requirement is a highest concern.

2.3.1 Full custom flow

In full custom design, designer manually place and route all circuits which gives the possibility to use special circuit styles and arbitrary sizing of the transistors. Figure 2-2 shows full custom design flow chart (Lyons, E. et.al.,2009). Full custom design is mainly used in critical parts. It has long iteration design time and need upfront planning than in standard cell based approach. Designer has to plan every single detail of the block, updating the schematics and optimize the new changes. After that, he/she has to draw every polygon of the layout before can have fully routed design.

Follow by re-extracting the parasitics and re-analyzing timing, noise and power. Finally, the designer has to also generate updated timing and physical abstracts.

The above process can take days or weeks depending on the design size and the nature of the design change. With standard cell based approach most of the steps are well automated. The process takes few hours instead of days or weeks. With this faster design iteration time the designer can now afford to experiment more with different placement and routing scenarios.

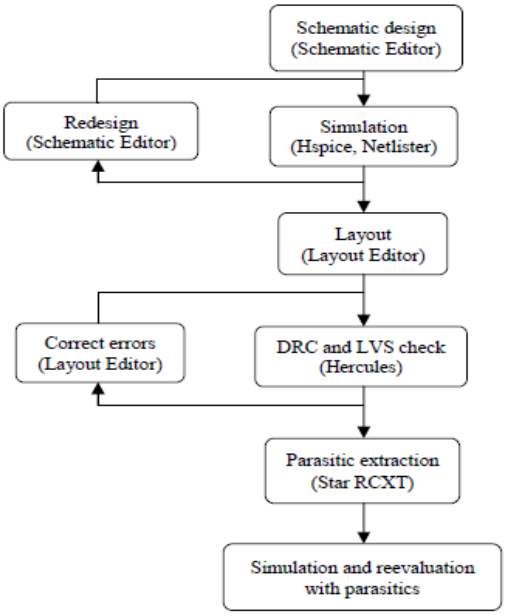

Figure 2-2 Full Custom design flow chart, Lyons, E. et.al. (2009)

2.3.2 Design flow for Standard cell based approach

In standard cell design, basic gates or building blocks, e.g multiplexers, full adders, flip-flops, and basic logic functions, are provided by a chip vendor. Design can now