MICROPROCESSOR SOLDER BUMP BRIDGING DEFECTS SCREENING STRATEGY IN MANUFACTURING TEST FLOW

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LIST OF SYMBOLS

V_{cc}	-	Input voltage source
$V_{O(SENSE)}$	-	Current sense circuitry output voltage
$V_{O(COMPARATOR)}$	-	Comparator output voltage
V_{LIMIT}	-	Current limiter in term of voltage
V_S	-	Current sense input voltage
V_{REF}	-	Reference Voltage
R_G	-	MOSFET Gate Resistance
R_{SENSE}	-	Sense Resistor
I_{SENSE}	-	Sense Current
AU	-	Arbitrary unit
A_V	-	Amplifier Gain

LIST OF ABBREVIATIONS

SBB	-	Solder bump bridging
DPM	-	Defect per millions
HVM	-	High volume manufacturing
BI	-	Burn In
BIB	-	Burn In Board
PV	-	Platform Validation
IO	-	Input and Output
IC	-	Integrated Circuit
IP	-	Intellectual Property
IM	-	Infant Mortality
BGA	-	Ball Grid Array
LGA	-	Land Grid Array
SOC	-	System on chip
MCP	-	Multi-chip Package
CPU	-	Central Processing Unit
PCH	-	Platform Control Hub
PCB	-	Printed circuit board
DUT	-	Device under test
DAC	-	Digital Analogue Converter
BOM	-	Build of Materials
TTL	-	Transistor-transistor logic
PBIC	-	Post Burn In Check
SIP	-	System in Package
SoC	-	System on chip
MCP	-	Multi-chip Package
VLSI	-	Very Large Scale Integration

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MICROPROCESSOR SOLDER BUMP BRIDGING DEFECTS SCREENING STRATEGY IN MANUFACTURING TEST FLOW

ABSTRACT

Solder bump bridging (SBB) is a type microprocessor packaging defects in Flip-Chip or C4 interconnection layer. The presence of micro conductive contaminate particle in die-package layer which causes bridging between two or more adjacent solder bump. These contaminate particles are mainly comes from solder bump fraction result from deficient packaging process. Today semiconductor manufacturing test flow is still imperfect to completely screen or detect the SBB defect. As bounce back, the test holes contributes to the defect per million (DPM) of the product. In this research, the test holes of SBB defect in High Volume Manufacturing (HVM) will be defined. Meanwhile, SBB defect characterization will be studied where the electrical behavioural of baby bumps is explained. In the final part of the study, an effective SBB screening test at Burn In is developed to minimizing test holes. From the research finding, un-bridging of SBB occurs at extreme high current of 4.5 A where the baby bump burnt and partial unbridged. This unbridged state are unstable and lacking in term of reliability. However, the SBB un-bridging only impacted on Type B SBB defect where baby bump bridging power bump with ground bump. Lastly, the SBB screening test at Burn In stage is developed as part of this research. In conclusion, the proposed test has the potential in minimizing HVM SBB defect test holes by improving SBB defect fault coverage.

STRATEGI PENYARINGAN KECACATAN PENYAMBUNGAN BENJOLAN PATERI MIKROPEMSES DALAM ALIRAN UJIAN PEMBUATAN

ABSTRAK

Penyambungan Benjolan Pateri (SBB) ialah sejenis kecacatan pemasangan mikropemproses dalam lapisan sambungan Flip-Chip atau dikenali sebagai C4. Kemunculan zarah konduktif bersaiz mikro dalam lapisan C4 menyebabkan penyambungan antara dua atau lebih benjolan pateri bersebelahan. Kehadiran zarah pengkontaminasi konduktif bersaiz mikro ini berasal daripada pecahan bonggol pateri dalam proses pemasangan yang kurang berkesan. Sehingga hari ini, ujian pembuatan semikonduktor masih belum sempurna dalam pengesanan kecacatan SBB. Akibatnya, lubang dalam ujian kecacatan ini menyumbang kepada kecacatan per juta (DPM) produk. Dalam kajian ini, lubang ujian kecacatan SBB dalam Pembuatan Berjumlah Tinggi (HVM) akan ditentukan. Selain daripada itu, kecacatan SBB akan diperincikan dan perilaku elektriknya akan dijelaskan. Dalam bahagian akhir kajian, ujian saringan SBB yang berkesan di Proses Memarak Dalam (BI) dikembangkan untuk meminimumkan lubang ujian. Dari hasil penyelidikan, SBB terbuka berlaku pada arus tinggi 4.5 A di mana benjolan pateri bayi terbakar dan penyambungan pateri benjolan terbuka. Keadaan penyambungan pateri benjolan terbuka ini adalah tidak stabil dan kekurangan dalam kebolehpercayaan. Bagaimanapun, SBB penyambungan pateri benjolan terbuka hanya memberi kesan kepada kecacatan Jenis B SBB di mana benjolan bayi merapatkan pin kuasa dengan pin asas. Terakhirnya, ujian SBB dalam BI dihasilkan sebagai sebahagian daripada kajian ini. Sebagai kesimpulan, ujian yang dicadangkan ini berpotensi dalam meminimumkan lubang ujian kecacatan SBB dalm HVM dengan meningkatkan liputan kesalahan kecacatan SBB.

CHAPTER 1

INTRODUCTION

1.1 Introduction

Transistors are the fundamental building blocks of computers, switching between the binary 1 and 0 that makes up the language of computers. As the silicon transistors that make up computer circuits shrink, engineers are able to fit exponentially more onto every processor, making computers cheaper and more powerful. According to the latest International Technology Roadmap for Semiconductors (ITRS), a joint report from chip giants including Intel and Samsung, by 2021 transistors will shrink to a point at which it is no longer economically viable to make them smaller [1].

As in 2016, the transistors size shrinking toward 10nm or smaller lithography process, the manufacturing test becomes more challenging. Moving toward smaller lithography process, the yield rated issue arise, more advance test is required for defect screening [2]. Product manufacturing testing in semiconductor sector is one of the most expensive and time consuming part. Testing does not make the product more useful, or faster, but it does improve the product quality and reliability of the product.

Solder bump bridging (SBB) is a type of silicon defect or reject chips in manufacturing. The number of these defect contributed some percentages in total yield lost. Solder bump bridging is an electric short-circuit between Flip Chip bumps within area in presence of contaminate substances such as conductive material like

solder leftover. The conductive particles within die-package substrate layer causes bridging between two or more adjacent solder bump. These contaminate particles are mainly comes from solder bump fraction result from deficient die and substrate interconnection process. These SBB state are unstable, it switches between state of bridging and not bridging. The reason of the unstable state is caused by external electric potential excitation. This instability state caused a fault pass in the manufacturing test.

In this project, the implement of SBB screening strategy in Burn-In test of manufacturing flow may help improve manufacturing test deficient in SBB screening. This SBB defect screening strategy enable the microprocessor with SBB defect able to be detected and screened out during Burn-In test. By implementing this new SBB screening strategy, the defect per millions (DPM) of the microprocessor will be improved.

1.2 Problem Statement

Today semiconductor high volume manufacturing (HVM) test flow is still imperfect to completely screen or reject the defect in silicon production. The goals of manufacturing test are to screen out manufacturing defects, Bin for speed, and verify that devices meet the published Direct Current (DC), Alternating Current (AC), and frequency specifications. As bounce back of the deficient in achieving ideal fault coverage in HVM test, the defect chips contributed a number in the defect per million (DPM). DPM of the delivered product reflect as the quality and reliability of fabrication.

In legacy HVM test flow, the silicon will go through couple test before and after assembly. Before assembly, defects dies will be rejected during Sort test, these chips will not proceed for assembly. After assembly, Burn-In (BI), Performance Test and Platform Validation (PV) test were conducted. In Performance test, functional test sequence is a sequence of primary input vectors that is applied to a synchronous sequential circuit under its functional operation conditions. Functional test sequences can be generated by gate-level sequential test generation procedures [3-5]. The HVM test plan are product dependent, different product tends have a different test plan based on product DPM budget, product family, product power, market segment, usage condition, fabrication process and etc.

Solder Bump Bridging (SBB) is a type of physical defect due to imperfection of packaging process in chip manufacturing. The presence of baby bump in Flip Chip interconnection layer is the main trigger of SBB defects. SBB induces short-circuits within group of solder ball in adjacent. These Baby Bumps are mainly comes from solder bump fraction result from deficient die and substrate interconnection process. This imperfection in packaging process contributes to an extra yield lost and extra DPM.

In the past, the open-short test in Performance Test is able to effectively screen the SBB defect flawlessly. The SBB screening problem arise when Burn-In is the first test in product HVM test plan. There are lack of Burn-In tester which are capable to perform open-short test due to tester capability. Finding from failure analysis shows the Baby Bumps perish after Burn-In. Subsequently, the defects units appear good and passes the open-short test in Performance Test. These SBB unbridged DUT are not stable and intermittent.

Ultrasonic scan and X-Ray technique would have a better accuracy in package defects screen. However, these techniques do not fit in manufacturing factory need in term of production speed and manufacturing testing solution.

1.3 Objective

The main objectives of this research study are as follow:

i. To investigate on the efficiency of manufacturing test on SBB defects screening.
ii. To investigate the SBB defects units behaviour toward electric power.
iii. To develop an efficient SBB defects type B screening solution in manufacturing test.

1.4 Scope of research study

The project aims to develop an effective test solution to screen Solder Bump Bridging (SBB) defect at Burn-In (BI) stages of manufacturing flow. By implementing the developed SBB BI test solution, the defects per millions (DPM) are expected to be reduce or meeting the target DPM.

Basically the Integrated Circuit (IC) pinout are made up of 3 main groups, which is power input pin, VSS pin (or ground pin), and signal pin. Signal pins consists of digital IO (Input/output pin) and analogue output pin. In this project, the work will only be done on screen power pin neighbouring SBB. This limitation is due to the Burn in board (BIB) signal routing space and component placement constraints.

In order to develop the project, three main parts are considered. The first part of the project is the study of the SBB defects conditions and behavioural. The study is mainly on the factors of the SBB state instability. At the end of first part, SBB instability against electric sensitivity relationship are expected to be well characterized.

The second part of the project consists of developing the BI board (BIB) which are able to support the SBB screening test. During bridging or electric short-circuit, the input pin are tend to draw a tremendously higher current. Current sense circuitry will be design and implement on BIB.

The final part of the project is SBB BI test solution validation. In this stage, the developed test solution will be run with high volume for test qualification and stability study

1.5 Thesis Outline

This thesis on Solder Bump Bridging (SBB) defects screening test implementation study are presented by chapter. The SBB defects screening test development at Burn-In platform will fairly summarise in following chapters.

In Chapter 2, the focal point of the literature review is on upbringing of Solder Bump Bridging defects definition. In addition, correlation of high volume manufacturing (HVM) test and defects per millions (DPM) modelling is descripted. The Burn-In goals and Burn-In tester specification are summarized in detail.

In Chapter 3, the research methodology of development of the effective SBB defects screening test in Burn-In are precisely construe. Nevertheless, the systemic

description on test strategy in both the software and hardware design and development for the effective test solution.

In Chapter 4, the findings of study on baby bump reaction toward electricity and thermal is characterize based on the experiment result. Meanwhile, the final design of test board schematic design is discussed. Effectiveness of the Solder Bump Bridging defects screening test is qualified and validated though round stability of cycle run result are summarize as last part of this chapter.

In Chapter 5, the conclusion of this project is mentioned. In addition, limitations and recommendations of the project are mentioned for possible future work and further improvements.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

This chapter mentions about the definition of Solder Bump Bridging (SBB) and background of silicon manufacturing test process which are currently implemented in most of semiconductor industry fabrication plant. Besides that, definition and purpose of Burn-In test are deliberated. Furthermore, the silicon structure in terms of die to substrate interconnection and silicon packaging are elaborated.

2.2 Semiconductor Manufacturing Flow

Fabrication processes have been subject to rule checks for a long time. The implementation of rule checks for improved manufacturing. The goals of manufacturing test are to screen out manufacturing defects and verify that devices meet the published specifications [6].

There are many attributes of a good test. A good test passes only good product and fails only bad product, it optimizes yields and screens out defects. From wafer fabrication to product shipping, there multiple test stage in manufacturing flow [7]. Figure 1.1 shows a simplify semiconductor production flow. The test has a short test time, it minimizes product costs and reduces capital equipment needs. The test is comprehensive, it covers all structures in the device under test.

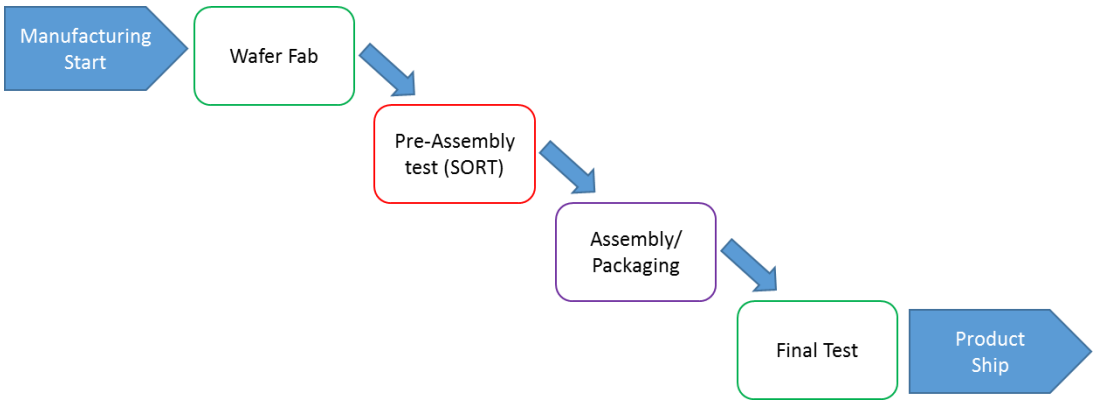

Figure 2.1: A Simplify Semiconductor Production Flow [7].

There are couples of test held in between stages of wafer fabrication, assembly, and customer. Each of the test has its specific purpose and functions in the goal of defect screening. Sort test, Burn In, Performance test and Platform Validation test are four major type of test in microprocessor manufacturing test.

The type of test are as follow:

I. Sort test is the process step immediately following fabrication processing where die are tested while still on a wafer.

II. Burn-in consists of functionally exercising an assembled part at a high temperature and voltage [8]. The primary goal of burn-in is to accelerate particle defects and processing problems to failure.

III. Performance test is several test sockets in the manufacturing flow where packaged units are tested with a test program that validate the electrical specifications of the product.

IV. Platform validation test is the approach to test chips functionality in actual systems environment which running operating systems and software. Components are mounted to test motherboards and inserted into test computer systems for validation under realistic operating conditions.

In general, fault coverage of specific defects types are dependent to effectiveness of the particular manufacturing test sequences [9].

2.3 Defects per millions (DPM)

Defects per millions (DPM) is a measurement of High Volume Manufacturing (HVM) test performance for specific product. DPM or Defects per millions opportunities (DPMO). Six Sigma (6σ) is a set of techniques and tools for process improvement on the quality of the output by identifying the causes and minimizing variability in process. DPM is six sigma initiative measurement of process performance. It is not equivalent to Part per Millions (PPM) as its definition of opportunity in semiconductor assembly processes [10]. DPM numbers represent the number of units per million that are defective which passed HVM test due to test hole have been shipped to customers. HVM test flow which are considered stable or highly capable, for example 32 nm lithography process HVM test which have low quantity of DPM units produced. Equation 2.1 shows DPM calculation equation. [24]

$$DPM = \frac{Quantity\ of\ distinct\ units\ with\ defects}{Quantity\ of\ distinct\ units\ produced\ or\ tested} \times 1000\ 000 \qquad (2.1)$$

In semiconductor production, the ultimate goal in quality would be the elimination of defects and attaining 100% yield. Perfect yield in Very Large Scale Integration (VLSI) manufacturing is almost unachievable due to the complex

manufacturing step and shrinking of device fabrication process [12]. 10 nm lithography process have lower yield than 14 nm lithography process [13-14] because 14 nm process is less complicated and stable in term of wafer fabrication process. Better test coverage would have a lower DPM, 100 % test coverage is more attainable compared to 100 % yield.

The setting of test requirement is utmost important in achieving the quality goal or DPM goal. The high level concept of DPM modelling consists of relationship between input quality (defect density), test strength, and output quality. Input quality represents the density of defects on silicon. Test strength is HVM test capabilities to screen silicon defect. Lastly, the output quality is representing the DPM numbers. Zero DPM is achievable with ideal inputs (100 % yield) or ideal test (100 % fault coverage). Figure 2.2 illustrated the concept of DPM modelling consists of relationship between input quality, test strength, and output quality.

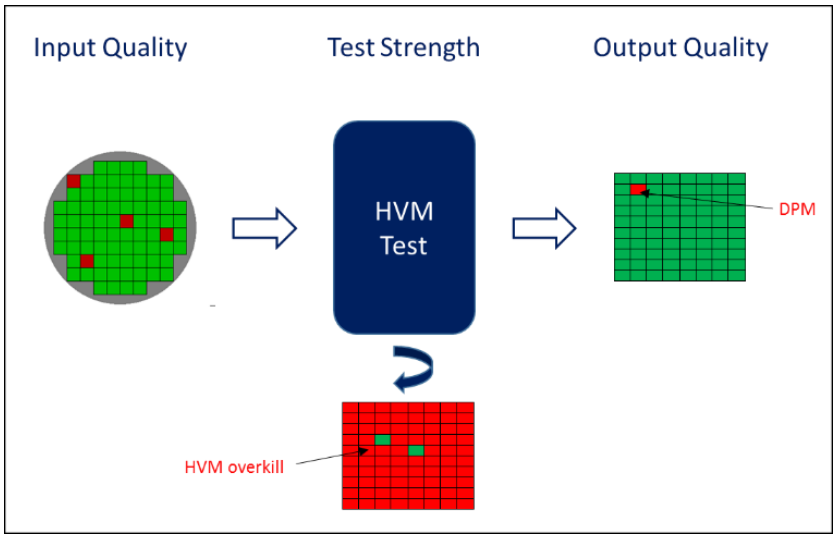

Figure 2.2: DPM modelling

Unfortunately, 100 % test coverage is not even near equivalent to 100 % fault coverage due to systemic defects and process marginality. In semiconductor

manufacturing practical, 100 % test coverage is impractical and the test would be unacceptably expensive and time consuming. The DPM modelling allows industry in defining a cost effective balance HVM test which is achieving customer expected DPM goal [15].

In microprocessor industry, the product market segment is extremely board. The DPM of the products is depends on the market segment requirement and customer expectation.

2.4 Burn-In (BI)

Burn-In (BI) consists of functionally exercising silicon part at high temperature and voltage over a period of time. During Burn-In, the chips is run in a chamber at an elevated temperature and voltage for a specific amount of time. Burn-In time, voltage and temperature are process dependent and determined the rate of chip degradation. The primary goal of Burn-In is to accelerate defect and eliminate defect chip in high volume manufacturing (HVM) flow.

The primary goal of burn-in is to accelerate particle defects like early life failures (Infant Mortality) of silicon product in an effort to assure that outgoing defect per million (DPM) targets are met. BI is able to screen out assembly defects or infant mortality parts by accelerating the aging process. BI gives you clearer picture of chip's defects types hence determining the source of defects and depending on BIT which can clear out part with early failure issues.

Burn-In is part of product qualification process. The product qualification process is to ensure that the product meets quality and reliability requirements [16].

The fallout after Burn-In fallout need to meet the quality and reliability requirement for Infant mortality and quality validation. When numbers of qualification failure is beyond the fallout baseline limit, the cause of failure need to be identified, corrected and qualification recheck.

The Bathtub curve, is a curve presented the signature failure rate over time. It simply states the probability of failure of any manufactured item is highest during the beginning of its life (infant mortality) and towards end of life. However, between these high-probability areas, the rate of failure is relatively low. Figure 2.3 shows Bathtub curve.

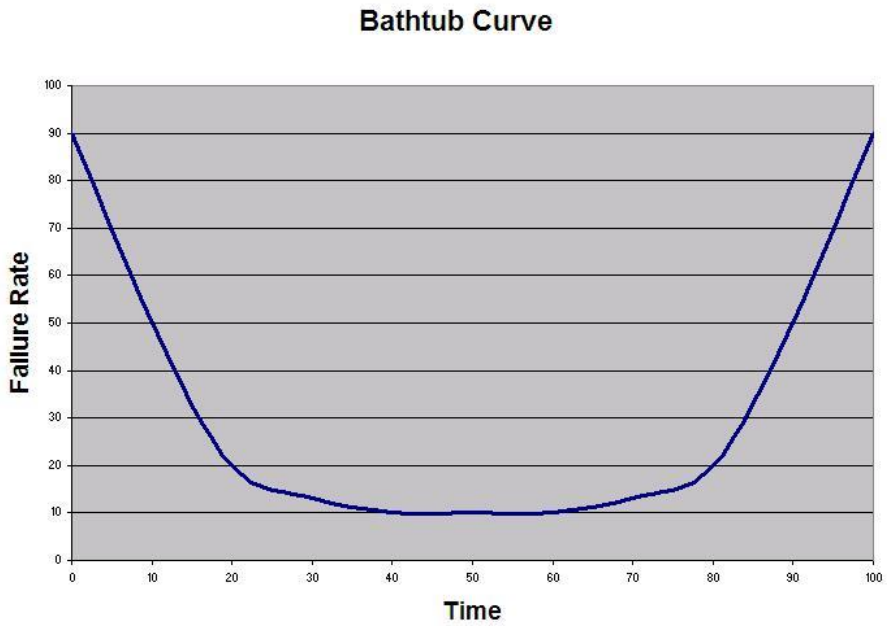

Figure 2.3: Bathtub Curve [12]

In the past, Burn-In test requirements is more relax which only includes the periodically toggling of functional to ensure the DUT (Device Under Test) is still grossly alive. In current Burn-In technologies, the test during Burn-In offers much larger test pattern loading capabilities and improved failure observability through auto signal check pin. However, improvement in Burn-In approaches, post Burn-In check

(PBIC) which provide full coverage functional test is still a requirement and performing to catch Burn-In induced failures.

From HVM test fallout statistics, fabrication process related defects only visible after some level of Burn-In. The PBIC fallout data is used to study the relationship of Burn-In acceleration failure rate to the process baseline. Ideally, the fallout of PBIC only represent random fallout that is expected for respective fabrication process.

2.5 Integrated Circuit (IC) interconnecting and packaging

Integrated Circuit (IC) interconnecting and packaging is the final stage in silicon fabrication, in which IC assembled from wafer to its package. LGA (Land Grid Array) and BGA (Ball Grid Array) packaging is the most favourite type of packaging in microprocessor segment. Similarly, Flip Chip and Wire-Bonding are current most popular die to package interconnect technology in the product segment.

LGA and BGA packaging are commonly used in monolithic and multi-chip package (MCP) product. SoC (system on chip) is an example of monolithic product which only consists of single die/IC in its packaging. SIP (system in package) is an example for MCP product which may have two or more die/IC within single package. Some PC (personal computer) processor is a MCP which made up from a CPU (Central Processing Unit) and PCH (Platform Control Hub) IC. Figure 2.4 below shows an example of MCP processor which consists of two IC dies in one package.

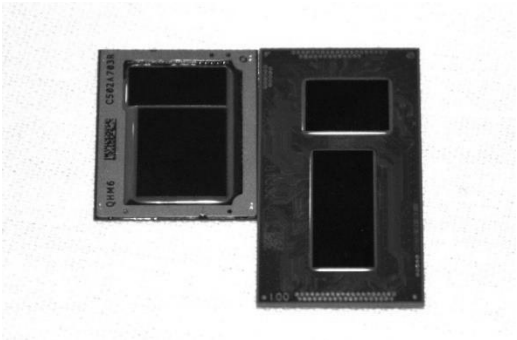

Figure 2.4: Multi-Chip Packaging Processor [18]

2.6 Flip Chip

Flip chip and wire-bonding described method of electrically connecting the semiconductor devices such as Integrated Circuit (IC) dies or microelectromechanical systems (MEMS) to external carrier like package substrate. In practical, both flip chip and wire-bonding may co-exist in same package design.

Flip Chip or abbreviation C4 is a method or process interconnecting IC die to external circuitry with solder bumps that have been deposited onto the chip pads [19]. Figure 2.5 below illustrated wire-bonding and flip chip interconnect. RDL bump or C4 bump connecting IC die to package substrate. The underfill is an electrically-insulating adhesive to provide a stronger mechanical connection and heat bridge to ensure the solder joints are not stressed due to differential heating of the chip and the rest of the system.

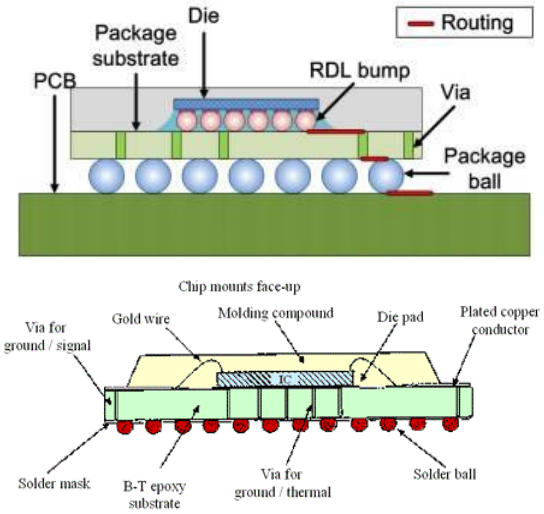

Figure 2.5: Flip chip (top) and wire-bonding (bottom) interconnect [21, 23]

In manufacturing practicability, flip chips have several disadvantages. The wafer bumping yield loss could be due to many variable including process, materials, non-uniformity bump height, low bump shear strength, broken wafers or die, solder bridging, and missing bumps.

2.7 IC Package Defects

There are two primary categories of integrated circuit (IC) package which are lead frame type packages and substrate type packages. Package defects concerns arise come to assembly of ICs on the substrate. Most of packaging defects found within the layer of die attach material or package underfill. The package underfill serves as physically attaches a die to a substrate, heat spreading from a die, and internal stresses reliever.

Delamination of die attach material is a common type of defects shows up in manufacturing. Thermal shock or mismatches in the coefficients of thermal expansion

of materials can also cause delamination. The next common defects is called a void, appears as a large gap in the die-attach material. Voids may originate as bubbles trapped in die-attach materials or lack of sufficient die-attach material applied during packaging process. SBB is the defect where the C4 bump is bridging within adjacent bump. SBB is mainly caused by the presence of conductive materials in die attach material. Figure 2.6 shows the package defects in die attach material layer.

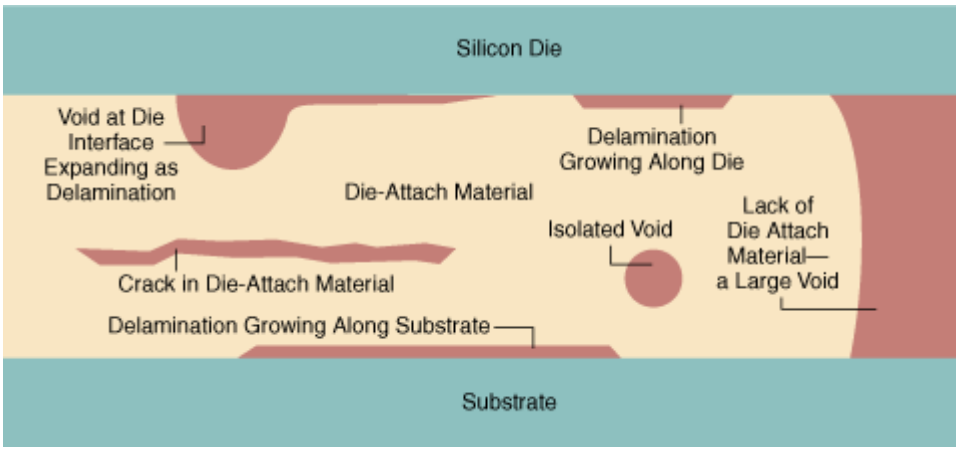

Figure 2.6: The package defects in die attach material layer [27].

Uncovering the defects is difficult, but a combination of x-ray imaging and acoustic imaging able disclose all of an IC's internal structural defects. X-ray images quickly reveal thick or deep defects that offer high contrast while Acoustic, or ultrasound, images show very thin gap-type defects. These two method are widely used by IC manufacturer in the effort of failure analysis of packaging defects in manufacturing test. Acoustic scan technique is employed in defects detection by interpreting the ultrasound signal. This techniques able to scan package defects like popcorn crack, mold void, delamination and die crack. [28]

2.8 Solder Bump Bridging (SBB)

Solder Bump Bridging (SBB) is a type of physical defect due to imperfection of packaging process in chip manufacturing. This imperfection in packaging process contributes to an extra yield lost and extra defects per millions (DPM). From previous DPM research finding, lack perfect test coverage in package defects screen [21]. Table 2.1 shows manufacturing test coverage with respective type of package defect. The defect shown are mainly defects caused imperfect assembly process.

Table 2.1: Types of package defects with respective test coverage [21].

Defects in Packaging Process		Defects Coverage (%)
1. Placement	1.1 Bridging	95
	1.2 Extra Part	55
	1.3 Wrong Part	86
	1.4 Misaligned part	97
	1.5 Opens	91
	1.6 Other	0
	1.7 Wrong Polarity	83
2. Termination	2.1 Bridging	85
	2.2 Excess	92
	2.3 Insufficient	78
	2.4 Open	94
	2.5 Other	0
	2.6 Poor wetting	30
	2.7 Solder Balling	82
	2.8 Tombstoning	98
	2.9 Volding	0
3. Component	3.1 Dead	0
	3.2 Other	0
	3.3 Tolerance	0

The HVM test plan are product dependent, different product tends have a different test plan based on product DPM budget, product family, product power, market segment, usage condition, fabrication process and etc. Only tested good units

in Sort test are qualified to continue for packaging process. Some of the HVM test flow are not able to screen SBB defect mainly due to Burn-In tester limitation.

SBB is a packaging defects of microprocessor in Flip-Chip interconnection layer. Baby Bump is a tiny lead particle found in the underfill layer C4 interconnection. The presence of baby bump in C4 interconnection layer is the main trigger of SBB defects. These Baby Bump are mainly comes from Solder Bump fraction result from deficient Flip-Chip packaging process [23]. SBB defects can be classified into 7 types based on the baby bump location. Figure 2.7 shows types of SBB defects.

Figure 2.7: Types of SBB defects.

Solder bump bridging is electrical reaction wherever the presence of conductive Baby Bump in underfill layer of C4 interconnect causes short-circuit between two or more adjacent solder bump [25]. Figure 2.8 shows the presence of the Baby Bump in C4 interconnection layer.

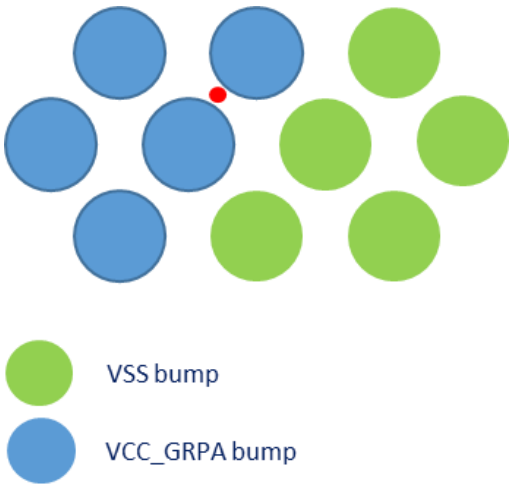

Figure 2.8: SBB defects illustration image

Certainly, the open short test in Performance test is able to effectively screen the SBB defect without fail. The SBB screening problem arise when Burn-In is the first test in product HVM test plan. Burn-In tester are not capable to perform open-short test due to tester capability limitation. Finding from failure analysis shows the Baby Bumps perish after Burn-In test execution. Subsequently, the defects units appear good and passes the open-short test in Performance Test. The limitation of Burn-In tester generates test holes SBB defects screening test. These SBB defect unbridged state is not stable and intermittent where the baby bump might tends to roll back, solder bump will back to the bridging state.

2.9 Open/short test

Open/short test is a simple in determining if the DUT pins is properly aligned to their respective contactor filaments. It will detect any misalignment or misorientation. Once detected, the testing process will no longer proceed to the succeeding tests. It is the first test within first test in Performance Test. This test is used to eliminate defective units before other succeeding tests.

It works with the principle that a diode is connected between the two test pin with force a current of 100 uA to test pins and measure the voltage. Open connectivity have a voltage readout near to design circuitry reference voltage while short connectivity readout is significant low (usually less than 0.2 V). Figure 2.9 shows the circuity of open/short test. Table 3.3 shows the test case logic and respective the expected test outcome.

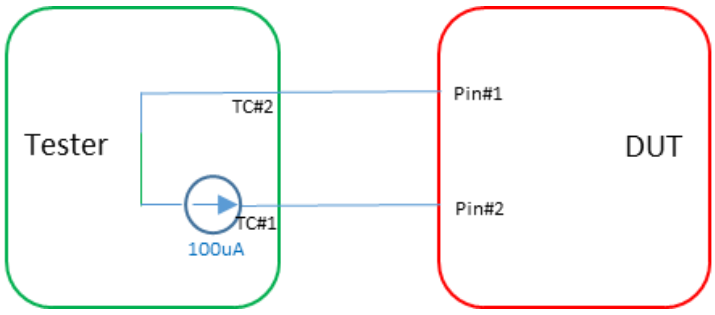

Figure 2.9: Open/Short Test Circuitry

Table 3.3: Open/short test logic and expected outcome.

Test Pin1	Test Pin2	Correct Setting	Status	Test Outcomes
VCC_GRP 1	VCC_GRP 1	Short	Short	Pass
VCC_GRP 1	VCC_GRP 2	Open	Open	Pass
VCC_GRP 1	VCC_GRP 3	Open	Short	Fail
IO_1	IO_2	Open	Open	Pass
IO_1	VSS	Open	Short	Fail

2.9 Summary

In summary, the goals of manufacturing tests are to screen out manufacturing defects in conjunction to assure that outgoing DPM targets is fulfilled. The presence of baby bump causes C4 bump bridging. In today manufacturing test flow, there is a lack of effectiveness in existing manufacturing test in screening out the SBB. As a result, SBB is invincible against manufacturing defect screen strategy.

CHAPTER 3

METHODOLOGY

3.1 Introduction

In this chapter, both the software and hardware design and development for the effective test solution to screen Solder Bump Bridging defect at Burn-In are described. This part will divide into two parts which Burn-In board development and Burn-In test program development.

3.2 Effective SBB Screening Test Development Strategy

In general, Solder Bump Bridging (SBB) screening test is a test for SBB detection and screening. The SBB screening test will be embedded within Burn-In Stress test list.

In this SBB screening test development, the development are divided into three stages which are study of SBB reaction toward electrical field, SBB detection strategy, and SBB strategy development and implementation. These development stages are dependent and continuous in ascending sequence

The purpose of the experiment is to understand the reaction of the solder bump bridging in reaction in response to intake the electrical power. Two experiment is conducted based on the four different parameters and variables which are electrical current, electrical potential, and input power. The experiment is design to characterize

the relationship between the solder bump bridging reactions with electric potential, electric current, and power. The expected outcomes from this stage are SBB reactions toward study factors is characterize and finalized with experiment outcomes.

Proceeding to second stage, the characterization study on SBB relationship with electrical power need to be finalize in prior. The second stage expected outcome are SBB detection test strategy based on the SBB characterization study. At this stage, Burn-In test environment will be assess and test strategy will be develop. In Burn-In test environment assessment, the features and limitations of Burn-In test platform will be review. This BI test chamber capability assessment is crucial for SBB test strategy planning. Based on the data on SBB characterization study and BI test chamber capability assessment, the SBB test strategy will be design to detect the SBB defects with current BI test chamber capability.

The final stage is SBB screening test development. The SBB screening strategy in second stage is developed into SBB screening test design. SBB screening test design consists of two main part, which are test hardware design and test program development. In test hardware design, Burn-In Board will be redesign to support the SBB screening test. Some features will be added to BIB for the SBB screening test enable purpose. SBB screening test program is a test module embedded in Burn-In test. In test program development, the SBB screening test strategy is converted to SBB screening test model in Burn-In test program. SBB screening test model contains the SBB screening test strategy in Burn-In environment coding form. Figure 3.1 shows SBB screening test development is illustrated in the flow chart.

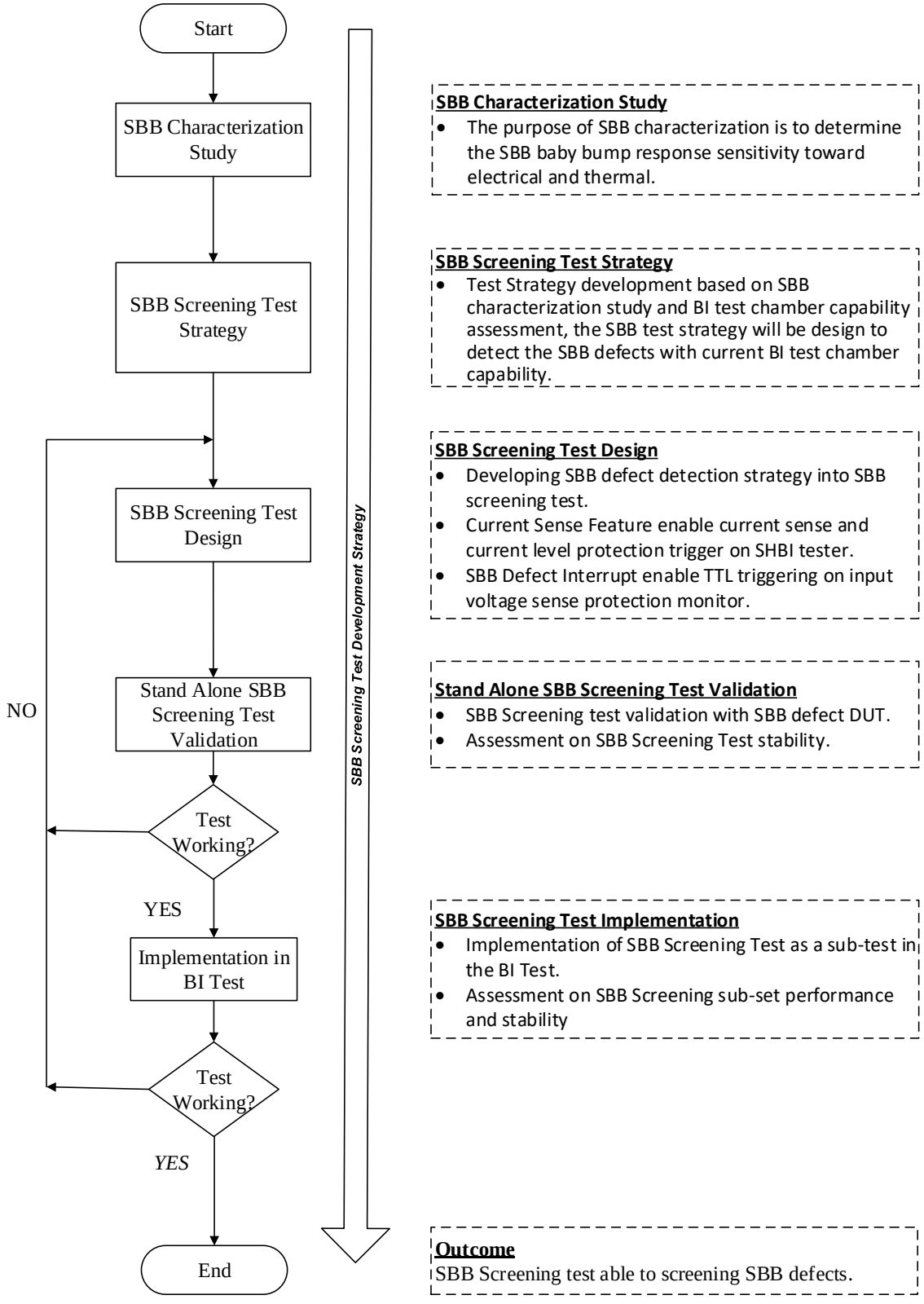

Figure 3.1: SBB screening test development flow