# PCIE IP VALIDATION PROCESS ACROSS PROCESS CORNER, VOLTAGE AND TEMPERATURE CONDITIONS

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# PCIE IP VALIDATION PROCESS ACROSS PROCESS CORNER, VOLTAGE AND TEMPERATURE CONDITIONS

**by**

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| | | |
|---|---|---|
| FPGA | : | Field Programmable Gate Array |
| IP | : | Intellectual Property |
| PCIe | : | Peripheral Component Interconnect Express |
| PCI SIG | : | Peripheral Component Interconnect Special Interest Group |
| USB | : | Universal Serial Bus |
| SATA | : | Serial AT Attachment |
| HSSI | : | High Speed Serial Interface |
| SV | : | System Validation |
| CV | : | Compatibility Validation |
| EV | : | Electrical Validation |
| PRQ | : | Product Release Qualification |
| SOC | : | System on Chip |
| LTSSM | : | Link Training and Status State Machine |
| PIPE | : | PHY Interface for PCIe |
| EP | : | Endpoint |
| RP | : | Root Port |
| TX | : | Transmitter |
| RX | : | Receiver |
| TT | : | Typical Skew Unit |
| SS | : | Slow -Slow Skew Unit |
| FF | : | Fast-Fast Skew Unit |
| DUT | : | Device Under Test |
| ANOVA | : | Analysis of Variance |
| T | : | Temperature |
| V | : | Voltage |
| GT/s | : | Giga-Transfer per Second |
| ms | : | milli-second |

PROSES PENGESAHAN IP PCIE MERANGKUMI SEMUA VARIASI KELAJUAN PERANTI, VOLTAN DAN SUHU.

## ABSTRAK

Pengesahan IP telah menjadi lebih mencabar untuk peranti FPGA kerana ia menyokong kelajuan operasi yang tinggi. Peripheral Component Interconnect Express (PCIe) adalah IP yang digunakan untuk pemindahan data berkelajuan tinggi yang disokong oleh Intel FPGA. Spesifikasi asas PCIe 3.0 menyokong pemindahan data berkelajuan 8.0 GT/s, 5.0 GT/s dan 2.5 GT/s. Latihan pautan dan Inisialisasi dilakukan pada lapisan fizikal untuk menganalisa lebar pautan dan kadar data pautan. Lapisan fizikal semakin kompleks apabila ia menyokong kelajuan yang lebih tinggi. Keadaan operasi hanya berlaku ketika Hubungan Latihan dan Keadaan Status Mesin (LTSSM) mencapai keadaan L0 setelah peranti dikonfigurasi. Latihan kestabilan latihan diperbaiki dengan mengoptimumkan reka bentuk logik dalam lapisan aplikasi. Dua ujian protokol yang biasanya disahkan dalam industri adalah pengujian menghidupkan dan pengujian pautan & lapisan yang lebih tinggi. Alat pengujian yang disokong oleh Quartus digunakan sepenuhnya untuk mengesan kegagalan semasa latihan pautan. Pencirian prestasi pautan meliputi semua sudut proses, keadaan voltan dan suhu amat sukar dianalisa. Dengan menggunakan kaedah ujian hipotesis, data yang dikumpul memberikan trend yang jelas pada prestasi pautan PCIe. Pernyataan $H_0$ menunjukkan perbezaan yang jelas untuk kes lulus dan gagal. Dalam kajian ini, kes terburuk berlaku pada voltan rendah dan suhu rendah tanpa mengira sebarang sudut proses. Nilai-p lebih besar daripada 0.05 membuktikan pernyataan $H_0$ yang diterima. Perbezaan pada peratusan lulus dan gagal tidak menjejaskan prestasi pautan keseluruhan PCIe. Ia menyimpulkan bahawa kegagalan semasa latihan pautan itu rawak dan tidak disebabkan oleh sebarang kecacatan pada susun atur silikon peranti FPGA. Oleh itu, pengesahan IP menunjukkan kekukuhan peranti dan dapat mematuhi spesifikasi asas PCIe.

PCIE IP VALIDATION PROCESS ACROSS PROCESS CORNER, VOLTAGE AND TEMPERATURE CONDITIONS

## ABSTRACT

IP validation has become more challenging for FPGA device as it supports high operating speed. The Peripheral Component Interconnect Express (PCIe) is an IP used for high speed data transfer that supported by Intel FPGAs. The base specifications of PCIe 3.0 supports 8.0 GT/s, 5.0 GT/s and 2.5 GT/s. The link training and Initialization takes place at physical layer to initialize the link width and link data rate. The physical layer is getting more complex when it supports higher speed. The operational state only happens when Link Training and Status State Machine (LTSSM) reaches L0 state after device being configured. The stability of link training is improved by optimizing the soft logic design in application layer. Two protocol tests usually validated in industry are link up testing and link & higher layer testing. Debugging tools supported by Quartus are fully utilized to detect any failure during link training. The characterization of link performance covers process corners, voltage and temperature conditions are hard to analyze. By using hypothesis testing method, data collected gives a clear trend on the PCIe link performance. The $H_0$ statement shows a significant difference for passing and failing case. In this research, the worst case happened at low voltage and low temperature regardless of any process corners. The p-value is greater than 0.05 proved $H_0$ statement is accepted. The difference on passing and failing percentage is insignificantly impacting overall link performance of PCIe. It concludes that the bug is random and not caused by any defects on the silicon layout of FPGA device. Thus, IP validation shows the robustness of the device and able to comply with base specification of PCIe.

# CHAPTER 1

# INTRODUCTION

## 1.1 Overview

The advancement of technology is very competitive in electronic industry. As the electronic technology shrinks in size, the greater the electronic fabric design complexity gets. Thus, it gets harder to validate the specifications of the analog and digital signals.

Intellectual Property (IP) validation is to validate the functionality of the IP hence to determine the robustness of the device. Post-Silicon IP validation for microprocessors encapsulate crucial areas such as system validation (SV), compatibility validation (CV), and electrical validation (EV) [1]. A decision made for Product Release Qualification (PRQ) milestone are based on results obtained from the validation [2]. The PRQ milestone is to ensure the device is functionally good and ready to be out in market.

In the hike of advanced technology nowadays especially in communication fields, sophisticated military equipment and autonomous driving in automotive industry have driven the needs of advanced semiconductor technology that capable of morphing and perform delicate tasks that can be done by a small yet powerful Intel FPGA chip. These demands had led data transmission consortium a vital part in high end technology particularly to meet with industrial standards. Peripheral Component Interconnect

Express (PCIe), Universal Serial Bus (USB), Synchronous Optical Network (SONET) and Universal Asynchronous Receiver Transmitter (UART) are among the industrial standards in data transmission interface protocols.

PCIe IP is a high-speed serial interface commonly used as an interface for flash storage in industrial applications such as data center, cloud computing, sever and Ultrabook. For instance, SATA-based interface that can be found in Solid State Drive (SSD) in many computer and electronic devices has limited capacity of data transfer [2]. PCIe technology is most preferable protocol used in communication industry as it gives higher speed and better throughput.

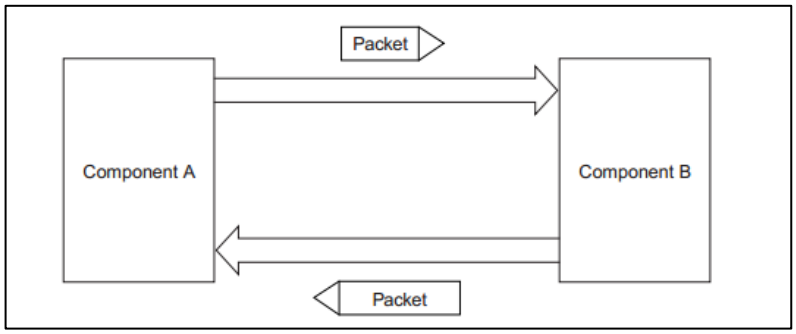

Figure 1.1 PCI Express Link [3].

Figure 1.1 illustrates the handshaking procedure between two devices. In PCIe link, component A act as a root port device while component B as an endpoint device. For instance, a root port can be assumed as a PC while the endpoint as a graphic card. A PCIe link shows a packet-based of bi-directional communication channel for component A and component B.

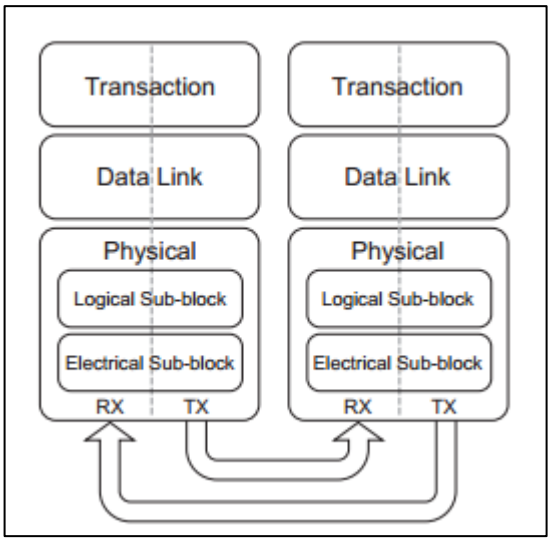

Figure 1.2 High Level Diagram of PCIe [3].

Figure 1.2 shows the PCIe protocol consists of three layers to carry the packets of data between two devices through transmitter and receiver physical port. The three layers of protocol stack are transaction layer, data link layer and physical layer. The application layer is on top of three layers and designed as a soft layer. The soft layer can be modified and implemented depends on customer's application. Link Initialization and Link Training is a Physical Layer control process that configures and initializes a device's Physical Layer, port, and associated Link so that normal packet traffic can proceed on the Link. This process is initiated after reset without any software. A receiver may optionally check for violations of the link training and initialization protocol. Link training takes place after FPGA is configured and exercise physical layer of transceiver.

Four main states play major role for link initialization which are detect, poling, configuration, and L0 state. L0 state is the normal operational of receiving and transmitting packet of data takes place. There are sub states under each state before it reaches stable known as L0 state. The stability of L0 state is determined when it is not

having any retrain and correct register settings with expected link speed and lane width.

There are many issues during link training process. Several steps are needed to enable the functionality of PCIe IP. The firmware, software, and hardware need to be considered during validation. These considerations help to improve the stability of PCIe link.

The performance of PCIe link training is further validated across various process corner, voltage and temperature conditions. Process corner is a skew unit variation in a silicon fabrication. Those variations affect the performance of the device depending on the operating voltage and temperature. Process corner covers three different skew units, which are typical device (TT), slow device (SS) and fast device (FF). The timing calibration of Intel FPGA using Nios technology help compensate for changes in process corners, voltage or temperature. The advance calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions.

## 1.2 Problem statement

The serial protocol like PCIe has evolved over the years to provide very high operating speeds and better throughput. This evolution has resulted in their physical layer protocol namely physical medium attachment (PMA) and physical coding sublayer (PCS) architecture became more complexed.

The link training and link initialization is the most essential processes at physical layer. This process establishes many important tasks such as link width

negotiation and link data rate negotiation. All these functions are accomplished by Link Training and Status State Machine (LTSSM). The LTSSM tunes and trains the PCIe link for reliable data transfer. L0 state is the normal operational state where data and control packets are transitioned. The transition state from LTSSM to reach L0 state is hard to achieve due to complexity of physical layer structure when the operating speed is higher.

Furthermore, the application layer of PCIe protocol stack was designed using soft logic circuit. The design gets more complicated and hard to meet the timing margin of the circuit to comply with PCIe protocol. As a result, more complexed routing path in the FPGA utilized when more protocol testing is required.

For IP validation, protocol testing is tested at 1000 iterations with different process corners, voltage and temperature settings. The link performance varies at different link speed and lane width across process, voltage and temperature (PVT). The variation is hard to analyze and conclude because it doesn't show any big significant different for each test. Thus, an accurate data analysis methodology is needed to apprehend the problem, and these will be the focus of this research.

## 1.3 Research Objective

The objectives of this research are:

1. To improve the stability of PCIe protocol link training by optimizing the soft logic design in application layer.
2. To analyze the performance of PCIe protocol across PVT variation by using hypothesis testing.

## 1.4 Project scopes

There are a few methodologies used by industry to characterize a link stability of PCIe link training process especially on a high-end FPGA device. This research project focuses on the link training process of PCIe protocol using Intel FPGA 20nm technology as an endpoint device and StratixV FPGA 28nm as a root port device. In addition, this research will cover three speeds that are supported in PCIe Base Specification Revision 3.0, there are 2.5 GT/s, 5.0 GT/s and 8.0 GT/s. All the lane configuration supported by PCIe protocol x1, x2, x4 and x8 lane are validated during protocol testing.

Three process corners involved in this research, which are FF, SS and TT of transceiver. The voltage variations are covered at minimum and maximum voltage as documented in device specifications. The experimental setup at low temperature (-25℃) and high temperature (100℃) are experimented in this research.

Link stability performance is examined and debugged through SignalTap and System Console supported by Quartus software. The flow of automation is using TCL language. MiniTab 16.0 is used to analyze the raw data. ANOVA method and Tukey as comparison method are applied in this research.

## 1.6 Thesis Organization

The remainder of this dissertation is organized as follows:

Chapter 2 reviews the importance of post silicon IP validation in high speed protocol, introduction of PCIe protocol, PCIe hard IP, the link training state descriptions, link training failure, debugging guideline for Xilinx, link stability of PCIe protocol overview and reset mechanism,

Chapter 3 describe the overall methodology of this research starting with experimental setup for root port device and endpoint device. The maximum and minimum voltage and temperature supported by an endpoint device are listed. The software setup which utilized all the tools by Quartus. The methodology in identifying the failure causes during link training is explained. This chapter end with a chapter summary outlining method to analyze data using hypothesis testing.

Chapter 4 begins with a prove of link training performance reaches L0 state during protocol test. It is followed by the result of 1000 iterations of protocol test across fast and slow process corner. It analyzes the performance of PCIe link stability over various link speed and lane width configuration at different voltage and temperature

condition. This chapter ends with an analysis and discussion on the comparison of the performance for different process corner, voltage and temperature.

Chapter 5 summarizes and concludes the results from the improvement of link stability using the methodology explained and performance of PCIe link stability for different process corner, voltage and temperature and outlines future recommendations for improvement related to this research.

# CHAPTER 2

# LITERATURE REVIEW

## 2.1 Overview

This chapter starts with some in depth study on post-silicon validation especially on high-speed serial interconnect that is used by Intel PSG; the leading Field-Programmable Gate Array (FPGA) which provide the speed of hardware and the flexibility of software. The importance of post-silicon validation and challenges is described. One main protocol, PCIe Hard IP, Intel's most leading protocol is well explored with major interest in link stability of link training process. The PVT impacting the stability of PCIe link training is discussed. This chapter ends with a chapter summary

## 2.1 Importance of post-silicon IP validation

The pace of technology is getting faster where computing devices and gadgets are well-equipped with smaller dimension of integrated chip, powerful sensors and advance software are patched to make the device compatible with human needs [3]. A time-to-market strategy has made the pace of technology kicks in.

Post-silicon IP validation is a very critical part of device characterization especially in FPGA devices. It is used to identify and solve bugs in complex integrated

circuit which cannot be captured during pre-silicon validation [4]. The complexity in layout of integrated circuits increased the bugs for fabricated silicon. The limited time-to-market period worsen the situation, as the quality assurance of the device is neglected [5].

The detection and diagnosis are required to impose debug operation prior to high volume production [6]. The dependency on pre-silicon validation collected data is not valid as the coverage is lesser. During pre-silicon validation, test cases will be running on virtual environment with sophisticated software tools are used [7]. Simulation and emulation are one of the tools used in pre-silicon validation still, it constraints the accuracy of the device.

Worst test case coverage on the silicon will induced the probability of emerging the bugs thus a well-planned data analysis methodology is important to see the performance of the new silicon.

There are few level of debugging in post-silicon IP validation, which include the software and hardware preparation. These approaches will help to execute task in timely manner and easier to uproot the failures. During bugs detection phase, proper stimuli need to be carried out, listing all the critical bugs that are difficult to solve. This method is prone to be able to dissect the bugs into smaller regions thus easy to identify the occurrence of the bugs. Once the bugs are identified, software patching, silicon re-spin and editing the baseline design [7] are the only options left to incinerate the bugs.

There are few types of bugs that can be classified including electrical bugs and logic bugs [8]. Electrical bugs are closely related to signal integrity of the board such

as crosstalk between traces and the length of the traces induced noise. The power supply shortage and thermal effects in experimental setup also cause electrical bugs. The interfaces of digital and analog circuitries deemed to be very challenging component to dealt with [9]. Process corner variations which cover slow and fast corner devices will varies the electrical bugs in post-silicon validation. Thus, handling the experimental setup require extra precaution as it will help to isolate the logic bugs emerge in the validation.

Typically, logic bugs emerged from design error. Furthermore, with the unknown territorial state of the device behavior further factor in with incorrect implementation of hardware and low-level system software, will induce additional logic bugs.

Post-silicon IP validation needs to imitate a real system environment including DUT, board and system level validation [1]. The real system environment illustrates a behavior of new silicon that correlates the findings from user side, but typically, users will not undergo extreme limit of the test. The protocol validation is done to ensure the performance of PCIe able to support the device. The stress test on post-silicon IP validation helps to identify the robustness of the device that will ensure high confidence level to the system.

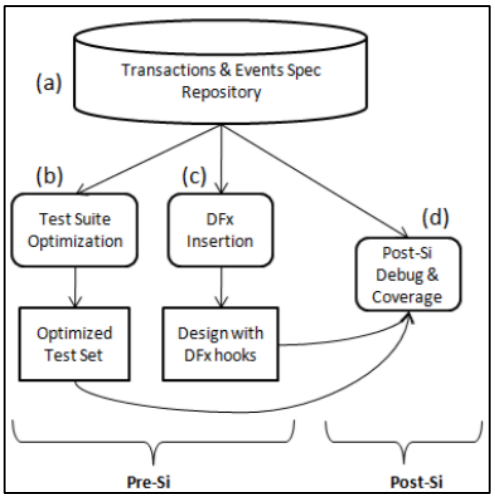

Figure 2.1 Pre to post flow [10].

Figure 2.1 shows the workflow of pre-silicon validation and post-silicon validation. Although the effort of post-silicon validation is cost inefficient and time consuming to meet the milestone of first fabricated silicon, new effort has been introduced to improve the productivity of post-silicon validation and debug by proper investment in design for debug or validation (DFx) and in test development during pre-silicon stages [10]. Pre-silicon validation illustrates the system level behavior. It requires more investment compared to post-silicon validation. Implementing a proper planning in the early stage of IP architecture to cover the important system help to ensure a good performance and utilized a good setting upon silicon availability.

By extending the delay models, which determine the slow paths and slow IC during pre-silicon validation helps to determine the worst case of first fabricated silicon [11]. Thus, it isolates the worst cases that need further investigation and reduce a run time during post-silicon validation.

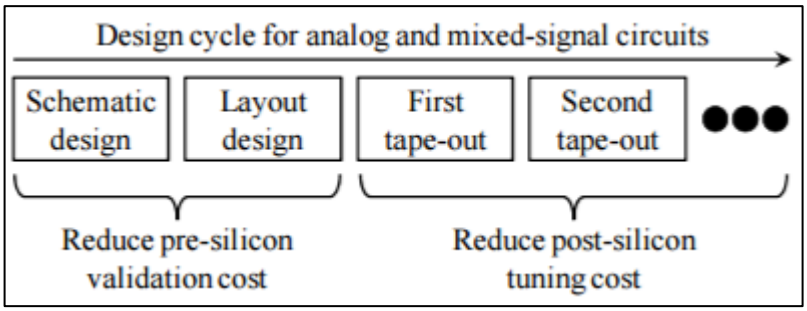

Figure 2.2 Bayesian Model Fusion (BMF) [12].

Figure 2.2 shows an example of the efficient validation using Bayesian Model Fusion (BMF) at early stage, while at final stage, analog mixed-signal (AMS) is tuned. The method introduced helps to reduce cost and timeframe of pre-silicon and post-silicon validation [12]. At the final stage of post-silicon validation, the approach was done by estimating the data accurately from schematic level. Proper planning will be rolled out in timely manner to achieve time-to-market product goals.

## 2.2 PCIe Architecture

PCIe is a high performance, general purpose I/O inter-connect technology defined for a wide variety of future computing and communication platforms. Data transaction is encapsulated in packets. The data formed in transaction layer is passed through data link layer. The physical layer help transmit data which is encoded according to the type of data sent by transmitter port, through physical link cable to far end device.

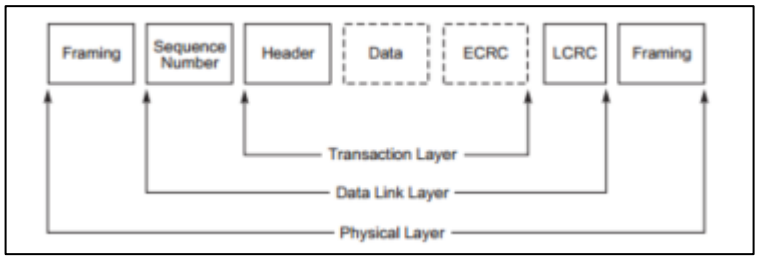

Figure 2.3 Packet Flow Through the Layers [3].

Figure 2.3 illustrates the 3.0 base specification of PCI Express Revision 3.0 covers up to the highest transfer rate up to 8.0GT/s. The transfer rate is standardized across all PCI Express user. The maximum transfer rate introduced in base specifications revision3.0 are Generation 1 (Gen 1) PCI Express systems is 2.5 GT/s; Generation 2 (Gen 2) PCI Express systems, 5.0 GT/s; and Generation 3 (Gen 3) PCI Express systems, 8.0 GT/s. These rates specify the raw bit transfer rate per lane in a single direction and not the rate at which data is transferred through the physical connection of the system. Once initialized, each Link must only operate at one of the supported signaling levels. The data rate is expected to increase with technology advances in the future.

In PCIe IP validation, two components are required to have PCIe supported interface namely the root port and the endpoint. Intel FPGA device families support PCIe IP interface, which can be configure as the two components mentioned earlier. The PCIe configuration follows the industry standard which stated in Base Specification of PCIe Revision 3.0.

## 2.3 PCIe Hard IP

There are two methodologies of IPs including hard IP and soft IP. Hard IP has an IP block which cover the physical block implementation in a layout and logic implementation in RTL code. Optimizing the hard-circuited IP through process technology will guarantee better timing performance [13]. It saves 20 percent of the logic resources by implementing hard IP in the design. Soft IP is a soft logic implementation in RTL code which need extra effort to patch as a physical implementation.

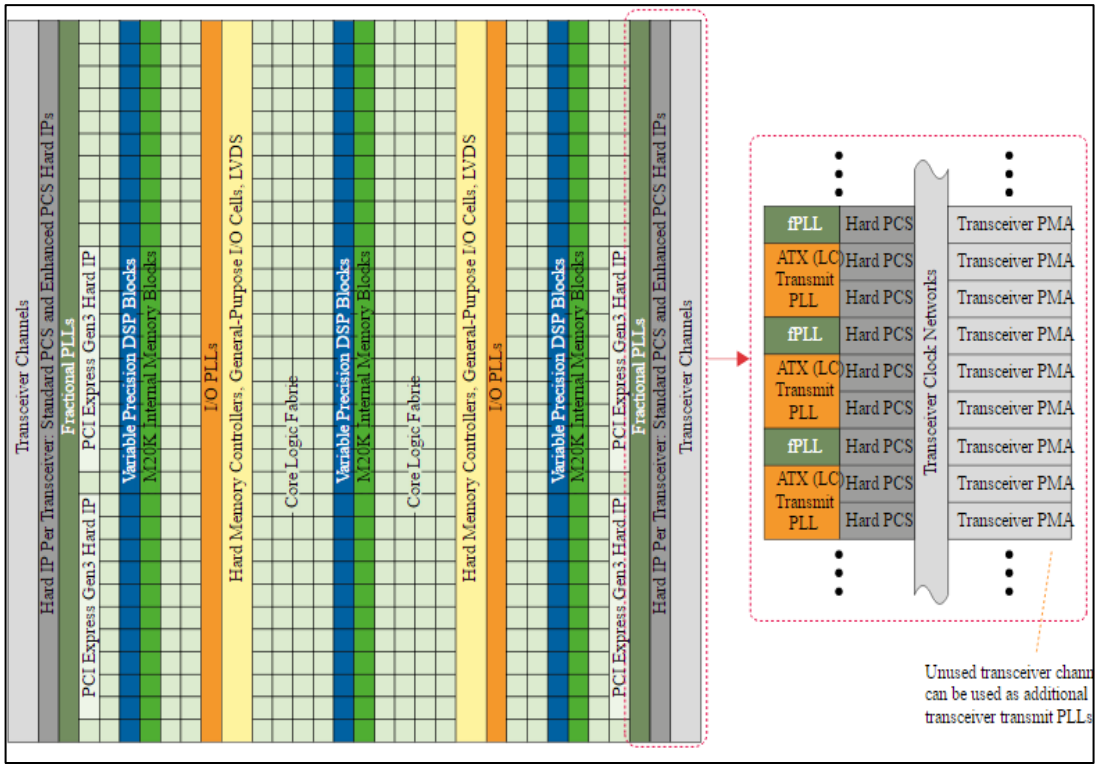


Figure 2.4 Intel FPGA 20nm device overview [18].

Figure 2.4 shows a device overview of Intel FPGA 20nm where hard IP is located on the right and the left side of the transceiver of a device. Intel FPGA 20nm

technology has embedded the PCIe hard IP block and complies with PCIe base specification, Rev 3.0. It has the highest data transfer rate supported by PCIe 8.0 GT/s. The outdated intel FPGA family devices can only comply with PCIe base specification, Rev1.0 and Rev2.0, which support up to 5.0GT/s.

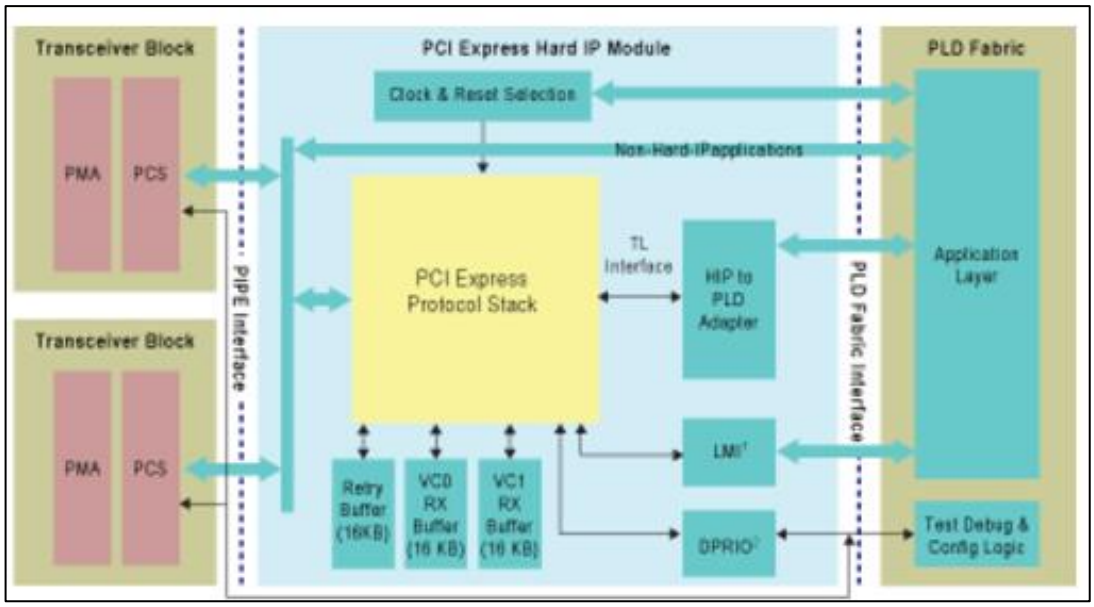

Figure 2.5 Overview of PCIe hard IP block diagram [19].

Figure 2.5 illustrates the PCIe hard IP module between transceiver block and programmable logic design (PLD) fabric. The protocol stack is designed to comply with industrial PCIe protocol standards to give a high confidence level to Intel FPGA PCIe performance. There are benefits of hard IP block as it saved up the resource of logic elements because it is hard-circuited in a silicon layout. It shortens the time of designing a pattern and reduce timing failure. The logic bugs captured during device enabling can be eliminated by optimizing the design logic at application layer.

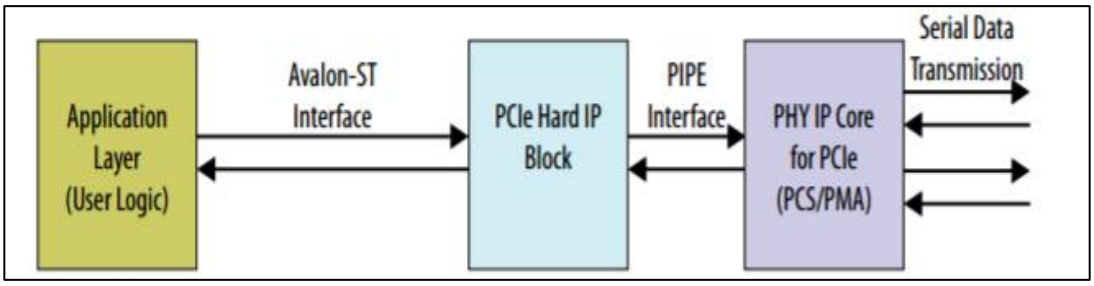

Figure 2.6 Intel FPGA 20nm bridging with Avalon-ST interface [20].

Figure 2.6 shows the interfacing of Intel FPGA 20nm fabric through Avalon ST-interface. The PHY IP core consists of PCS, PMA and a media access control (MAC) layer. The bridging between PCIe hard IP block and PHY IP core is through PIPE interface.

The application layer is designed by user to be implemented in core fabric of FPGA. It can be edit according to user preferences to achieve maximum effective throughput. Avalon-streaming (Avalon ST) is one of the type of application interface to the application layer. In hard IP mode system settings, the lane data rate including Gen1, Gen2, and Gen3, which support only the 256-bit is chosen according to user's criteria.

There are two root types; native endpoint and root port. Avalon ST only support native endpoint operation [14]. The system settings used to optimize the throughput for efficient data transfer. These settings need to be implement in pattern bring up hence in post-silicon validation.

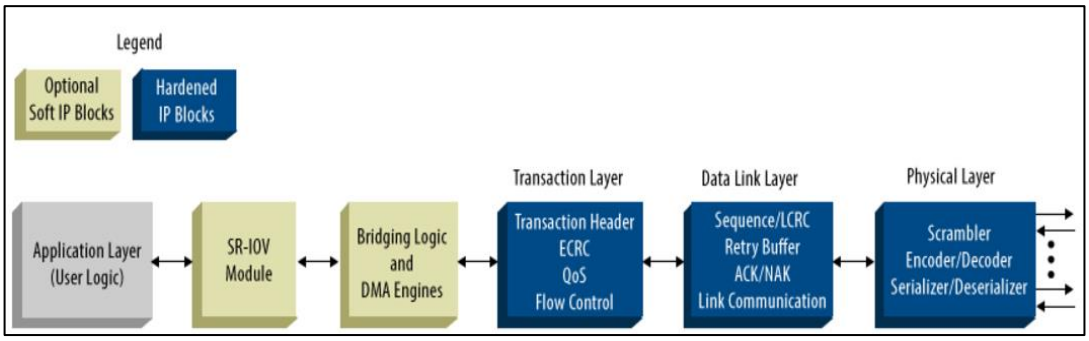

Figure 2.7 Intel FPGA PCIe block diagram [3].

Figure 2.7 shows a PCIe block diagram which consists of soft IP blocks and hardened IP blocks. PCIe layer stack is hardened IP block that comprised of transaction layer, data link layer and physical layer. Bridging logic and DMA engines are soft IP which mainly used for debugging.

Intel FPGA PCIe hard IP gives high confidence level to the performance of PCIe as it is hard-circuited in silicon. It is easier to identify the failure causes by reviewing the system settings and simulation that can be generated and tested during pre-silicon validation. The link training can be simulated and tuned if major issue occurs.

## 2.4 Link Training and Status State Machine (LTSSM) Descriptions

In any device supported by PCIe protocol, link training process is the basic element of PCIe. Besides, the packet formed in transaction layer and any transaction of packet through layer by layer, there is a mechanism needs to start as it will determine the stability of the link. The link training process can predict PCIe link stability when it stables at its expected performance including speed rate, lane width and link up status.

Ordered sets are used for link training, it will be transmitted as a group of characters on all lanes. Ordered sets are packets that originate and terminate in the physical layer. To successfully go through lane initialization and form an expected link to start a link training process, ordered sets are send as an indicator for the lane readiness.

Before a packet of data is transmitted on the link, the link training process will kick starts the PCIe engine. Link training process is taking place after FPGA being configured. PCIe protocol is a handshaking protocol of two devices, where both devices must support PCIe protocol. The endpoint and the root port need to be configure before a link training starts and reaches L0 state. The normal operating PCIe only happens when it reaches L0 state.

The new silicon will be the endpoint while the root port will be the matured silicon. This is due to matured product that has its performance improved over time, thus reduce debugging steps that is very time consuming.

The handshaking process to initiate PCIe link training requires two basic components, which are a transmitter, handling the status bit during link up process, and a receiver that handle the error status bits. A successful status of link up process can be determine based on PCIe protocol specifications provided by PCI-SIG.

In high-level overview, link training process is occurring between data link layer and physical layer which also known as PHYMAC layer. DETECT, POLLING, CONFIGURATION and L0 are four states component present during link training process. Each states execute their task independently and capable of pinpointing the failure causes during link training which in turn eased the debugging efforts.

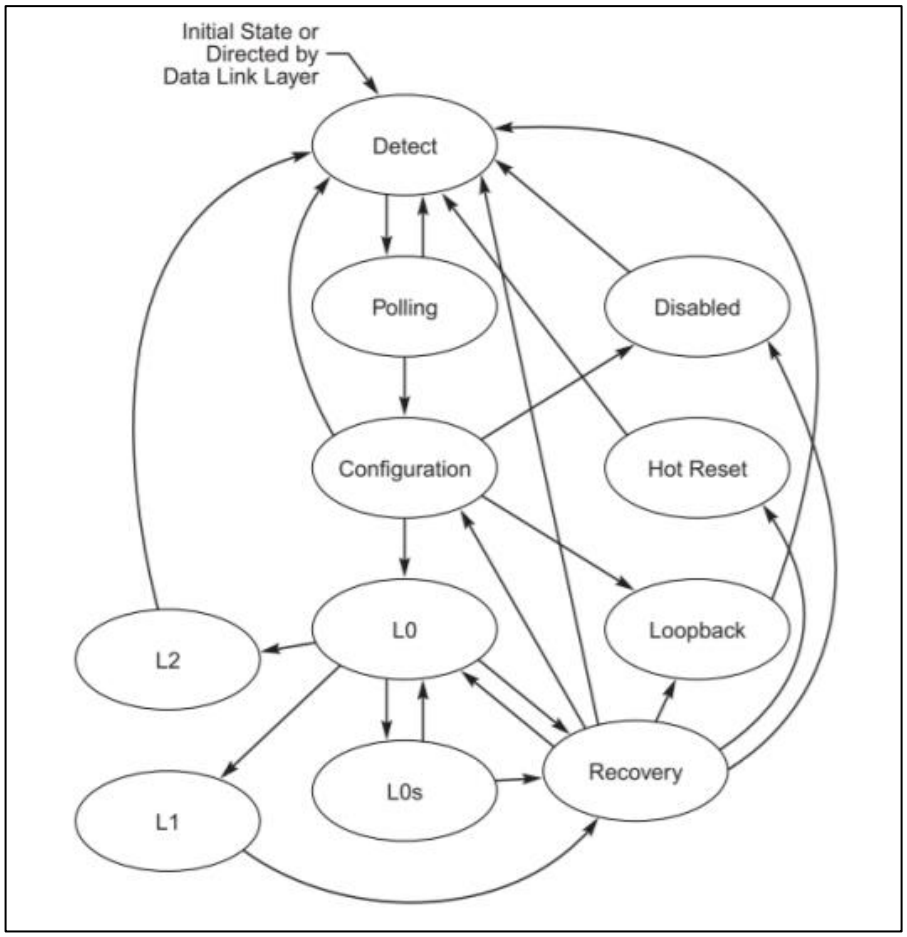

Figure 2.8 LTSSM flow diagram [3].

Figure 2.8 shows a LTSSM flow transition from one state to another. DETECT State is the first LTSSM state that entered after hardware reset or Hot reset. It is to detect the present of far end device and it actives all the time.

The next state is POLLING state, it serves as transmitter and responder to training Ordered Sets. During this state, bit lock and Symbol lock are established and Lane polarity is configured. The transmitter port validation focuses on electrical characteristics and it covers all signal integrity issue including crosstalk.

CONFIGURATION state took place after polling state done with its process execution. Transmitter and receiver start sending data on the expected data rate. Link

and lane numbering; x1, x2, x4 and x8 are negotiated in this state depending on the PCIe design configured on the device.

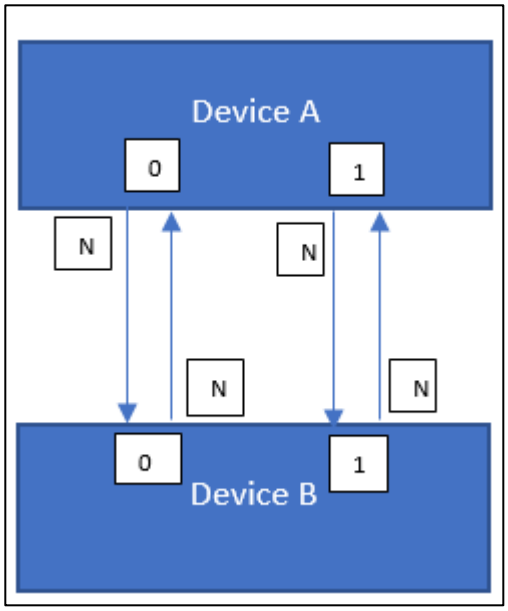


Figure 2.9 Before lane initialization.

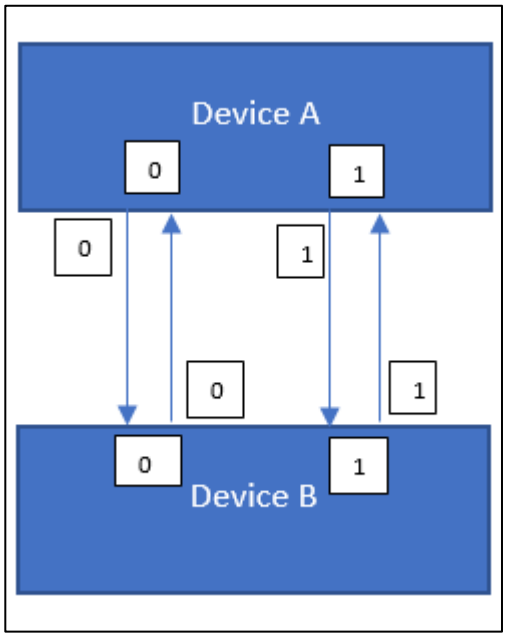


Figure 2.10 After lane numbering.

Figure 2.9 and 2.10 shows an example of x2 lane configuration before and after lane numbering process. Configuration of lane numbering begins with device A sending TS1 ordered set, the device B detecting the link status active ON will send a respond through TS1 ordered set. Then, device A sends TS2 ordered sets indicating the link number is activated. After device B received TS2 ordered set, it confirmed the lane numbering by sending TS2 to device A. Thus, both devices are acknowledged on how many lanes to be tested.

L0 state is the main goal of every link training process. Achieving L0 state at the early stage of device enabling is very difficult, as it has to pass through several stages that need to be fulfilled. The stability of PCIe link can be measure by running the protocol test for different process corner, voltage and temperature conditions. The asserted link up status is indicating the link ready for data transaction. In an event when the link is failing, it will go to recovery state or restart the whole process over again.

For ease debugging purposes, the four main states mentioned early are very important. This is because it requires state-by-state error cleansing process to identify the errors flag during link training process. There is timeout on each states that can cause a major issue when running on a very stressful operating condition.

## 2.5 Link training issue

Link Initialization and Link Training is a Physical Layer control process that configures and initializes a device Physical Layer, port and associated Link so that the

normal packet traffic can proceed on the Link. This process is automatically initialized after reset without any software involvement. A sub-set of Link retraining is initiated automatically due to power ON state from a low power mode or an error condition that renders the Link instability.

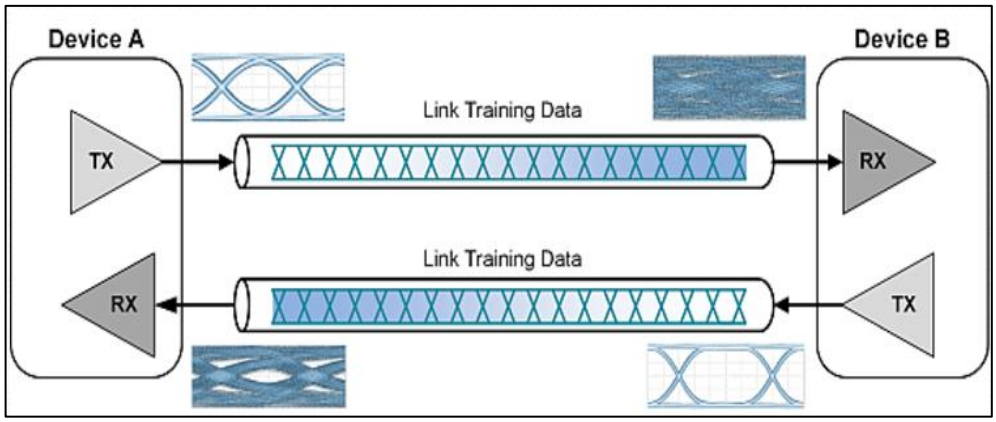


Figure 2.91 The link training overview [18].

Figure 2.11 illustrates the link training at the same speed on both devices. The eye of data transmitted and received will determine how good or bad the link training is. When the observed data is far off the expected data, the link training issues occurred.

Reset failure is a very common in new silicon in comparison to the reset mechanism from matured product. The device is stuck at reset state even after releasing its reset. By resetting the device, it clears off the issue occurred in link training. If the reset failure happen, the device is probably having a bug on the silicon layout and not PCIe related issue.

Receiver error is asserted during link training process, as it does not meet the specifications. The equalization engine need to be optimized and fully functional to

support data transaction. Packet of data dropped in the whole process resulting in the unreliable data being transferred which consequently effecting the system performance.

Furthermore, the speed trains down to non-desired speed is one of the common issue found recently for enabling the new device. This is usually related to speed supported by root port device. The endpoint only can go up to its maximum speed when root port is supporting the speed. The LTSSM state can help iron out this issue.

Another issue found is the lane width trains down to non-expected lanes as pattern design. Physical connection of link between both devices such as PCB layout and devices that can contribute to signal integrity issue needs to be error free. As the lanes increases, noise between traces will induced on each lanes. Experimental setup including power supply and the placement of metal on the board need an extra care.

Error flagging by accessing direct memory access (DMA) engine is a new method to locate the bugs Base Specification of PCIe. DMA is interfacing the application layer and transaction layer. By reading and writing a DMA master it has a better coverage on the error flagging during link training process.

The issues found during device enabling need to be addressed and solved in a very short time. It is a first level of PCIe link training issue before it achieves link stability and can be tested over various range of operating conditions.