POWER MANAGEMENT CONTROLLER BY USING INTEL MAX 10 FPGA

By

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A Dissertation submitted for partial fulfillment of the requirement for the degree of Master of Science (Electronics Systems Design Engineering)

August 2017

ACKNOWLEDGEMENT

I would first like to thank my thesis advisor Dr. Syed Sahal Nazli Alhady Bin Syed Hassan of the School of Electronics at USM. He consistently allowed this paper to be my own work, but steered me in the right the direction whenever he thought I needed it. He also goes through chapter by chapter on my thesis to check if anything that need improvement. Lastly, he also helps me to prepare the equipment for this project oscilloscope and power supply during demonstration.

Secondly, I want to thank Rich Howell that propose the power management controller idea to work on Intel Stratix 10 FPGA by using Intel MAX 10 FPGA. I also want to thank Tony Chen and Mostafa Shaban provide me support on the Intel Enpirion PowerSoC Evaluation Kit during initial test. Finally, I want to thank Intel Cooperation that allow me to use their board for this project development. It also allows me to introduce the usefulness of FPGA and contributed for the electronics industry.

I also want to thank USAINS especially Mazlin, she helps me on the administration on the thesis for USM. Beside this she also helps me on the submission of the thesis to School of Electronics at USM.

Finally, I must express my very profound gratitude to my parents and to my spouse for providing me with unfailing support and continuous encouragement throughout my year of study and through the process of designing and writing this thesis. This accomplishment would not have been possible without them. Thank you.

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List of Abbreviation

Abbreviation	Meaning
ADC	Analog to Digital Convertor
ALRT	PM Bus Alert Signal
ASIC	Applications-specific Integrated Circuit
ASSP	Application-Specific Standard Product
Avalon-MM	Avalon Memory Mapped Interface
CAN Bus	Controller Area Network
CPLD	Complex Programmable Logic Device
CTRL	PM Bus Control Signal
DC	Direct Current
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
I/O	Input/Output
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
IP	Intellectual Property
LDO	Low-Dropout Regulator
LED	Light Emitting Diode
MCU	Microcontroller
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PC	Personal Computer
PM Bus	Power Management Bus
PLL	Phase Lock Loop
POL	Point of Load
POR	Power On Reset
PWM	Pulse Width Modulation
PGOOD	Power Good Signal
RS 232	Recommended Standard 232
RS 485	Recommended Standard 485
SM Bus	System Management Bus

SCL	PM Bus Serial Clock Line
SDA	PM Bus Serial Data Line
SPI	Serial Peripheral Interface
SoC	System on a Chip
SRAM	Static Random-Access Memory
TSD	Thermal Sensing Diode
UFM	User Flash Memory
USB	Universal Serial Bus
UART	Universal Asynchronous Receiver/Transmitter

ABSTRACT

Currently, FPGA (Field Programmable Gate Array) is one of the choices that consider for digital system design compare to ASIC (Application-Specific Integrated Circuit). This is due to the flexibility of the FPGA to update design based on the application. Intel Stratix 10 FPGA is the FPGA from Intel Cooperation that required proper power sequencing to avoid damage on the devices. Besides power sequencing, Intel Stratix 10 FPGA required 200 us to 100 ms POR (Power On Reset) during power up sequence to avoid FPGA in reset state and require total power down sequence in 100 ms. There are a lot of power sequencing methods are implemented for FPGA such as discrete component, resistor divider rule, sequencing IC (Integrated Circuit), MCU (Microcontroller), CPLD (Complex Programmable Logic Device) and FPGA. All these approaches are used to control the power on and off for the voltage regulator through pin enable voltage regulator and standard interface such as SM (System Management) Bus and PM (Power Management) Bus. For this project, non-volatile Intel MAX 10 FPGA is used for power management controller. This FPGA include internal ADC (Analog to Digital Converter) and UFM (User Flash Memory) that is critical to design power management controller. Power management controller is running on NIOS II and Avalon-MM (Memory-Mapped) Bus is used to connect all the ADC, UFM, timer, UART (Universal Asynchronous Receiver/Transmitter), PWM (Pulse Width Modulation) and PM Bus. This project is to power up and power down the PM Bus compatible voltage regulator within the POR specification which is 200 us to 100 ms and achieve 100 ms power down for FPGA. There are a number of advantages using Intel MAX 10 FPGA such as built in ADC, UFM, flexibility of FPGA, and NIOS II soft processor.

ABSTRAK

Pada masa ini, FPGA (Programmable Gate Field Array) adalah salah satu pilihan yang mempertimbangkan untuk rekabentuk sistem digital jika dibandingkan dengan ASIC (Application-Specific Integrated Circuit). Ini adalah kerana fleksibiliti FPGA untuk mengemaskini sistem. Intel Stratix 10 FPGA adalah FPGA dari Intel Cooperation memerlukan penjujukan kuasa yang betul untuk mengelakkan kerosakan pada peranti. Selain kuasa penjujukan, Intel Stratix 10 FPGA perlukan antara 200 us and 100 ms POR (Power On Reset) semasa kuasa dihidupkan untuk mengelakkan FPGA dari menetapkan semula dan sebanyak 100 ms yang perlu dimatikan FPGA. Banyak kaedah kuasa penjujukan dilaksanakan untuk FPGA seperti komponen diskret, pembahagi peraturan perintang, urutan IC (Integrated Circuit), MCU (Microcontroller), CPLD (Complex Programmable Logic Device) dan FPGA. Semua pendekatan ini digunakan untuk mengawal kuasa untuk dihidupkan dan dimatikan kepada pengatur voltan melalui pin bagi membolehkan pengatur voltan dan antaramuka piawai seperti SM (System Management) Bas dan PM (Power Management) Bus. Projek ini, cip tidak meruap Intel MAX 10 FPGA digunakan untuk pengawal pengurusan kuasa voltan. FPGA ini termasuk ADC (Analog to Digital Converter) dan UFM (User Flash Memory) yang kritikal untuk membentuk pengawal pengurusan kuasa. Pengawal pengurusan kuasa akan menggunakan NIOS II dan Avalon-MM (Memory-Mapped) Bas akan menyambung semua ADC, UFM, pemasa, UART (Universal Asynchronous Receiver/Transmitter), PWM (Pulse Width Modulation) dan PM Bus. Keputusan untuk projek ini adalah menguruskan kuasa kepada FPGA dengan PM Bus pengatur voltan serasi dalam spesifikasi POR dari 200 us ke 100 ms dan 100 ms spesifikasi untuk mematikan FPGA. Terdapat beberapa kelebihan menggunakan Intel MAX 10 FPGA seperti dibina pada ADC, UFM, fleksibiliti FPGA, dan NIOS II.

CHAPTER 1

INTRODUCTION

1.1 Background

Analog and digital systems are going complex in the networking, optical transport networks, board cast, military, medical, test instrument, wireless, ASIC prototyping, compute, parallel processing, data centers and storage systems [1-10]. Advance power sequencing, power rail monitoring and fail safe system are required to implement in these applications [11-13]. Advance system board with multiple voltage rails, different interface and signal conversion can be found on these application boards. Intel Stratix 10 FPGA from Intel is the most advance and complex digital device that required on these applications [1, 9, 14, 15]. As these applications required significant cost and critical operation, protection design is an essential in the application board [1]. Mixed signals design is essential for the electronics designer and multiple voltage domain is part of the design in FPGA [17, 18].

Proper power up and power down sequence are required for Intel Stratix 10 FPGA to prevent current surge and it may damage the device. There are a lot of voltage rails need to power up and all these voltages rails are categories into 3 majors group as group 1, group 2 and group 3. Power up sequence of Intel Stratix 10 FPGA must be in the order of group 1 to group 3 and each group voltage must reach 90% of the nominal voltage before powering up the subsequence group voltage. For the power down sequence, the group voltage must be power down in reverse order from group 3 to group 1 and each group voltage must reach 10% of the nominal group voltage before powering

down subsequence group votlage [19, 20] . Beside the power sequence, POR of each voltage rails on Intel Stratix 10 FPGA must be meet as specified by the data sheet from 200 us to 100 ms [2]. During power down sequence, Intel Stratix 10 FPGA required to full turn off the device from group 3 to group 1 in 100 ms [3]. Figure 1.1 and 1.2 are the power up sequence and power down sequence requirement for Intel Stratix 10 FPGA.

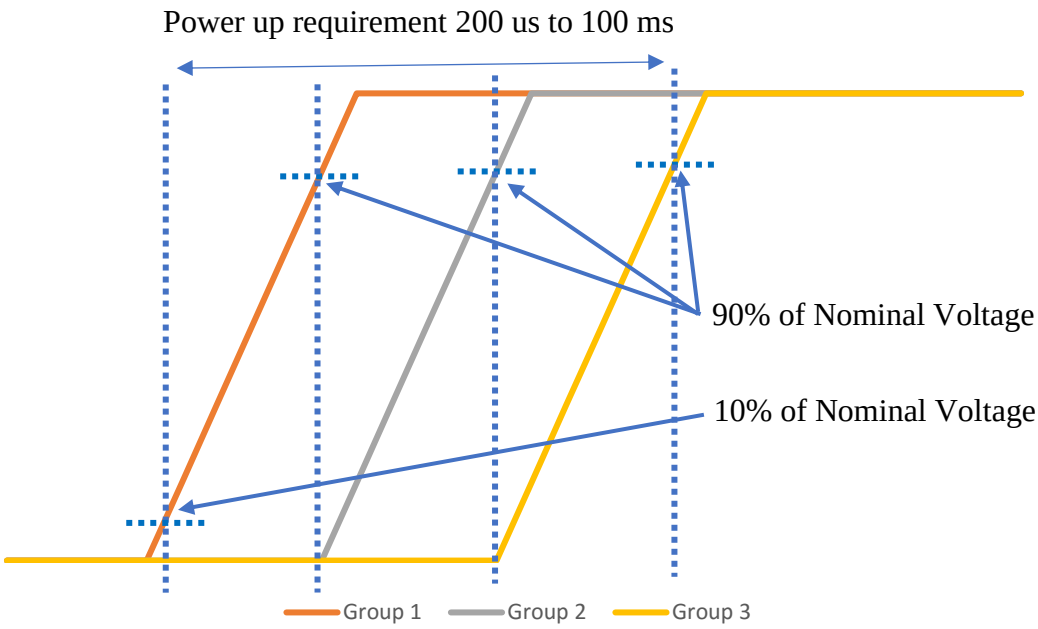

Figure 1.1 Power up requirement for Intel Stratix 10 FPGA

To control on the power sequencing on Intel Stratix 10 FPGA, intelligent system must be developed to overcome the Intel Stratix 10 FPGA voltage rails requirement [3]. Beside precise control on power sequence, intelligent system also requires to monitor the voltage that supply to the Intel Stratix 10 FPGA. Upon the faulty detection, the intelligent system also need to do the fault recover to prevent the damage to the Intel Stratix 10 FPGA [1].

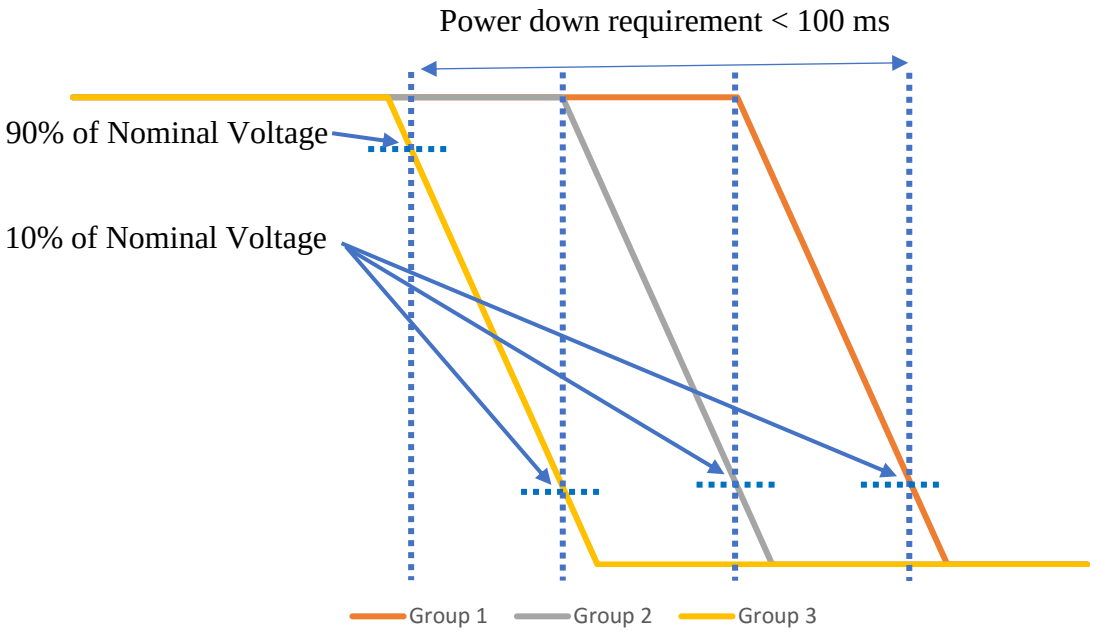

Figure 1.2 Power down requirement for Intel Stratix 10 FPGA

1.2 Problem Statement

FPGA implementation on application board is required to use proper power sequencing as the growing of the FPGA adoption in recent year [4]. There are no exception for Intel Stratix 10 FPGA that required proper power sequencing [3].There are a lot of methods used for power sequencing on FPGA such using discrete component, cascading PGOOD pin into enable pin on voltage regulator, power-up sequencing with a multi-output reset IC, implementation of an analog up/down sequencer, implementation of delay on power switches and digital system health monitors with PM Bus interface [5, 6].

Previously, CPLDs are one of the device that commonly used for control path application such as power sequencing. CPLDs have the instant-on, multicore, lowest cost per I/O and re-programming ability feature that allow on this usage [23, 24]. Due

to density of CPLDs, it is not possible to design a power management controller in the CPLD [7]. FPGA can be one of the option to implement power management controller. Due to the nonvolatile SRAM of FPGA, external flash memory is required to store the FPGA configuration file [8]. By adding SRAM to the board, this is going to increase the overall board component count and cost [9].

1.3 Objectives

The aim of this dissertation is to design, implement and evaluate the power management controller for Intel Stratix 10 FPGA by using Intel MAX 10 FPGA [10]. Intel MAX 10 FPGA is the first Intel FPGA built in analog to digital convertor and non-volatile flash into single package [29, 30]. Power management controller is developed to meet the Intel Stratix 10 FPGA standard POR requirement. To realize the power management controller for FPGA by using Intel MAX 10 FPGA, the following objectives are adopted:

i. To implement power management controller by using Intel MAX 10 FPGA development kit and Intel Enpirion PowerSoC Evaluation Kit
ii. To implement soft microprocessor NIOS II in order to achieve power up and power down sequence
iii. To characterize and analyze the performance of the propose power management controller

1.4 Scope

This project is focus on the implementation of power management controller design in single chip solution Intel MAX 10 FPGA. Voltage regulator is controlled via PM Bus

and voltage regulator that used enable pin or PWM for controlling the voltage regulator is supported. This project is implemented by using 3 analog channels to monitor the voltage on 3 voltage regulators. In this project, the power management controller design is based on Intel MAX 10 FPGA, custom cooling fan for Intel MAX 10 FPGA and Intel Power Solutions EM2130 PowerSoC Evaluation board [10, 11]. The output voltage of PowerSoC evaluation boards are preset and ranging from 0.9 V – 1.2V [12]. This design only support for standard POR for Intel Stratix 10 FPGA.

1.5 Research Contribution

This project is developed to contribute the power sequencing requirement, monitoring and logging for Intel Stratix 10 FPGA [3]. By using single chip FPGA, the power management controller can be implemented and supported PM Bus protocol based on I2C interface [13]. The single chip Intel MAX 10 FPGA that included on chip UFM and ADC allow the overall component count reduction and signal integrity design effort on the printed circuit board [28-30].

1.6 Thesis Outline

This thesis is organized in 6 chapters. Below is the distribution on the chapter for this thesis

Chapter 1 includes the background, introduction, scope and research contribution on power sequencing, monitoring and logging. This chapter also discuss on Intel Stratix 10 FPGA power requirement. It also discusses on different power sequencing approach.

Chapter 2 discusses on the literature review and mainly consist of the method that previously done on power sequencing. It also includes the devices that previously used to control the power sequencing by CPLD and microcontroller. This chapter also discuss about methods can be used to control the voltage regulator by using enable pin, PWM, PM Bus and other interface signals.

Chapter 3 introduces the hardware specification, requirement to implement into the power management controller. It is also cover the software specification and requirement for the power management controller. This chapter included the detail information on the communication protocol PM Bus for power module communication. Beside communication protocol, voltage monitor and fault line detection are also discussed in this chapter. Finally, the algorithm on the power management controller is part of this chapter.

Chapter 4 is going to evaluation the power management controller. This chapter is included the power sequencing, fault line detection, fault line logging, voltage monitoring and user command configuration. Power sequencing on voltage regulator output is captured by oscilloscope. As for the fault line detection, logging and voltage monitor can evaluate through the user command by using TeraTerm. This chapter is also compare the single chip solution FPGA with other power sequencing method.

Chapter 5 is the conclusion on the power management controller and feasible implementation on power management controller on future Intel Stratix 10 FPGA board. This chapter will list the possible future work can perform on the power management controller.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Traditionally, the power sequencing on the FPGAs are using discrete and passive component such as resistor, capacitor and diode. By using discrete and passive component, precision delay on power sequencing is harder to control. The other method that used for power sequencing is by using resistor divider rules. By using resistor divider rules, multichannel supplies device such as ADP5134 can be sequence by connecting attenuated version of the regulator's output to the next enable pin of the regulator [14].

The most common and easy method to implement power sequence is using power sequence integrated circuit [4]. The delay of sequence is preset in the power sequencing IC and the delay is used to control the enable pin of the voltage regulator [15]. The voltage regulator can turn on by set high state to the enable pin and set low state to turn off the voltage regulator. As it lacks user control preset delay and number of control pins on power sequence IC, the other intelligent method is using microcontroller to control the power sequencing on enable pin on voltage regulator [16].

Another method that use for the power sequencing is by using CPLDs. For this method, CPLD is configured to work as sequencing IC and this is going to improve the user define delay for each voltage regulator [9]. Since CPLD have more I/Os, the method is required less component for the power sequencing on FPGA.

Multiple ways of power sequence method had been discussed from pin enable power regulator, sequencing integrated circuit, and power system management [4, 14, 15, 17]. Some of the design on the power management by adopting open standard protocol PM Bus [13, 18]. Before using the PM Bus as the power management open standard protocol multiple serial buses are compared such SM Bus, Ethernet, SPI, RS 485 RS 232, and CAN Bus [37, 38]. The implementation of the PM Bus required external master controller to manage the power management system [19].

Based on the reading from other research, it does mention a lot of methods on power sequence and monitoring the power supply line by using ADC. There are also propose on intelligent energy management by using digital power control method or digital power management method [17]. Multiple POL technique stack up by using FPGA to control the voltage regulator and implemented as power management [20]. For cases that design the PM Bus slave digital power management does exist. The design is use the slave controller to management the voltage regulator and this design do require a master controller [21].

2.2 Implementation of Power Up and Down Sequence, Voltage Monitor and Fault Report

Intel Stratix 10 FPGA is a new FPGA that required power sequencing which simple not many solutions offered in the market. Below is the sub section that highlight on the different power sequence, voltage monitor and fault report technique implemented to manage the power on FPGA.

2.2.1 Passive discrete components

The most common technique used for sequencing is by combination of the passive components such as resistor, diode and capacitor. Figure 2.1 is one of the technique that using resistor and capacitor to slow down the ramp rate. This design technique is used together with the pin enable voltage regulator and it only supported power up sequence [4]. Besides that, this design is not able to meet Intel Stratix 10 FPGA requirement during power up sequence as it required 90% of the nominal voltage on each rail before powering up another voltage group. This method is only work on power up sequence but not the desired power down requirement for Intel Stratix 10 FPGA. It also does not support the voltage read back and faulty logging functionality.

Another approach using resistor divider rule to control the power sequencing. For this approach, this design is using multichannel supplies voltage regulator (ADP5134) that have multiple enable pin for each regulator. Based on this design, the voltage regulator can be turn on and turn off sequentially [14]. But the turn off method on this design cannot be implemented in Intel Stratix 10 FPGA as it violated the reverse power down sequence requirement. Besides that, this design also does not monitor the output voltage during power up and power down. Figure 2.2 is the implementation of power up and power down sequence by using ADP5134 with resistor divider rule.

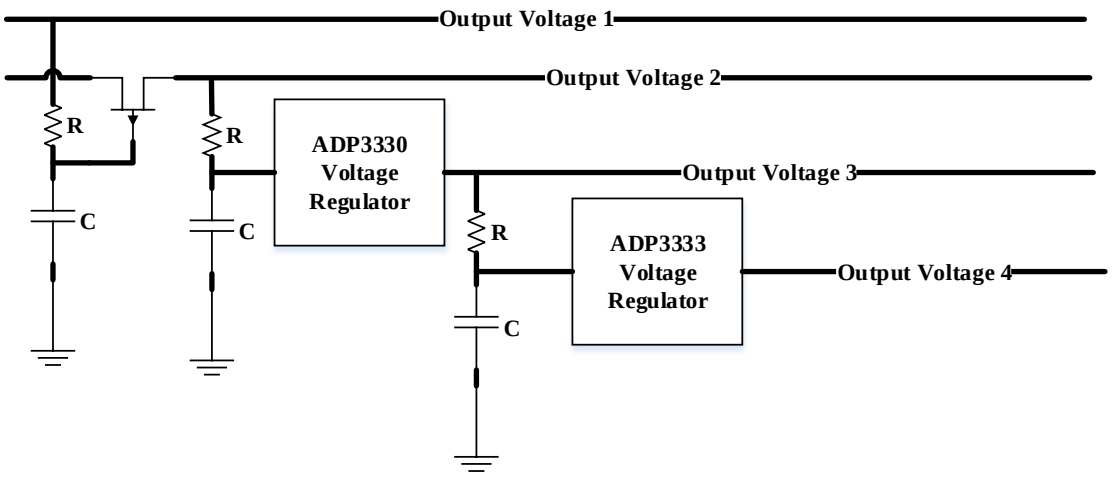

Figure 2.1 Implementation of power sequence using resistor and capacitor

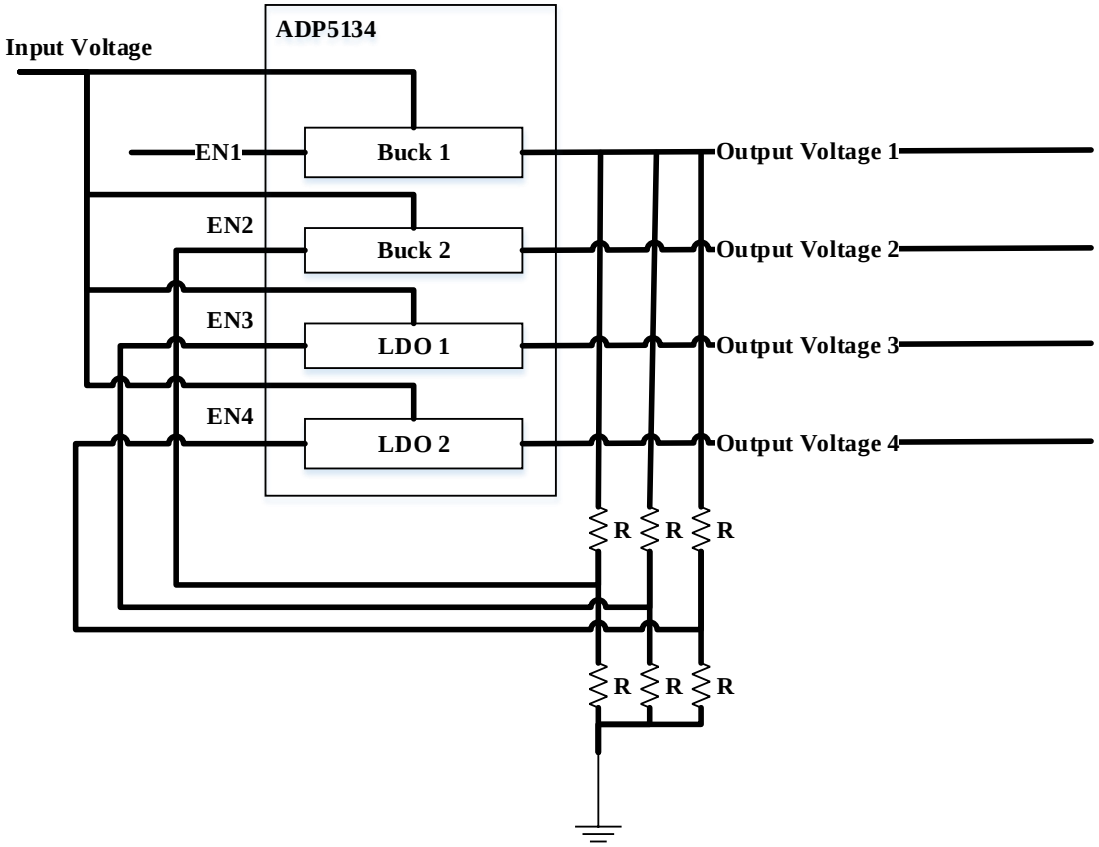

Figure 2.2 Implementation of power sequence using resistor divider rule

Last approach of using passive and active is by using the combination of resistor, capacitor and diodes. This design also used the pin enable voltage regulator to achieve power up and power down sequence. The desired value of the delay can be controlled

by varying the value of resistor and capacitor value [14]. By using this method, precise delay control of the delay is hard to achieve as the resistor and capacitor value can be varies by temperature and manufacturing process. This design also not able to meet the power down requirement of Intel Stratix 10 FPGA and it does not support voltage monitoring and faulty logging. Below is the Figure 2.3 shown on the implementation of resistor, capacitor and diode to form the passive delay network.

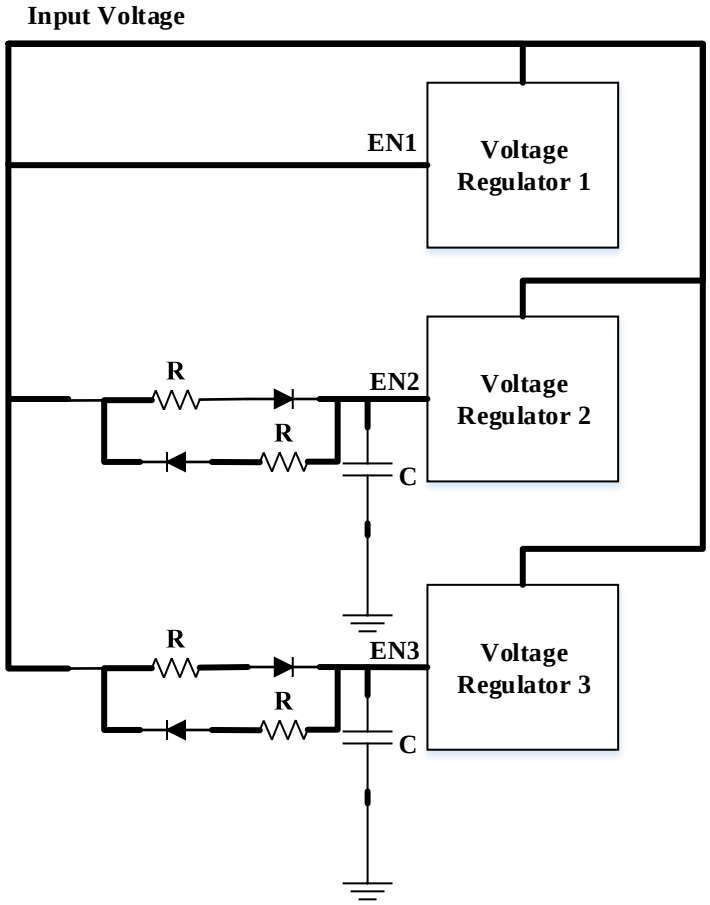

Figure 2.3 Implementation of power sequence using passive delay network

2.2.2 Sequencing IC

Beside using the passive components as power sequencing, another method that use for voltage sequencing by using the sequencing IC. There are 3 types of sequencing IC that

commonly use simple sequencer, sequencer with voltage monitoring and sequencer with build in voltage monitoring.

The first sequencer method that implemented is by using LM3880, this device has 3 output per device and the delay is preset based on the part number that user required. Figure 2.4 is the typical method that implemented for power sequence. For this design is easier to implement compare to using ADM1086 as there is no external temperature and process variation capacitor and no software development required to use this device [5]. This device also support power up and power down sequence that match with Intel Stratix 10 FPGA. For this approach to use for Intel Stratix 10 FPGA, there are few drawbacks such as the maximum enable port for the sequencer, manufacturer preset delay and number of sequencer required. All these drawbacks will cause the board design effort, board size and component counts.

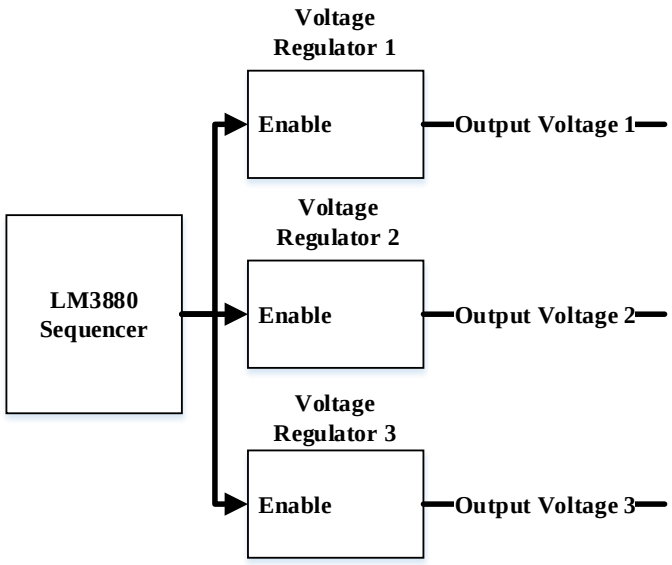

Figure 2.4 Basic implementation of power sequence using sequencing IC

Another method simple sequencer approach, the delay of each voltage rail is control by individual sequences IC and the delay for each sequencer is determine by

the external component. For ADM 1086, the delay of the device is controlled by the capacitance of the capacitor. Figure 2.5 shown the implementation of power sequence by using sequencer IC with external voltage monitor IC. This design method is using sequencer and external voltage monitoring IC to achieve accurately and reliability of power sequencing [4]. By using external voltage monitoring, the sequencer is only start if the known good voltage is detected. This approach is generally not able to implement in Intel Stratix 10 FPGA as the power up and power down delay is controlled by external capacitor. Process and temperature variation on the external capacitor will cause the inconsistent of the delay. This will cause the Intel Stratix 10 FPGA do not power up correctly. Based on this design, voltage rail is using one sequencer with a voltage monitoring IC and this will increase the board design complexity as well as increase the component counts on the board. Two of these factors will cause cost and board size increase.

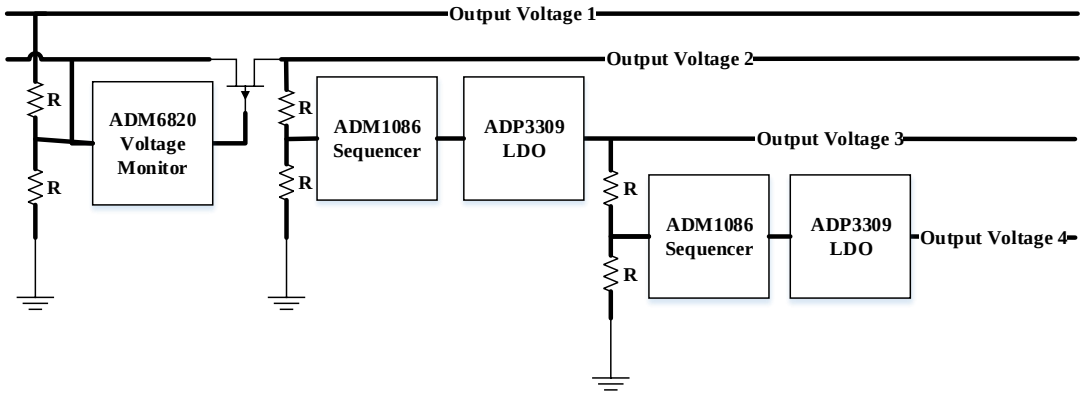

Figure 2.5 Implementation of power sequence using sequencing IC and voltage monitor IC

For design that used more complex sequencer with build in voltage monitor, the sequencer ADM 1060 is the centralize device that control the others voltage regulator by toggle the pin enable voltage regulator as in Figure 2.6. This device included the

voltage monitoring for fault detection. Beside this, it also able to do power up and power down sequence by using the programmable delay block. The delay for each channel is predefined by the programmable delay block. By using this design, user can only access the predefine delay on the device and during power up and power down sequence the voltage rail is not monitor by the sequencer. For this approach, the designer also needs to use at least 3 ADM1060 to cover all the voltages used by Intel Stratix 10 FPGA as 2 of the channels for voltage supervisor on this device only work with negative voltages. ADM1060 is built in with EEPROM for device configuration on sequencing but it does not use for logging purpose [22]. There is also a drawback in this design approach that the sequencer only turn off the voltage rail that fault detection which is violate the power sequence on Intel Stratix 10 FPGA.

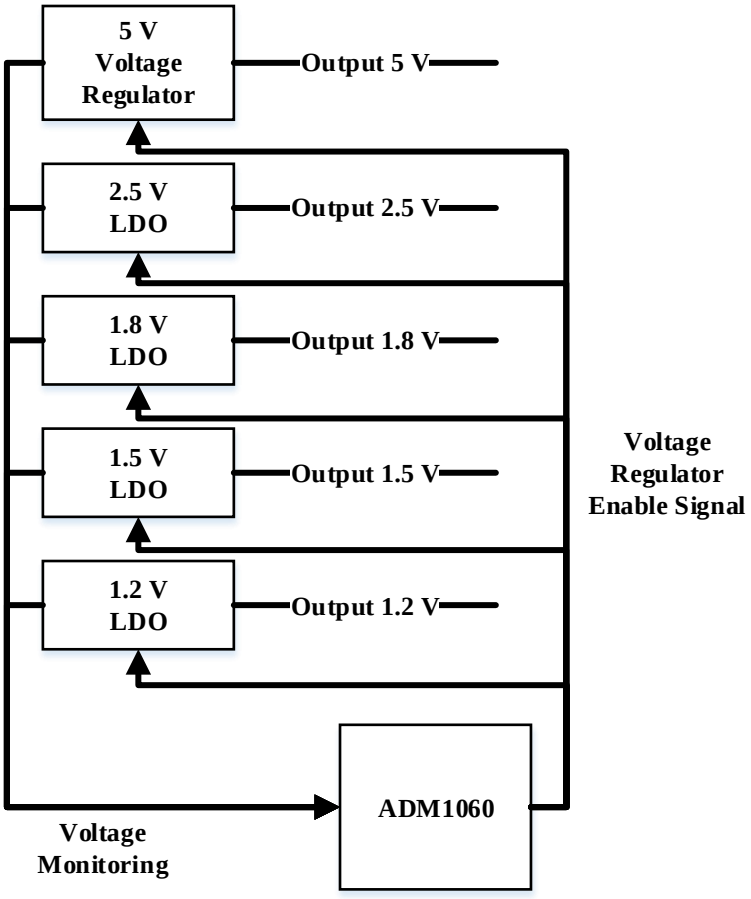

Figure 2.6 Voltage sequence design by using sequence with built-in voltage monitor

2.2.3 MCU

In MCU design approach, MCU is the master controller that use to control the FPGA based slave device via PM Bus. The FPGA is a slave controller that manage the pin enable voltage regulator. For this approach, it is required to develop the firmware for MCU and digital design on FPGA. For MCU development, the designer required to define the PM Bus command to use in this project and implementation of the delay for each voltage rails. As for FPGA development, designer is developing the instruction sets supported by PM Bus specification [21]. This approach is only focus on development of PM Bus compatible controller which can be replace by Intel Enpirion PowerSoC EM2130 voltage regulator. This design is also incurred additional cost and time for both MCU and FPGA such as development time, development tools and external flash device to store FPGA configuration. Figure 2.7 below is the implementation on this project by using MCU.

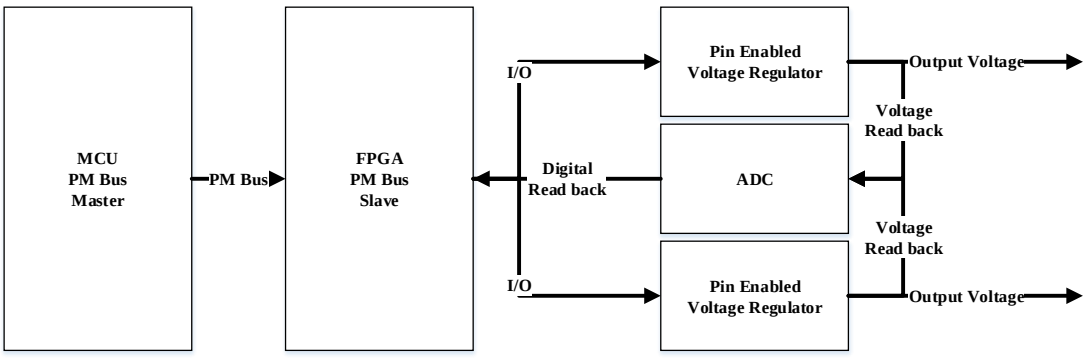

Figure 2.7 PM Bus implementation of voltage sequencer by using MCU and FPGA

Another simpler approach is using MCU to direct control the sequencing. For this method, the MCU GPIOs are connected directly to the pin enable voltage regulator as Figure 2.8. This is enabling the MCU to control both the power up and power down

sequence by firmware development. MSP430 is a 16-bit MCU that used to control sequence of the voltage rail based on time or voltage through ADC [16]. For this design, it is only worked on pin enable voltage regulator and no faulty logging for any failing output voltage. Without PM Bus implemented, MCU is not able to manage the functionality of the voltage regulator such as voltage adjustment, voltage feedback and temperature of voltage regulator.

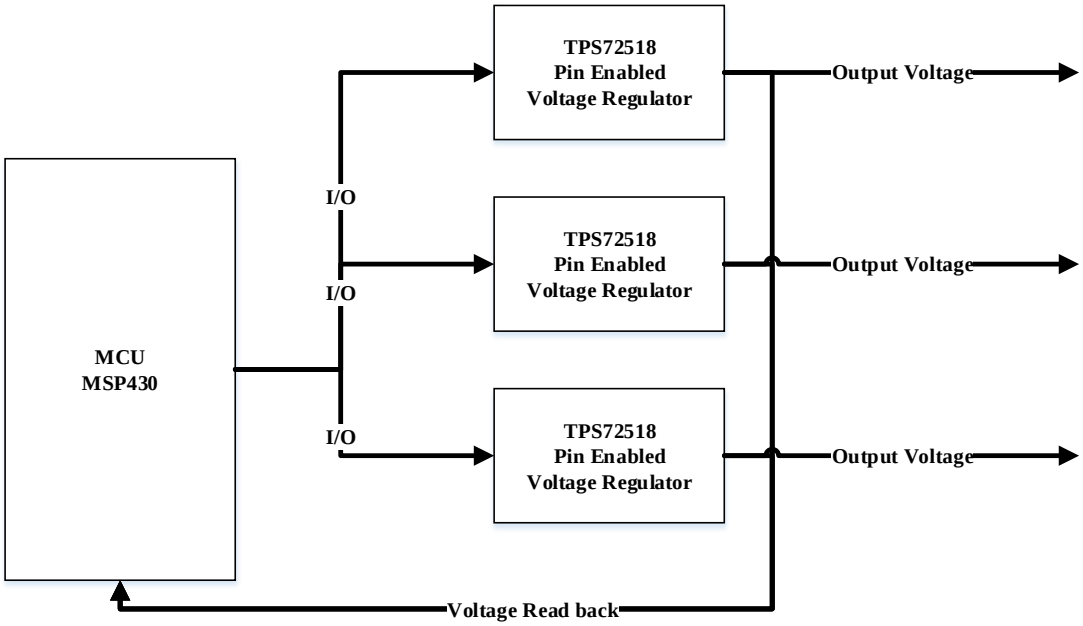

Figure 2.8 Simple MCU implementation of power sequencing

2.2.4 CPLD

CPLD is one of choices that used for power sequencing as CPLD is a multi-voltage system, non-volatile and instant-on device. CPLD control the voltage regulator by toggle the on and off on pin enable voltage regulator. The additional design added for this approach is hold the CPU, FPGA and ASSP to reset state using CS. Lastly, the design also utilizes the JTAG port for monitoring power sequence and storing errors in programmable power supply [8]. For this approach, CPLD can perform voltage

monitoring and faulty data but it is fully depended on the respond from the programmable power supply. Designer will need to develop the protocol that support the communication between CPLD and programmable power supply using RTL. Figure 2.9 is shown general implementation of CPLD for power sequencing.

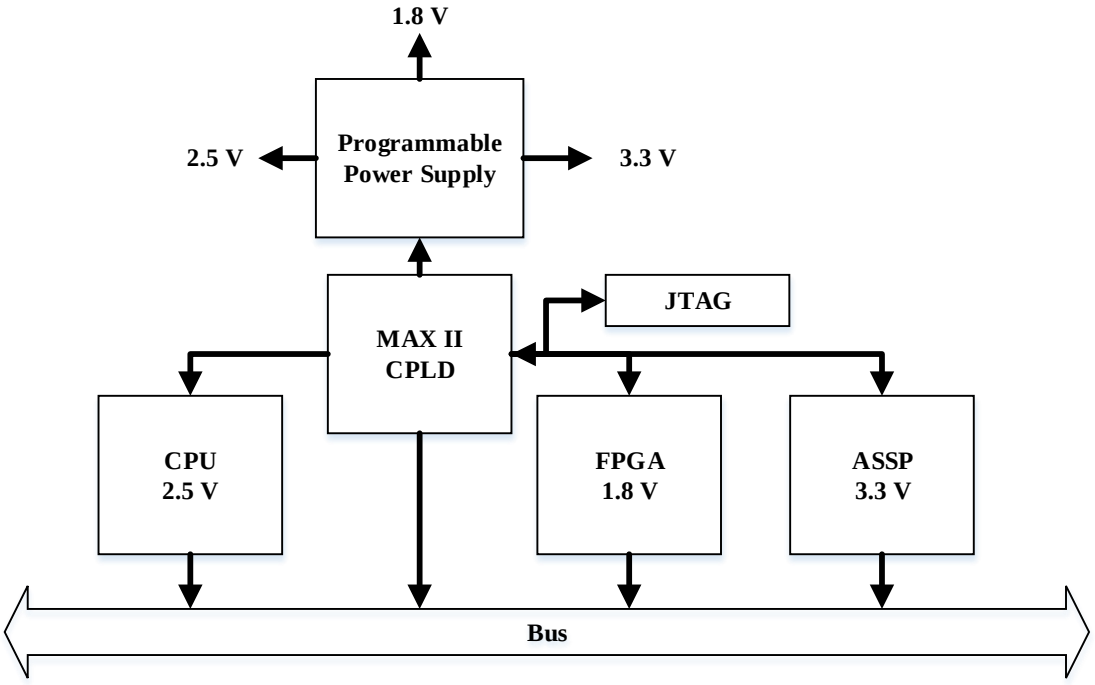

Figure 2.9 Power sequencing by using CPLD

2.2.5 FPGA

FPGA can configure to perform power up and power down sequence for Intel Stratix 10 FPGA. For this design, designer chose the POL and connected it to the I/O pins of the FPGA to enable power up and power down sequence. Based on this method, POL is a pin enabled voltage regulator and designer needs to precise control the POL by toggle the I/O pins of FPGA to turn on and off the POL. The output of POLs is monitor by the serial ADC and process by FPGA [20]. Based on this approach, the system is not able to log on faulty voltage as it does not implement flash memory and using FPGA

as power management controller is required external flash memory to store the FPGA configuration. Figure 2.10 is the implementation of FPGA in power sequencing.

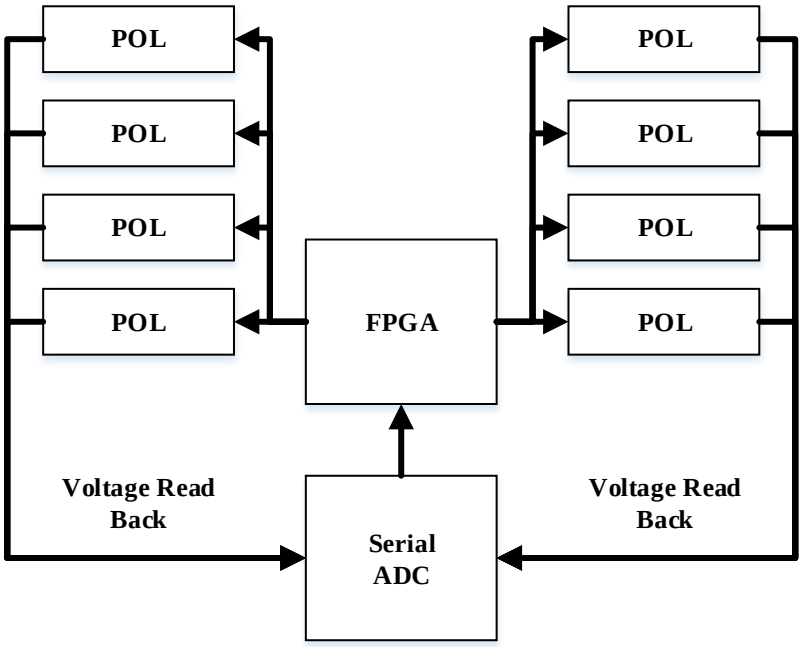

Figure 2.10 Implementation of power sequencing using FPGA

2.3 Summary

Based on the research study so far, most of the design and approach that found hardly focus on the power sequence, power monitor and faulty detection with logging feature. For the power sequence, the design only focus either on power up or power done only. Most of the design done previously are not able to implemented for Intel Stratix 10 FPGA. A lot of design that done previously only work on voltage monitor during supply stage but not the during the power up and power down real time monitoring. As for the logging feature, there is no implementation for faulty logging for future enchancement. There is also no implementation of the non-volatile single chip solution FPGA to implement power manage controller. This is the good opportunity to deliver the possibility of power management controller concept for Intel Stratix 10 FPGA designer

to ease the power management design. Below is the summary on different power sequencing, voltage monitor, fault detection and fault logging method that adopted.

Table 2.1 Comparison of different system on power sequencing, voltage monitor and logging

	Discrete Component [12, 22]	**Resistor Divider Rule [14]**	**Sequencing IC [11, 13, 22]**	**MCU [28, 35]**	**CPLD [23]**	**FPGA [20]**
Power Up Sequencing	Yes	Yes	Yes	Yes	Yes	Yes
Power Down Sequencing	No	No	Yes (Limited)	Yes	Yes	Yes
Voltage Monitor	No	No	Yes (Require MCU for interface)	Yes, internal ADC	No	No
Fault Detection	No	No	Yes (Require MCU for interface)	Yes, depend on ADC readback	No	No
Fault Logging	No	No	Yes (Require MCU for interface)	Yes, depend on flash memory size in MCU	No	No

CHAPTER 3

METHODOLOGY

3.1 Introduction

Power sequencing, voltage monitor, fault detection and faulty logging feature are implemented on power management controller for Intel Stratix 10 FPGA. As mentioned previously, a lot of methods can be implemented to manage the power on the FPGA. For this project, power management controller is the main core to management the power system for the Intel Stratix 10 FPGA. To achieve this, Intel MAX 10 FPGA is selected as the single chip solution FPGA to manage the power for the Intel Stratix 10 FPGA. Figure 3.1 show the complete flow implemented in this project.

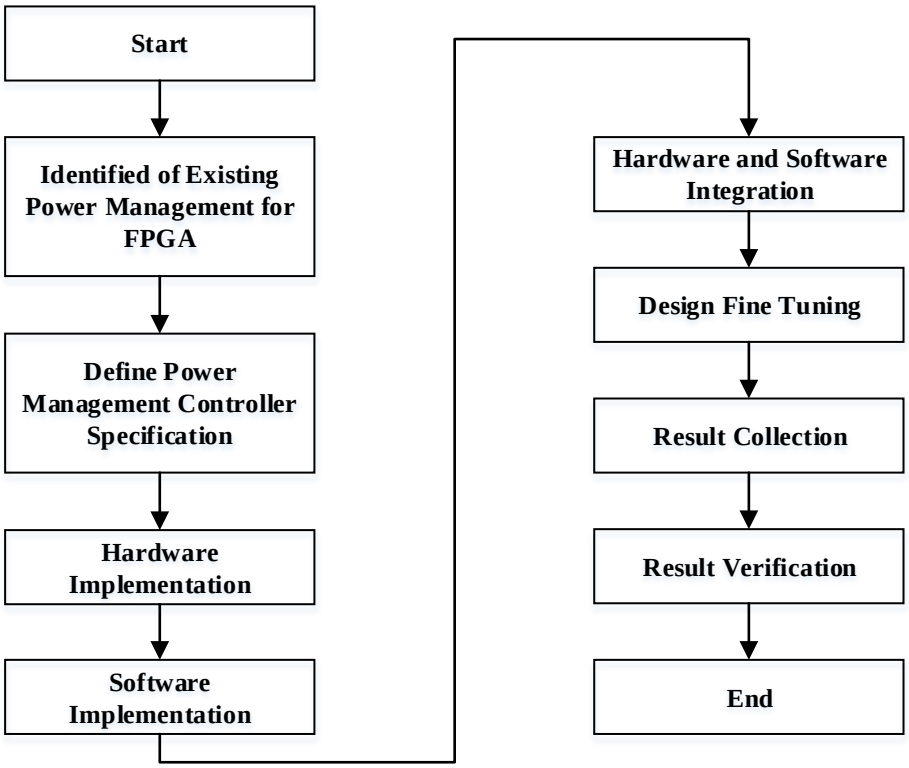

Figure 3.1 Complete design flow for Power Management Controller

In this project, 2 major developments are carried out to implementation of power management controller for Intel Stratix 10 FPGA. First part of the development is hardware implementation in session 3.2. This part is going through selection of hardware require for this project such as single chip solution FPGA, FPGA development kit, power module board, cooling system, external component and connectivity among boards. In the second part of the project, is the development of software for FPGA soft processor. The software part is involving the building system in the power management controller such as the building block of software microcontroller, program flow, voltage monitor method, logging functionality and protocol implementation.

3.2 Hardware Implementation

Power management controller is the central controller that management the power in the system board before, during and after powering the Intel Stratix 10 devices. Before powering up the Intel Stratix 10, power management controller must monitor each power supply line and initialize peripherals include fan rotation speed and flash memory availability. During power up Intel Stratix 10 device, power management controller must monitor each power supply meet the Intel Stratix 10 power up requirement such as the 90% of each power supply group before going to next power supply group. There is another important function that power management controller must achieve is to power up the Stratix 10 device within the POR specification [3]. The POR specification is based on the data sheet on the Intel Stratix 10 FPGA if the power management controller fail to meet the POR requirement then the Intel Stratix 10 FPGA will not able to power on correctly [2]. After the power up the Intel Stratix 10 FPGA,

power management controller must monitor the power supply from time to time if any unexpected condition that arise. Beside power up sequencing, the power management controller also need to have the power down sequencing from group 3 to group 1. The power management controller also programmed to monitor the temperature on the controller itself. Any unexpected temperature rising on the power management controller. The cooling fan is spinning to cool down the power management controller based on the PWM output from the FPGA pin.

Power management controller is the main core to management the power system for the Intel Stratix 10 FPGA. To achieve this, non-volatile Intel MAX 10 FPGA is selected as the core single chip solution FPGA to manage the power for the Intel Stratix 10 FPGA. Figure 3.2 is example that can use Intel MAX 10 FPGA as a power management controller to management the voltage rails in Intel Stratix 10 FPGA.

Intel MAX 10 FPGA is the complete solution that fit the voltage regulator communication, voltage monitoring, fault logging and fault recovery. Another advantage of using Intel MAX 10 FPGA is that no external flash memory needed for the configuration like SRAM based FPGA. The Intel MAX 10 FPGA have the instant on feature that allow configuration file store in the internal flash memory to configure the FPGA SRAM [10].

Voltage sequencing implementation is achieved by controlling the voltage through PM Bus to PM Bus compliance voltage regulator. For the voltage monitor, this is done by using build in ADC inside Intel MAX 10 FPGA [24]. Lastly, the logging

function is implemented using the flash memory embedded inside the Intel MAX 10 FPGA [25].

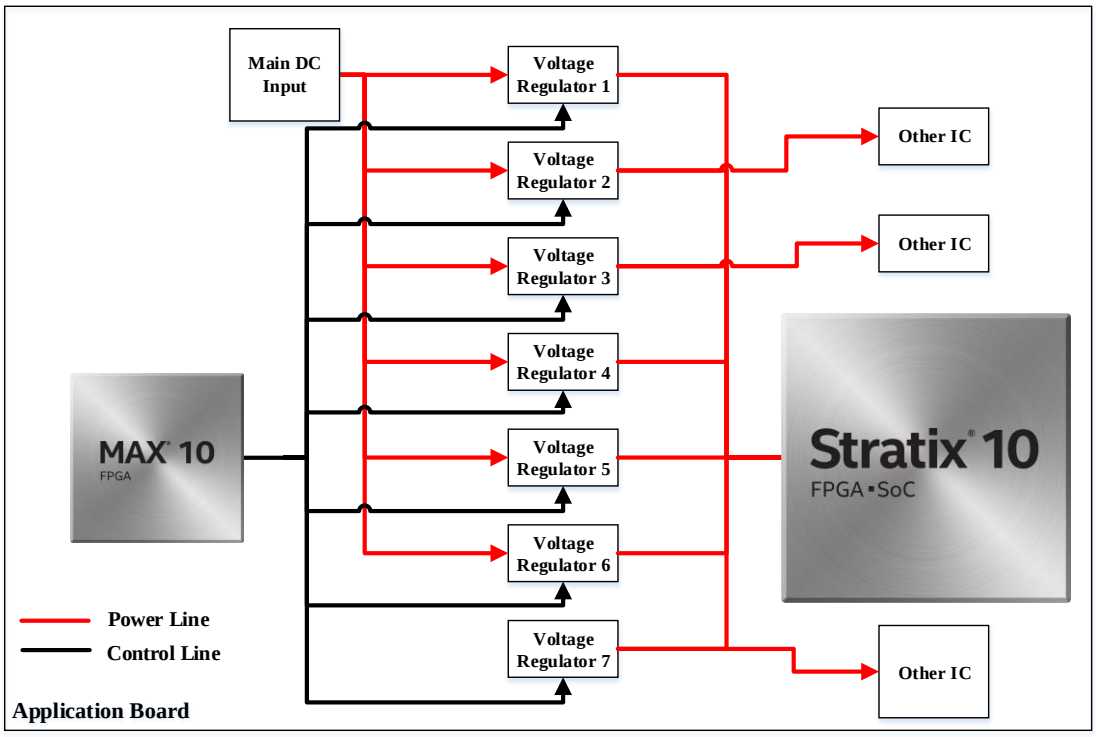

Figure 3.2 Example of the power distribution network for Intel Stratix 10 FPGA and Intel MAX 10 FPGA by using Power Management Controller

The power management controller is master device that using the PM Bus for the voltage regulator communication [13, 18, 26]. Voltage regulator is the slave devices that receive command from the master controller. The power management controller is used to control the on and off on pre-assign address on voltage regulator through PM Bus. For this project, PM Bus is one of the protocol that leverage on I2C and by running at the 400KHz based on PM Bus 1.2 specification [32, 36, 41-44]. PM Bus is the open standard that use to control, configure and monitor power supplies on voltage regulator [26]. PM Bus is working as master to multiple slave addresses that use to management on the power system. SCL, SDA, CONTROL and ALRT are the signals that based on

PM Bus specification. SCL is the clock signal that clock from master to slave device. SDA is the bidirectional data line as for the ALRT is alert line for the slave device to notify on faulty to master. CONTROL line is the optional pin to control the voltage regulator [13, 18, 26]. Figure 3.3 show the protocol that implemented in PM Bus. For PM Bus to turn on and off voltage regulator, PM Bus need to send the slave device address follow by OPERATION (0x01) command and last data byte to turn on (0x80) and off (0x40) the voltage regulator.

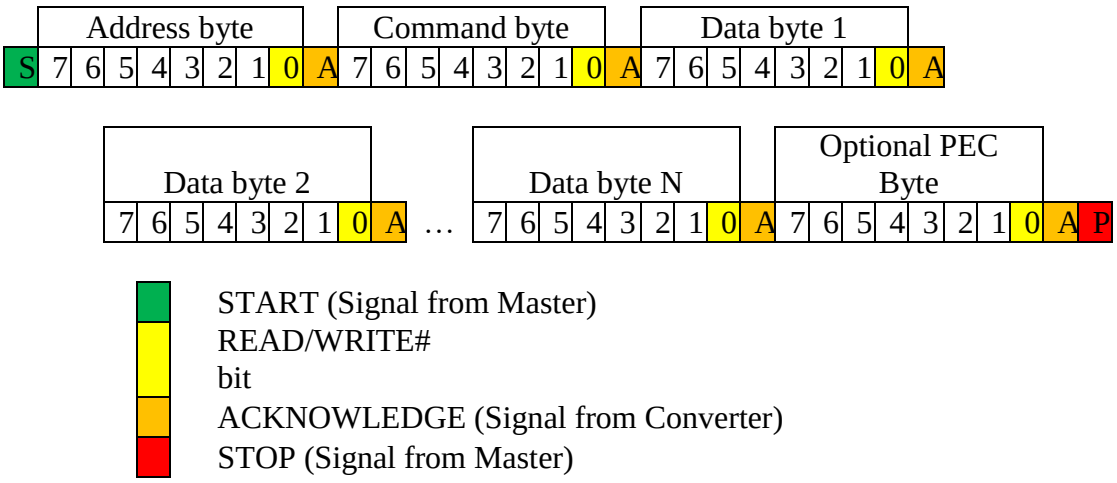

Figure 3.3 PM Bus Protocol

ADC in the power management controller is use to capture the analog voltage in each power supply line. These data is either be used as the power sequence or voltage monitor. 16 channels ADC port is connected directly to the power supply line depend on the usage in the design [24].

UFM in the power management controller is used to log the fault supply line information [25]. Over voltage, under voltage and temperature on the power management controller are stored in the user flash memory. The stored information can