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EXPERIMENTAL AND NUMERICAL STUDIES OF TRANSIENT HEAT
TRANSFER IN ELECTRONICS PACKAGING

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EXPERIMENTAL AND NUMERICAL STUDIES OF
TRANSIENT HEAT TRANSFER IN ELECTRONICS
PACKAGING

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**EXPERIMENTAL AND NUMERICAL STUDIES OF TRANSIENT HEAT
TRANSFER IN ELECTRONICS PACKAGING**

by

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**Thesis submitted in fulfillment of the
requirements for the degree
of Doctor of Philosophy**

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LIST OF ABBREVIATION

ANN	Artificial Neural Networks
AWE	Asymptotic Waveform Evaluation
BCI	Boundary Condition Independent
CFD	Computational Fluid Dynamics
CTE	Coefficient of Thermal Expansion
CTM	Compact Thermal Models
FEM	Finite Element Method
FHP	Flat Heat Pipe
FNM	Flow Network Modeling
GA	Genetic Algorithms
IC	Integrated Circuit
JEDEC	Joint Electron Device Engineering Council
LMA	Low Melting Temperature Alloy
MPSoC	Multi-processor System-On-Chip
NetDAQ	Networked Data Acquisition Unit
PCB	Printed Circuit Board
PDR	Pitch-to-diameter Ratios
PSO	Particle Swarm Optimizers
QFP	Quad Flat Package
RC	Resistor-Capacitor
TIM	Thermal Interface Material
TSI	Through Silicon Interposer
TSV	Through Silicon Via

VAT	Volume Average Theory
VCTIM	Vertical Carbon Thermal Interface Material
VPS	Virtual Power Source
TDI	Transient Dual Interface

LIST OF SYMBOLS

C_p	Specific heat J/KgK
dT/dx	Temperature gradient
h	Heat transfer coefficient $W/m^2.k$
k	Thermal conductivity W/mK
P	Device power W
Q	Heat Flux W/m^2
q^n	Convective heat flux w/m^2
R_{bd-a}	Thermal resistance board to ambient C^0/W
R_{j-bd}	Thermal resistance junction to board C^0/W
R_{c-p}	Thermal resistance chip to package C^0/W
R_{jc}	Thermal resistance-junction to chip C^0/W
R_{j-sink}	Thermal resistance junction to sink C^0/W
R_{pa}	Thermal resistance from package to ambient C^0/W
R_{sink-a}	Thermal resistance sink to ambient C^0/W
T_a	Ambient temperature 0C
T_{ball}	Solder ball temperature 0C
T_j	Junction temperature 0C
T_{max}	Maximum temperature 0C
T_s	Surface temperature 0C
T_∞	Fluid temperature
u	velocity in x direction m/s
v	velocity in y direction m/s
Θ_{sa}	Thermal resistance- heat sink to ambient C_0/W

Θ_{ja} Thermal resistance- junction to ambient C_0/W

PENGAJIAN EKSPERIMEN DAN SIMULASI PEMINDAHAN HABA FANA DALAM PAKEJ ELEKTRONIK

ABSTRAK

Permintaan bagi peranti mudah alih dan tablet adalah tinggi pada setiap masa dalam dekad yang lalu, perhatian yang amat menggalakkan telah ditumpu kepada bidang ini. Sesuatu kajian yang baru diperlukan dalam industri untuk mengiringi permintaan ini adalah untuk mengkaji ciri-ciri pemindahan haba sementara dan keadaan mantap, untuk memahami prestasi pemindahan haba yang memuaskan ke atas alat-alat ini, dan memastikan masa ujian haba untuk chip yang sesuai dengan output pengeluaran yang lebih baik. Fasa pertama kajian ini membentangkan keadaan mantap paksaan udara simulasi haba dengan lampiran penyebar haba untuk keadaan dengan pelbagai kuasa di dalam cip (0.5W-2.0W). Model haba keadaan mantap telah berjaya dibangunkan dan dioptimumkan, dan kontur haba bagi setiap kuasa chip telah ditunjukkan. Model simulasi haba telah disahkan dengan pendekatan eksperimen dengan suhu simpangan dalam perbezaan peratusan pada 6.02%. Model haba yang disahkan telah dilanjutkan untuk mencirikan kesan daripada pelbagai aliran udara ke atas rintangan haba dari cip ke ambien. Ia menggunakan rangkaian rintangan haba dan simulasi secara holistik untuk analisis terma yang tepat. Keputusan menunjukkan bahawa rintangan haba dari cip ke ambien adalah fungsi aliran udara tetapi bukan kuasa cip, aliran udara yang lebih tinggi akan mengurangkan rintangan haba dari cip ke ambien. Dalam kajian ini, rintangan haba minimum diperolehi pada $5.9^{\circ}\text{C} / \text{W}$ untuk aliran udara maksimum. Kajian seterusnya telah dilanjutkan kepada simulasi pemindahan haba sementara, dengan tujuan untuk memahami apakah sumber haba bantuan yang diperlukan untuk suhu simpangan mencapai 70°C dalam mod pemindahan haba sementara? Sumber haba bantuan ini adalah penting dalam

mengurangkan masa ujian chip. Pengetahuan yang mencukupi mengenai laluan pemindahan haba sementara telah ditunjukkan melalui penciptaan kontur haba dengan pelbagai sumber haba. Satu prototaip bantuan sumber haba telah berjaya dibina dan dikaji untuk membantu mengurangkan masa ujian haba untuk chip. Dan model pemindahan haba sementara juga telah disahkan dengan pendekatan eksperimen, keputusan simulasi pemindahan haba sementara dalam aspek masa yang diperolehi terletak dalam 11% daripada nilai eksperimen yang mengukur. Data menunjukkan ia memerlukan 22W sumber haba bantuan dan mengambil masa 69.65s untuk suhu simpangan mencapai 70°C daripada suhu bilik, in adalah satu pencapaian yang amat penting yang boleh digunakan dalam pengeshan chip. Kajian mengenai model pemindahan haba sementara disahkan juga dengan kesan pelbagai masa pemindahan haba sementara (15s - 75s) dan sumber haba (7W - 27W) untuk rintangan haba dari simpangan ke pateri bola. Rintangan haba dari cip ke pateri bola adalah fungsi masa sementara, di mana rintangan haba dari cip ke pateri bola meningkat dengan masa sementara; walau bagaimanapun, pada bila-bila masa tertentu rintangan haba tidak akan berubah dengan pelbagai sumber haba.

EXPERIMENTAL AND NUMERICAL STUDIES OF TRANSIENT HEAT TRANSFER IN ELECTRONICS PACKAGING

ABSTRACT

The demand for mobile and tablet devices is at all time high for the last decade, overwhelming attention has been paid to this field, the novelty studies that needed in industry to accompany this demand is to characterize the steady state and transient studies for satisfactory thermal performance on these devices, and ensuring reasonable thermal qualification time for chip and better production outputs. The part one of this study presents the steady state forced air thermal simulations with the attachment of heat spreader for various die power conditions (0.5W to 2.0W), the steady state thermal model has successfully been developed and optimized, and thermal contour for each die power was demonstrated. The simulated thermal model at steady state has been verified by thermocouple-measured junction temperature, with the maximum percentage difference at 6.02% only; the verified thermal model has been extended to characterize the thermal impacts of the various air flows on the resistance from die to the ambient. It utilizes heat path resistance network and simulation in a holistic manner for accurate thermal analysis. The results show that the heat path resistance from die to ambient is a function of air flow but not the die power, higher air flow will reduce the thermal resistance from die to ambient, and for this study the minimum thermal resistance obtained at $5.9^{\circ}\text{C}/\text{W}$ for maximum air flow.

The part two of this study has been extended to transient heat transfer simulation, with the intention to understand what is the auxiliary heat source that required for the junction temperature to achieve 70°C at transient mode? The auxiliary heat source is

crucial in helping to reduce the qualification time of chip. Sufficient understanding of transient heat transfer paths within the die has been demonstrated through the creation of thermal contour with various heat sources. An auxiliary heat source prototype has successfully been developed and tested. And the transient thermal model has also been verified with the thermocouple-measured transient time, the simulated transient time is within 11% of the experimental measured values. The data shows it requires 22W of auxiliary heat source and takes 69.65s for the junction temperature to reach 70°C from room temperature, this is a very significant achievement that can be applied in chip qualification. The study of verified transient model has also been extended to the effects of various transient times (15s to 75s) and heat sources (7W to 27W) to the heat path resistance from the die to ball, the heat path resistance from die to ball is a function of transient time, in which thermal resistance from die to solder ball increases with transient time; however, at any specific time thermal resistance will not change with various heat sources.

CHAPTER 1

INTRODUCTION

1.1 Introduction

One of the key challenges to maintain an IC's reliability under the compact and high performance environments is the thermal regime. In today's environment, with the emerging of the smart phone and tablet products which require running more data at the fast high speed, this triggers to the significant heat density and huge heat dissipation, trending to the shortened life and malfunction of an IC's device. A 10⁰C to 20⁰C's elevation in die temperature can increase 2 times the silicon failure rate, as a result, for various IC categories, temperature is the most significant contributor to the negative impact of reliability. To make the things worse, the current trend of the consumer product like smart phones and tablets are literally counting on the multi-processor systems-on-chip, which requires ultra-thin assembly with limited space, minimum cost, high expectation of great performance and reliability, and more importantly the time to market, as we are seeing nowadays new electronics devices emerge in the market every 3 to 6 months.

In order to meet the high requirements from the consumer market, from the thermal management perspective, the simple solution is what researches always ignore, and one of the focused areas for the researches is to really understand the transfer of heat in the saturated state and transient especially the later, and apply the in-depth knowledge that gained in the real research and development work of electronic field. With that in mind, gaining the basic theoretical steady state heat transfer knowledge is the prerequisite for a researcher, before embarking on the detailed research studies in the field of heat transfer in transient condition. Fast transient in the thermal

management has triggered the critical need for the research world to understand its applications in the communication, automotive and medical industries. If not all, at least the research of fast transient will significantly help to address the challenges of low cost, high reliability and time to market of the electronic devices, which will be outlining at the end of this research work.

1.2 Problem Statement

The thermal management in electronics industry has posted significant challenges in the 21st century, the engineering challenges in the management of thermal comes from two main areas: (a) increasing integration of advanced features sets, such as camera flash, camera front and rear, touch screen controller, wireless charger, 3G/4G network capabilities and etc, which is concomitant with increasing performance; and (b) the thermal constraints from the mobile devices architecture such as active cooling like fan and heat sink are not feasible in mobile devices, and also due to the shrinking form-factor especially the ultra-thin requirements.

With the emerging of the smart phone and tablet in every corner of the world, that explains literally the strong pervasion of these products into economic life, as published by the International Data Corporation (<http://www.idc.com/>), in the area of smart phone particularly, the global market grew 27.2% year by year and in the second quarter in 2014, with total over a third billion deliveries at 335 million mobile devices, the accurate data for the positive huge growth motivates multiple research areas. Although thermal management is always perceived as a secondary issue, it is still crucial to ensure the performance, reliability, time to market and cost are meeting the market's expectations.

It is not denying that impressive features, performance, time to market and cost factor that always attract consumers' satisfaction especially in the dynamic smart phone industry. Another challenge for the thermal engineer is how to apply the thermal knowledge into the challenge of time to market? Usually electronics or non-thermal engineers have more influence on the products' impressive features design and performance, while the thermal engineers can present a significant contribution just by applying the heat transfer knowledge in the areas of steady state and transient to reduce chip's qualification time, and thus shorter the time to market and make the products more cost efficient.

To recognize the importance of the fundamental heat transfer field, (Nishi, K. et al. 2013) used the steady state and transient heat transfer knowledge to study the transient thermal behavior around the microprocessor and skin temperature of the tablet device, incorporated both simulation and experimental studies, that is just one of the applications of using fundamental transient heat transfer and convert it into practical means, although this is regarded as the product's performance study, this is not the end and it should not be stagnated here, there are more variety applications that an engineer can proceed such as time to market and also cost efficiency by incorporating the fundamental heat transfer knowledge into the actual setup.

Another common study that researcher carries out is to introduce a transient cooling solution to address the fast transient challenge, (Harmand, S. et al. 2011) investigated the transient cooling solution that gives the pretty low resistance of thermal path, and that really helps to reduce the delta in temperatures and then the high temperature spots and overheated, that is a good study from the engineering perspective, but focuses may also need to be in the area of the overall cost and time to market, added thermal solution helps to address the issue of performance and reliability, but it may

not necessary helps in terms of the acceptable cost to the consumers, and more importantly is in this competitive market, how to generate the products to the market in the fastest manners?

With respect to the manufacturing of the chips and launching to the market in the timely manners, it is noticed that the test time of the chip contributed the most from the total validation time, it takes as long as 10 minutes to test a chip during transient heat transfer stage, and the gaps from the literature studies shown that nobody has ever carried out the studies on how to improve the test time of chip and thus improve the manufacturing output. A special heating element has been introduced in this study with the target of more than 80% improvement of test time for the chip.

All in all, with the market trend influx with the novel and complicated thermal solutions, researches tend to ignore that sometimes simple solution like just merely understand well the heat transfer concept and apply it in the area of interests, that unwittingly will help to generate the huge return of invested capital, as what will be outlined in the present study as the research objectives.

1.3 Research Objective

The objectives of this research are:

1. To construct steady state numerical thermal system with the incorporation of heat spreader, simulate thermal contour of heat spreader and die, compare the junction temperature between simulation and experiment.
2. To perform numerical thermal simulation of the steady state heat transfer, and study the impact of the air flow to the thermal resistance network by demonstrating the thermal contour and temperature monitoring points at different configurations.

3. To construct the transient numerical thermal model, and to conclude how the momentum, continuity and energy equations are solved in computational fluid dynamics background. To study the corresponding thermal stress testing heat source and transient time needed for the junction temperature to achieve 70⁰C (reasonable operating temperature for electronics devices), with the reduction of transient test time of chip from 10mins to less than 2 minutes, develop and build a heating element prototype, and compare the data between simulation and experiment.
4. To study the effect of the transient time to the thermal resistance in numerical thermal model.
5. To carry out the studies of the impact of the heat source to the thermal resistance in numerical thermal model.

1.4 Scope of work

In this work, a system was investigated for reasonable thermal qualification time for die and better production output. Simulations and experimental investigations were considered for both steady and transient conditions. Four different powers of die (e.g. 0.5, 1.0, 1.5 and 2.0W) were studied and four different fan flow rates were set at 100%, 50%, 30% and 10% of fan power to observe the thermal performance. The results of junction temperature, heat sink temperature and solder temperature will be captured. The overall thermal resistance are calculated and measured. Both the results from experiment and simulation were used to evaluate the qualification time of die.

1.5 Outline of Thesis

This dissertation consists of five main chapters; it provides a detailed content to represent what is really needed in each chapter. Chapter 1 discusses about the current trend of the electronic packaging in terms of challenges and market demands, and it discusses about the application of thermal solution in both steady state and transient. And it clearly states the problem statement, research objectives and thesis outline. Chapter 2 provides a comprehensive literature review that addresses the variety thermal issues that researchers have done, it is categorized into eight main areas, starting from the fundamental areas of steady state and transient heat transfer, mainly to get the insights how these areas have been studied by the researchers and how they applied the knowledge in more practical manners? Heat sink, heat spreader and thermal interface material are critical in providing the thermal solutions in electronic packaging, these three areas were fully reviewed. Thermal resistance network and thermal simulation are important too, which can help to provide in more detailed understanding of the heat transfer within the entire setup. The experimental measurement, which tells how accuracy is the simulation results, has thoroughly been reviewed.

Chapter 3 explains the detailed materials and methods that used in this study, while Chapter 4 provides the results and discussion, supported by the simulation, thermal characterization and experimental data, it discusses about the crucial observations from the methodology that used. Chapter 5 provides the final conclusions, which typically explains how the research objectives have been achieved, and also suggestions for future works. The dissertation is ended with all of the references that used.

CHAPTER 2

LITERATURE REVIEW

2.1 Steady state heat transfer studies in electronic packaging

Study deals with the challenges of the heat transfer in electronic packaging has been carried out, Haiduk (2011) studied the impact of the forced air convection cooling on heat sink thermal ratings during steady state, by declaring heat sink's ability to remove heat is decided by its impedance, that is measured in degrees Celsius per watt ($^{\circ}\text{C}/\text{W}$), with the support from the mathematic calculation and they used LFM(linear feet per minute) to calculate the effect of forced air convection on a heat sink at steady state, and also introduced a correction factor table, by using these two parameters, the heat sink's free air natural convection thermal resistance rating can be calculated, that is an estimation of the heat sink capability to remove heat, and there was no actual simulation and experimental data to verify the accuracy of the data.

Mohan and Govindarajan (2010) carried out the thermal studies at steady state with CPU at different base plates thickness of heat sink by using computational fluid dynamics (CFD) as shown in Figure 2.1,

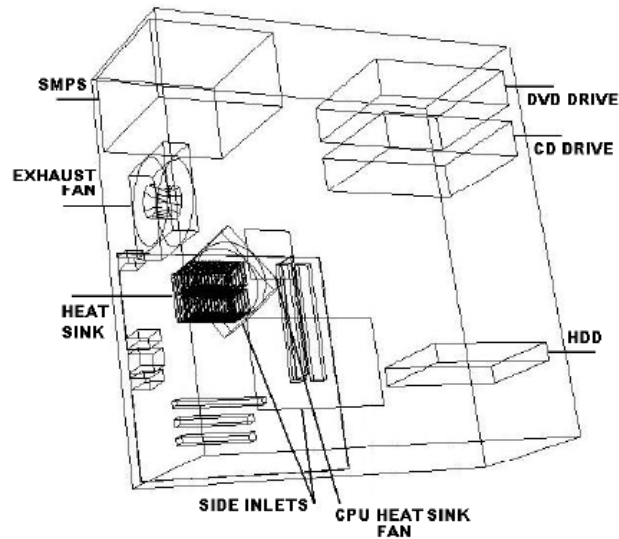


Figure 2.1: Computer Chassis Model (Mohan & Govindarajan, 2010)

It addressed the convergence issue with the simulation data, the study converged at 10^{-4} and 10^{-8} for flow and energy equations respectively; the studies also included the comparison of the data obtained from simulation and experiment, by replacing the material of the heat sink from aluminum to copper, however the actual experiment setup and prototype built were not elaborated in the paper. In addition, cost comparison has to be taken into consideration especially when new material like copper is introduced, as the cost impact can be huge due to the fact that copper is more expensive than aluminum.

Wakefield (2004) used a simplified approach to estimate the thermal resistance of heat sink at steady state under the forced convection application with the extrusion profile as shown in Figure 2.2.

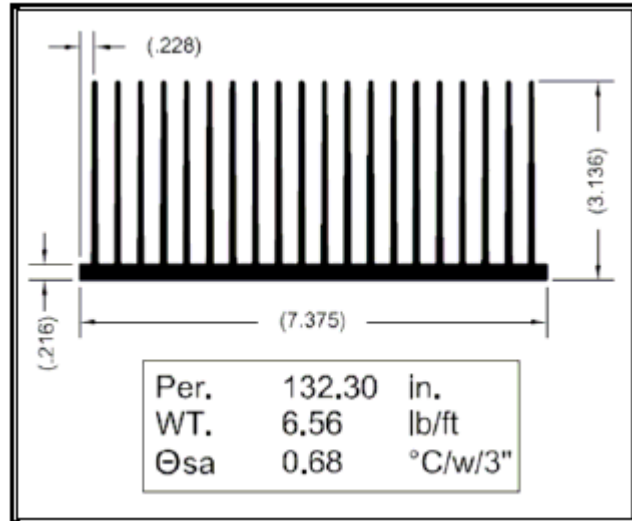


Figure 2.2: Wakefield extrusion profile (Wakefield, 2004)

It is a good reference as it concluded that it achieved excellent correlation between the detailed calculation with the heat sink thermal resistance to ambient at $\Theta_{sa} = 0.11\text{C}^{\circ}/\text{W}$ and the simple approach of Performance Factor Method at $\Theta_{sa} = 0.109\text{C}^{\circ}/\text{W}$, the technique of this approach has been validated and it developed the value by introducing “quick-and-easy” method, however that does not guarantee the accuracy and error may occur when the proposed approach is applied, the safest way is still by incorporating the actual simulation and measurement.

Edwards (2012) described that at steady state, many thermal metrics exist for semiconductor and integrated circuit (IC) packages, example like junction to ambient thermal resistance Θ_{ja} is often misapplied by those who tried to use it to estimate junction temperature in their systems, unless both companies used the same standardized test condition to measure Θ_{ja} , only then the thermal performance of an IC device can be compared, else the system designer should study the junction temperature of their device based on their own setup rather than blindly used the Θ_{ja} directly from the manufacturer.

Koval and Fedasyuk (1997) developed 3D models of heat exchange in semiconductor ICs, and also used the analogy approach of the thermal-electrical and a 3D analytical method to perform the simulation of the heat dissipation process at steady state in electronic packaging, then it used the approach of illustrating the thermal resistance's simulation in IC package, and it claimed the results obtained between the simulation and measurement for the IC package's thermal resistance vales differ around 10%, however it did not share the thermal simulation in details with the considerations of actual IC and heat sink geometries.

Manchester and Bird (1989) used 1D and 2D thermal models for steady state studies, which always causing in substantial errors in simulation, which can be 50% or more, for the thermal simulation that carried out, the target of the relative errors should be kept as low as 10% with respect to the junction temperature's response to the power, and with the validation with the actual measurements.

Vaddina et al. (2011) has performed a very comprehensive steady state thermal modeling in the 3D stacked die analysis as shown in Figure 2.3

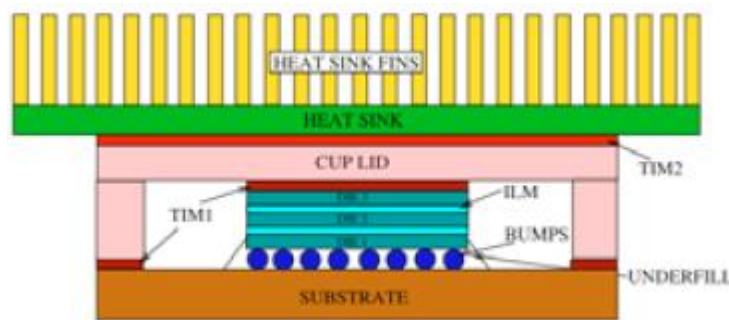


Figure 2.3: 3D stacked die model (Vaddina et al, 2011)

However the only limitation is the heat sink fins' thermal model were not shared, the studies only used the coefficient of effective heat transfer as a only heat sink's boundary condition, it also suggested that the die nearer to the heat sink will have the

low junction temperature, therefore, with the low thermal resistance from the silicon to the heat sink, whenever the fan speed increases, the junction temperature of the silicon will be lower and thus the lower thermal resistance from the silicon to the heat sink as what has been suggested from the simulation results.

Kowalski (2000) performed steady state of investigation in thermal for the design of a complicated cabinet used in high speed internet application, it utilized Flow Network Modeling (FNM) and Computational Fluid Dynamics (CFD) in a collaborative and more interaction manner for a fast and precise thermal studies of the whole system, to generate flow impedance characteristics, by using and creating the model of network for the full system, which is to predict the flow distribution throughout the whole system, a comprehensive measurement system for the airflow velocities has been carried out in various parts of the cabinet, the simulation variation for the flow rates that pass through card passages and total flow through the card passages, and entire air flow through the whole system are less than 10% of the measured values. The study is summarized in the flow chart as shown in Figure 2.4.

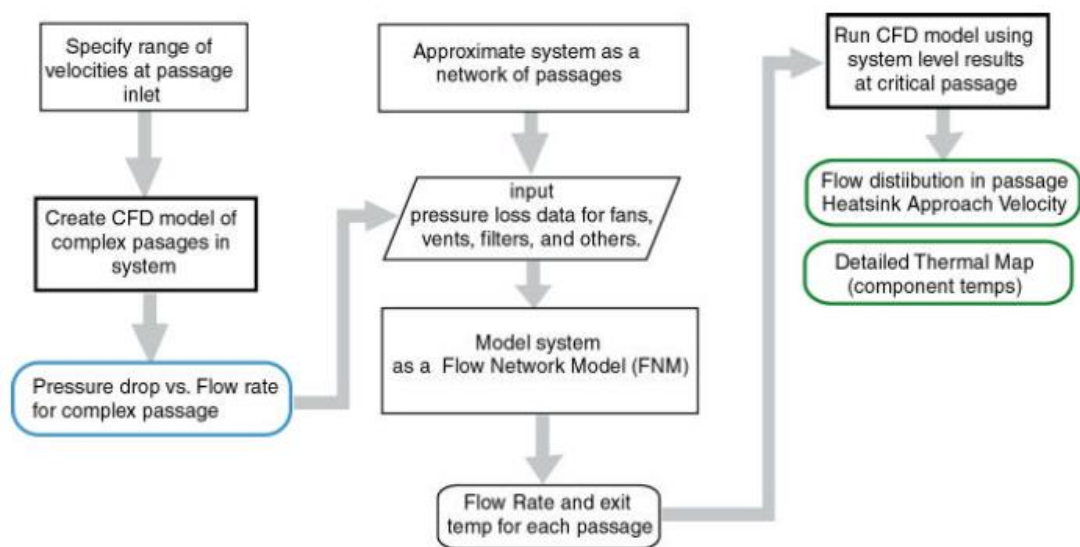


Figure 2.4: Flow Chart of the analysis technique (Kowalski, 2000)

Zhao (2002) studied the steady state thermal modeling of a network communication box with module such as printed circuit boards, IC packages inside, the IC packages were attached with heat sink to achieve cooling purposes.

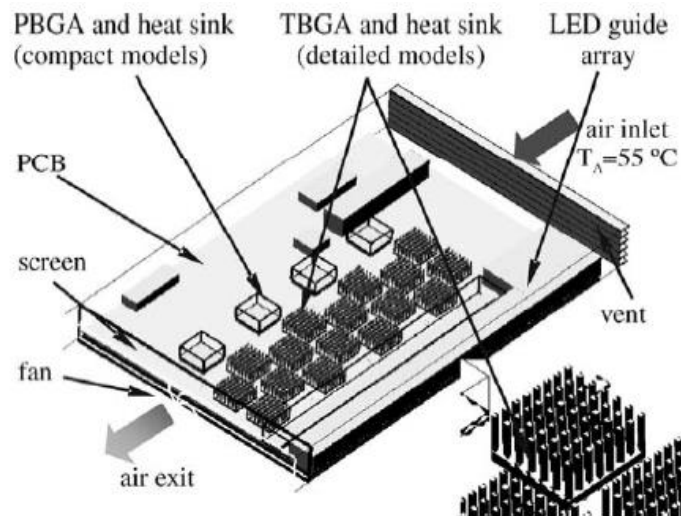


Figure 2.5: Thermal Model of the network module prototype (Zhao, 2002)

The full Navier-Stokes equations for the air-flow were solved, and Buoyancy effect was considered too. The analysis was carried out with the IC packages modeled for the purpose to get the junction temperature, and that can be used for optimization of the thermal system and the study of the system reliability. The impact of altering the design of the thermal system on the IC package silicon temperature together with the operating conditions of hydraulic system for the fans were examined in this study. Although the simulation results were compared with the Joint Electron Device Engineering Council (JEDEC) measured data of thermal characterization for IC package, which is attached with heat sink, due to the fact that the thermal exchange between the IC packages in the application of system together with the variations between the application Printed Circuit Board (PCB) and JEDEC board for testing, the comparison of the simulation data with the measurement data was not available

with the same condition of the test, the thermal test of the JEDEC provides a good reference for studying the numerical model in the similar forced air convection conditions. Further study on the JEDEC test standard and guidelines for reporting electronic package thermal information is available at JEDEC Standard, <http://www.jedec.org/sites/default/files/docs/jesd51-12.pdf>

Zhang et al. (2012) investigated the steady state thermal performance on the 3D integration die. The simulation of the temperature versus power have been carried out with the development of a thermal model in finite element by using Ansys to precisely predict the junction temperature and stress induced by thermal, the simulation and experimental methodology has been suggested, in which the measured data were obtaining by adding a thermocouple into the molding epoxy, with a hole with diameter 3.2mm drilled on the chip's top surface, and ended at the active layer of die, an epoxy-based adhesive has been filled into the hole as shown in Figure 2.6.

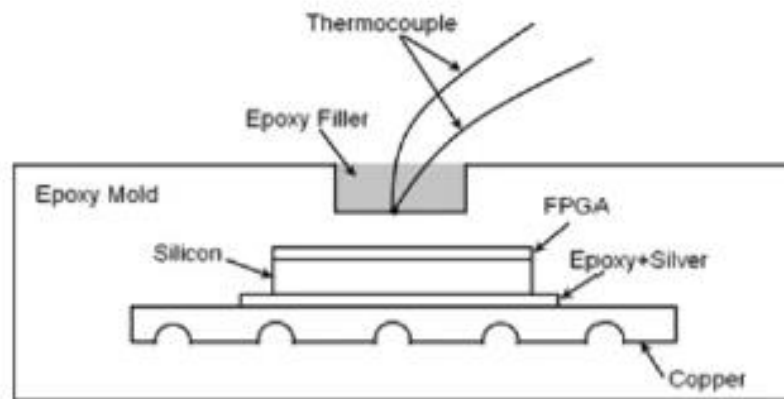


Figure 2.6: Schematic of Temperature Measurement (Zhang, C. et al. 2012)

The study also shared the considerations for the experimental setup, with the temperature measurement at room temperature 25°C and the accuracy of the experimental temperature value was within 1%. A study of the parametric on the

correlation between the important factors such as the rate of toggle, the frequency of clock, the utilization of slices, the buffers output, and thickness of die substrate, and junction temperature were implemented.

Chan et al. (2011) studied the effect of all sort of chip thicknesses on the silicon hot spot temperature by executing both analytical method as shown in Figure 2.7 and experimental method at steady state, with the different silicon thickness (21.5-400 μm) and different power of heat conditions (0.2-0.5W). With the purpose of suggesting a closed-form expression analytically to predict the resistance of spreading, the spreading resistance is a crucial measurement used to predict junction temperature. The proposed expression of analytical method in good correlation with the measured data, within 6%, with the impacts of the contact radius as non-dimensional, and also the thickness of substrate as non-dimensional parameter, together with the consideration of Biot number.

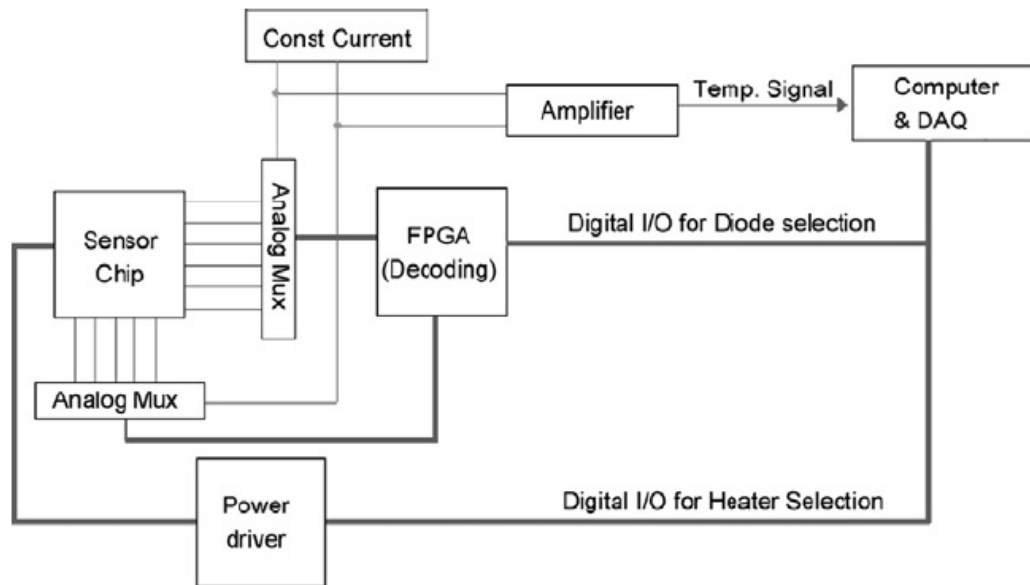


Figure 2.7: Circuit configuration of a diode temperature sensor array-DTSA (Chan, B. et al. 2011)

Moghaddam et al. (2003) evaluated the approach of many analytical compact models of heat transfer for thermal design at steady state, the performance and evaluation in the area electronic packaging, with the claim that providing 3D numerical thermal model is really taking time and not efficient. The developed model with the orthotropic materials was incorporated with the models of heat flow that are available in the calculation of the resistance network, and that can be used to calculate the heat transfer rate and silicon hot spot in the multi layers of chip as shown in Figure 2.8.

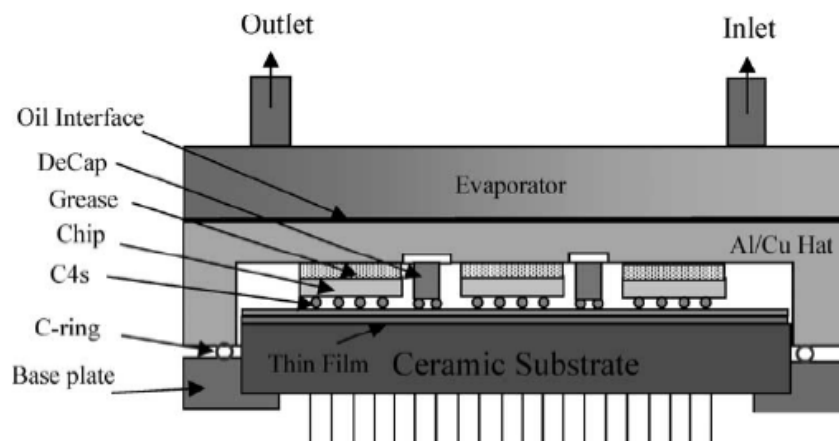


Figure 2.8: Multi-chip module with the cooling system (Moghaddam, M. et al. 2003)

Although the results obtained from the analytical and numerical models were sort of close, with the average difference of 0.3°C at the top insulation, there was not experimental data collected, future work should be carried out in experimental area.

Berriah et al. (2010) carried out the study of the steady state power distribution modules of the WaferBoard system. The study gives the findings of thermal management at steady state, and that contributes to the characterization of its performance, by factoring in the selection of material, the validation and also the design of the cooling system to mitigate the hot spots and significant gradients in thermal performance. The thermal performance of the suggested distribution of

power and the strategy of thermal management was assessed and validated by using the approach of finite element as shown in Figure 2.9 with no experimental data collected.

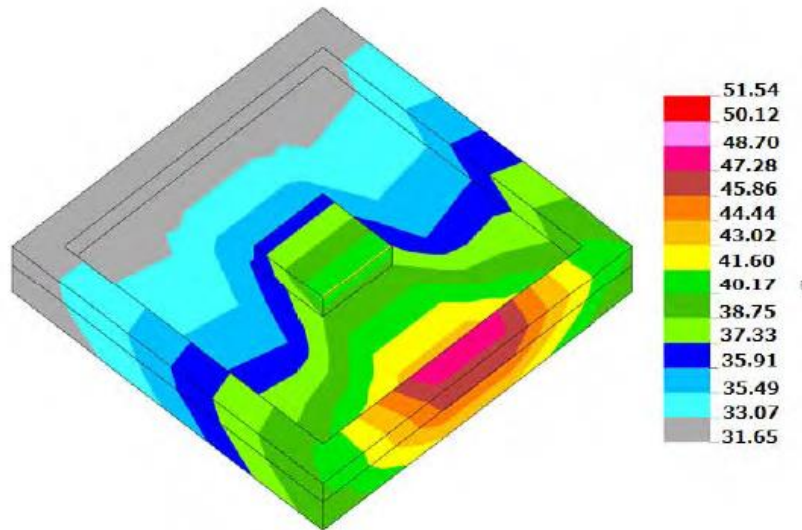


Figure 2.9: Temperature distribution for the power device configuration (Berriah, O. et al. 2010)

It proposed a good approach that was applied to simulate the behavior of steady state at crucial devices of power.

2.2 Transient heat transfer studies in electronic packaging

Nishi et al. (2013) studied tablet device's system level transient heat transfer as shown in Figure 2.10, the study started from the analysis of steady state based on the simulation of conduction for the better understanding of the impact on the die temperature and the temperature of skin, and thereafter determined the final configuration for the simulation at transient.

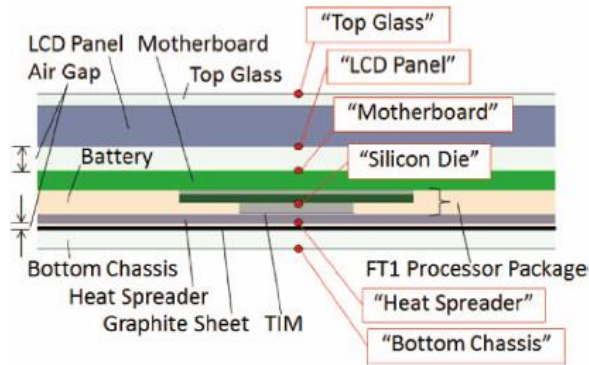


Figure 2.10: Internal side view around the processor (Nishi,K. et al. 2013).

The analysis of transient state was carried out with the assumption that made, in which a microprocessor will start to run the application of Thermal Design Power which is equivalent to workload after the system has reached steady state. The study was conducted with the simulation, with a lot of explanation focused on the boundary condition and simulation setup, but with no actual measurement carried out. On top of addressing the challenge of lowering down the junction temperature, the real application of this study needs to be discussed as well.

Bruce (2002) developed the simplified transient model for IC packages; the study used the thermal circuit as shown in the Figure 2.11 and the commonly available thermal metric to calculate the time versus temperature curve during the cycle of power on. The metrics of thermal has also been used to develop transient model for IC packages and calculate the thermal capacitance. Although this simplified method can easily be used for the calculation, it is strongly suggested that the simulation still needs to be taking place in order to achieve more accurate calculation.

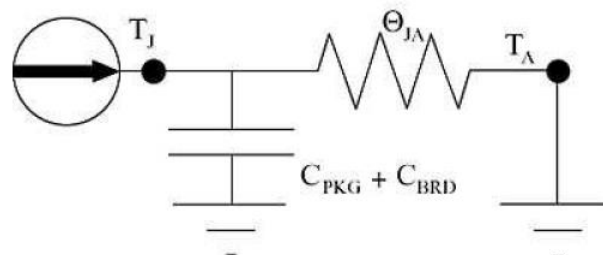


Figure 2.11: One stage RC network (Bruce, G. 2002)

Gupta and Weng (2010) developed a predicting method of IC in the area of thermal behavior in transient; the proposed method is helpful for power-management ICs and other devices in the environments of high temperature. After the characterization of thermal behavior, a model of mathematic was formulated, this equation used dissipation the power and the temperature of ambient to predict the hot spot of a silicon as a time function, and it can be used to simulate transient temperature inside the silicon. A law of physics with the thermal behavior was introduced and performed for the use of thermal-body models that defined as ICs, according to the study, a similar RC network in passive for modeling an IC with transient thermal model was suggested as shown in Figure 2.12.

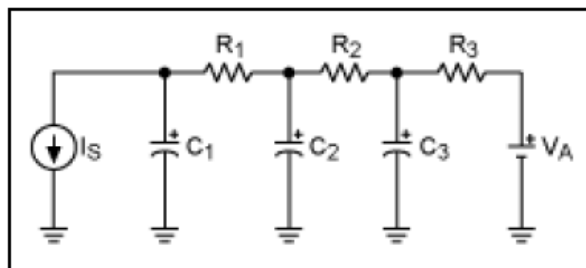


Figure 2.12: RC network models the transient-thermal behavior of chip when heat is generated (Gupta, M & Weng, D. 2010)

To prove the usefulness and precision of the suggested method, the data from experiment were shown as well, with the help of the correlation between the diode voltage and temperature as shown in Figure 2.13.

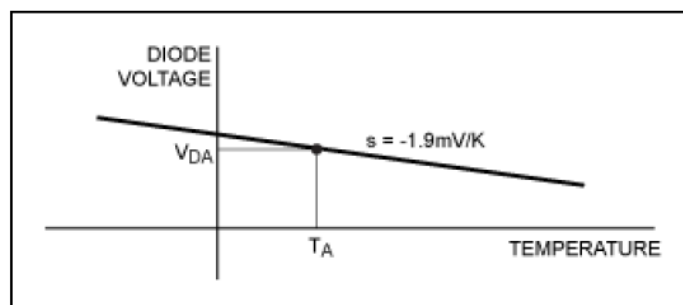


Figure 2.13: Forward voltage for a diode biased at constant current varies with temperature (Gupta, M. & Weng, D. 2010)

Although this approach has described an acceptable way of modeling the behavior of thermal in a silicon with the network of RC, the measurement method can still be improved by direct reading the temperature from the chip as an output rather than demonstrating the correction between the voltage and temperature, which indirectly introduced another noise factor which may impact the accuracy of the temperature reading for the chip.

Fedasyuk et al. (2001) explained a new method of characterization in transient heat transfer for the widely used structure of flip-chip as shown in Figure 2.14.

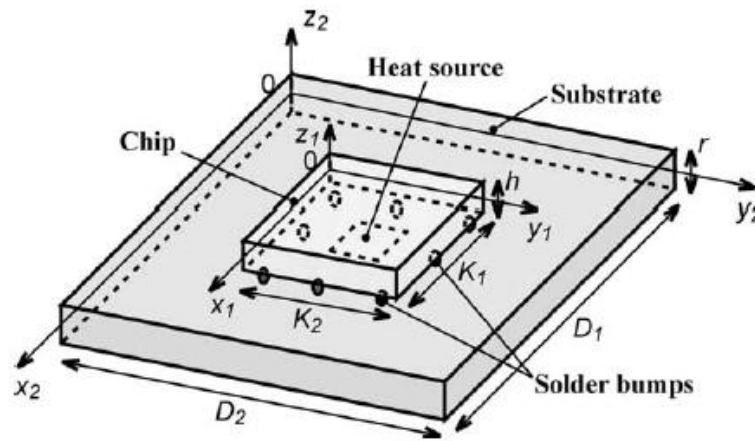


Figure 2.14: Flip-chip structure (Fedasyuk et al. 2001)

The study is according to the analytical approach of the transient heat exchange conjugate challenge for the substrate and silicon. The gist of this approach is in showing the function of sought for four variables in the terms of linear expansion along z coordinate and the studies of two functions with three parameters. The precision of the model is tested by comparing with the calculated results of the transient of temperature in the structure of flip-chip, by using the analogy of thermal-electrical approach; with the relative error obtained not more than 10-15%. Although it achieved error less than 2%, there was no actual setup or prototype involved, thus

the accuracy is still questionable due to the fact that the boundary conditions in the real setup is different for any of the case.

Smith et al. (2008) carried out the thermal interface characterization through both experimental and compact numerical modeling, to compare steady state versus the characterization of transient focusing on the package to chip assembly in the test environment that is similar to chip assembly as shown in Figure 2.15.

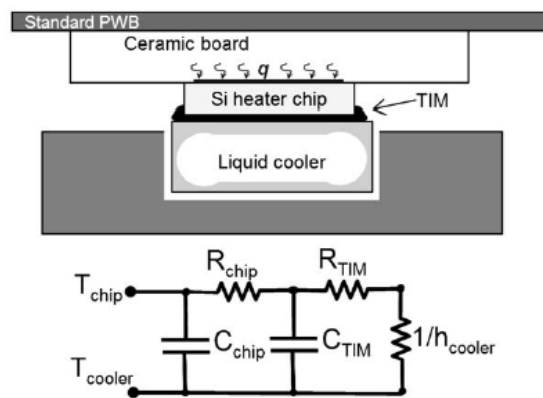


Figure 2.15: Schematic of the test fixture with corresponding RC network model describing heat flow through the thermal interface material (Smith et al. 2008)

The variable interface bond-line technique is solid and precise in both steady state and transient thermal interaction characterization, and it is suitable for the standard of industry chip-to-cooler's thermal interface material (TIM). And the study also concluded that transient measurement to extract the effective of conductivity for the TIM through the numerical model fitting is not enough due to the fact that uncharacterized complexities of the cooler's heat transfer, the spreading heat due to spatial non-uniformities in thermal flux, and noise factor in the early stage transients. Rencz et al. (2003) designed cum developed a heat-flux sensor to help the transient thermal characterization of IC; the intention is for fast transient measurements in the

characterization in IC packages. The proposed architecture for the sensor of heat-flux is shown in Figure 2.16.

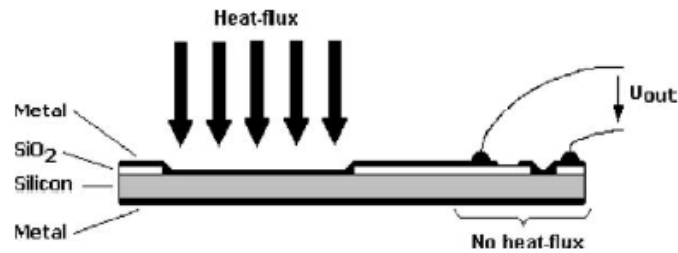


Figure 2.16: Proposed heat-flux sensor (Rencz, V. et al. 2003)

This is useful for the investigation of IC packages in experimental approach, in both cases of transient and steady state. The sensors come with the characteristics of linearity for the temperature range in board. A viable fast and simple way for the calibration to be presented as well, however, when the large volume of the sensors are fabricated together with the standard silicon technology is deployed, the individual calibration can be avoided. On top of capable of measuring the heat-flow in different heat paths, and for the validation of the spreading for the heat flow on huge surfaces, the sensor that developed can also be used for direct measurement of the map of heat flux in any surfaces that are flat as shown in Figure 2.17.

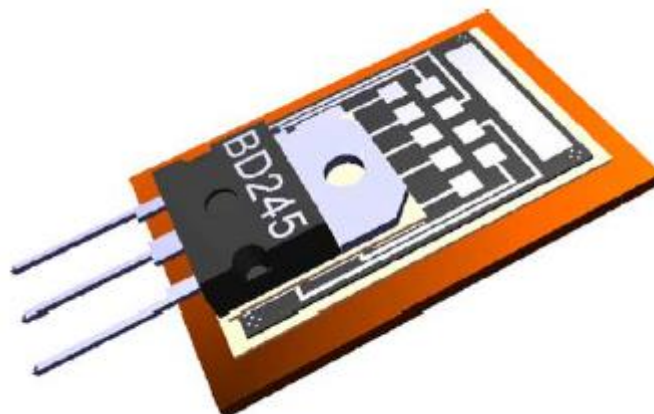


Figure 2.17: Measuring the heat flux distribution through a package surface.

The presented features shows that the sensor is a priceless tool that can be used to validate the model of compact thermal for IC packages, however, further study should be carried out with the characterization of the contact force between the sensor and the IC package, mainly to understand the impact of the contact force towards the measurement value such as the heat-flux, only then the proposed sensor structure will be more convincing in the applications.

Loh et al. (2007) used the asymptotic waveform evaluation (AWE) to characterize the quick transient heat conduction for Fourier and non-Fourier. The Fourier and non-Fourier equations have been simplified to a linear equation in differential term, by using the method of finite element, and thereafter solved with the AWE method. The moment AWE is coupled with finite element approach, it has the capability of solving one and two dimensional problems, and even the conduction of heat problems in three-dimensional with reasonable accuracy. However, the challenge of the AWE is its built-in instability of Pade simplification, which may result in unstable solutions, that may happen for stable system too.

Gowda et al. (1998) performed the laminar transient heat transfer simulation by using finite element approach, that flows through an inline tube bank, by applying the correlation of velocity procedures. The two-dimensional, non-steady Navier-Stokes, and energy equations have been solved by introducing both semi-implicit and explicit algorithm with 100 as Reynolds number, and 0.7 as Prandtl number, 1.5 and 2.0 as pitch-to-diameter ratios (PDR). The main results of the study showing a reducing in the CPU time for the case of the semi-implicit scheme. And also the changing of the Nusselt number with time is fast, especially at phase of the heat exchange between the fluid and cylinders, as for the average coefficient of friction.

Pablo and Atienza (2009) described that impacts of thermal performance can only be validated in the last stage of the design, that basically implies involving huge redesign cost. Therefore, the key design challenge is the implementation of the quick exploration approach of different hardware and software executions alternative for IC packages with precise predictions (e.g. energy & performance) that helps to address the transient thermal modeling behavior to calibrate the final design architectures. This paper proposes a new approach with the quick transient thermal modeling technique and studies of the Multi-processor System-On-Chip (MPSoCs) in 3D with cooling solution in active manner, together with software and hardware interaction framework, which enabled the fast studies of the run-time in 2D/3D MPSoCs in term of thermal behavior as shown in Figure 2.18.

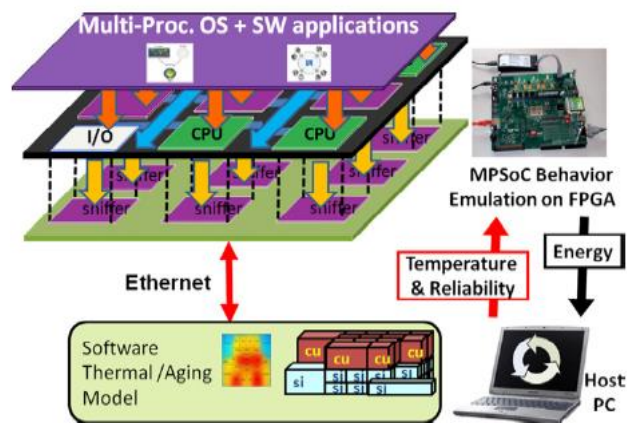


Figure 2.18: Overview of the 2D/3D MPSoCs thermal emulation framework. (Pablo. V. & Atienza, D. 2009)

The empirical results have shown that the suggested framework generated the detailed transient thermal exploration with nearly zero loss in thermal prediction accuracy (less than 3%) if compared with the traditional (which is time consuming) method of finite element.

Harmand et al. (2011) carried out the transient cooling of electronic components by Flat Heat Pipe (FHP) which was developed to give the cooling effect for different components in transient state. The FHP geometry studied is shown in Figure 2.19. The IC components are the heat sources (evaporators), which are mounted on the top surface of the FHP, and the fins are the sources (condensers) of cold, which are mounted on the bottom surface. The structure (i.e., the porous wick) capillary is enclosed in the FHP wall within the internal compartment.

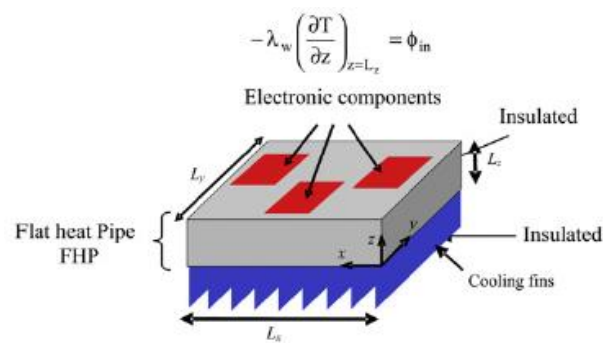


Figure 2.19: Flat Heat Pipe

The model is in transient, combining 3D thermal model with a 2D hydrodynamics one through the flux of mass for evaporation condensation, that happens in a mass conservation equation. The results show that the comparison of the thermal behavior in the FHP and its equivalent solid plate submitted to a transient thermal cycle, showing that the FHP improved the cooling effect for the long thermal cycle duration, particularly when the solid plate is more efficient for the case with short transient thermal cycles. The FHP also gives better thermal resistance, which directly helps to minimize the thermal gradient in the system and therefore reduce the hot spots.

Kandasamy et al. (2007) studied the transient cooling in electronics by using material with phase change characteristic-based heat sinks, with both empirical and numerical analysis have been performed. The prototype setup is shown in Figure 2.20.