CORRELATION METHODOLOGY BETWEEN SILICON AND HSPICE SIMULATION OF AC IO BUFFER

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LIST OF ABBREVIATIONS

Abbreviation	Meaning
AC	Alternative current
FPGA	Field Programmable Gate Array
GPIO	General Purpose Input Output
HSPICE	Higher-level Simulation Program with Integrated Circuit Emphasis
IBIS	Input/Output Buffer Information Specification
IC	Integrated Circuit
Idsat	Saturation current
IO	Input/Output
IP	Intellectual Property
IR	Current Resistor
PCB	Printed Circuit Board
PDN	Power Distribution Network
PSPICE	Personal Simulation Program with Integrated Circuit Emphasis
PVT	Process, Voltage, Temperature
SPICE	Simulation Program with Integrated Circuit Emphasis
SSN	Simultaneous Switching Noise
TSV	Thorough Silicon Via

KAEDAH KORELASI DI ANTARA SILIKON DAN SIMULASI HSPICE AC PENIMBAL IO

ABSTRAK

Dalam era teknologi terkini, sistem yang mempunyai berkeupayaan tinggi dan reka bentuk yang rumit memberi kesulitan kepada pereka bentuk. Keupayaan untuk mensimulasi reka bentuk komplek sebelum diberikan kepada pelanggan telah bertukar menjadi asas kepada pencapaian projek. Berdasarkan kepada pandangan pengilang, pemberian model HSPICE sangat berisiko kerana harta intelek (IP) penimbal IO yang sulit mungkin tersebar kepada orang luar. Pihak industri kebiasaannya mengedarkan model IBIS yang mengandungi teknik tingkah laku bagi memaparkan penimbal IO daripada model HSPICE tersebut. Maka, korelasi antara model HSPICE dan silikon menjadi penting bagi memberi lebih keyakinan dan meningkatkan kebolehpercayaan dan ketepatan model IBIS yang akan diedarkan kepada pelanggan. Dengan itu, kajian ini dijalankan untuk mencadangkan model korelasi bagi penimbal AC IO di antara simulasi HSPICE dan silikon secara cekap dan sifar kesilapan. Di dalam kerja penyelidikan ini, penimbal AC IO diuji berdasarkan masa menaik dan masa menurun bagi isyarat keluarannya. Dengan melaksanakan model korelasi ini, kebolehpercayaan model IBIS dari segi pemasaannya dapat memastikan keserasian dengan silikon secara berkesan. Bagi penyelidikan ini, hasilnya, proses sudut pantas dan tipikal memenuhi sasaran korelasi yang ditetapkan pada ± 20%, manakala proses sudut perlahan telah gagal memenuhi sasaran.

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ABSTRACT

In this technology era, the high-performance systems that include complexity on the design make noteworthy difficulties to board designers. The capacity to simulate the complex design before laying out the board has turned into a basic consideration for the accomplishment of a project. Based on manufacturer's viewpoint, releasing a HSPICE model is a high risk, since the confidentiality of IO Buffer intellectual property (IP) might be exposed to outsiders. Industries usually distribute the IBIS model in which behavioral technique for displaying IO buffers is obtained from the HSPICE model. Therefore, correlation between the HSPICE model and silicon become significant to increase the reliability and accuracy of IBIS model which would be released to the customer. Hence, this research was carried forward to initiate correlation model for correlation of the HSPICE and silicon of AC IO buffer, in an efficient and error free manner. AC IO buffer is one of the important features needed to ensure reliability of IBIS model before handing over to the customer. In this work, AC IO buffer is tested on the rising time and falling time of output signal from the IO buffer. By implementing this correlation model, the timing of the IBIS model could ensure compatibility with silicon effectively. As a result, the fast and typical process corners meet the correlation target which was set within ±20%, but slow process corner was not meeting the target.

CHAPTER 1

Introduction

1.1 Overview

Input/Output Buffer Information Specification (IBIS) is a modeling technique widely used by industries to model simple buffer which duplicates the proprietary nature of integrated circuit device design, while providing information-rich model for signal integrity and electromagnetic compatibility without revealing the Intellectual Property of their implementation.

IBIS model was developed from Higher Level Simulation Program with Integrated Circuit Emphasis (HSPICE) model. HSPICE model is a content of netlist details, confidential circuit netlist from the designer which cannot be exposed to outsiders. Hence, to gain confidence from customers, the IBIS model will be published to customers. IBIS model is a behavioral model which provides limited information before the device is fabricated. Before generating the IBIS model, correlation between silicon data and Simulation Program with Integrated Circuit Emphasis (SPICE) model is an absolute necessary. In the end, generated IBIS model will be a golden model of IO buffer. There are two types of IBIS model which is Traditional IBIS and IBIS-AMI [1].

Traditional IBIS generates the test format contain in tabular data such as IV output curve (I vs V), rising and falling time transition waveform (V vs t) and package parasitic information. This method was used to exchange the modelling information among semiconductor suppliers, software suppliers and end users. It helps the designers to save their time in doing analysis instead of generating prototype circuit boards before the fabrication of devices. Besides that, in real scenario, IBIS model will port over in software and will be used by customers. So, it is important to ensure the model has valid information.

IBIS model was basically developed from HSPICE model which models the real situation measurements. It will ensure the modeling of PCB boards, device packages, board traces, and resistors and also capacitors used on board will be included in the HSPICE model as netlist.

Even though the development of HSPICE models is based on similar setup to the hardware, there are always gaps between silicon measurements and HSPICE simulation models. Since simulation is an ideal case, theoretically the output will be ideal too. However, measurement results would not be an ideal scenario since various factors will impact the results such as distortion, noise, power dissipation and more. So it is necessary to ensure the variation between measurement and simulation are within some tolerance ranges before exposing it to vendors. Therefore, an efficient methodology is needed to correlate the measurement and HSPICE simulation model which will be used to generate IBIS model later.

1.2 Problem Statements

Field Programmable Gate Array (FPGA) is widely used in embedded industries nowadays. To drive the signal, IO ports will be used by users, for example, a user need to give some inputs to obtain outputs. Some users provide input in software design but the output is commonly observed from output ports/pin. When the IO port has started to take part in a design, the IO buffer will be used. Input buffers are used to drive input signals while output buffers are used to drive signal according to intended user designs.

If problem exist in the IO buffer, they could influence the results of following blocks, for example, data failed on setup or hold time, data corruption etc. To ensure the IO buffer is free from faults, it should be tested by the IP owner. Transition of rise time and fall time will impact the data displayed on output pins in real time. Sometimes the signal is not clean, it comes with ringing effect. Thus, simulating the complex design before developing the board is a critical factor for the success of this project.

In this research, only rising and falling time transition waveform (V vs t) will correlate between silicon measurement and HSPICE simulation model across various IO standards. Measurements on devices are correlated to HSPICE simulation model. Even though the modeling on HSPICE is equipped with Printed Circuit Board (PCB) models, device package models, board traces, board resistors or capacitor models, but it is expected that mismatch could happen due to some external impacts. This research will emphasize on correlation methodology between HSPICE simulation model and measurements on 20 nm silicon while to ensure the correlations are within the tolerances.

1.3 Objectives

The objectives of this research are:

i. To validate HSPICE simulation model's electrical behavior and silicon's electrical behavior across full-range of PVT conditions on an AC IO Buffer.

ii. To propose an efficient methodology to correlate HSPICE model with silicon measurement for the AC IO buffer.

1.4 Project Scopes

This research will only cover the rising and falling time across process corner, voltage and temperature (PVT) for three IO standards. The full range of PVT combination which will be covered in this research is tabled as below:-

Table 1.1. PVT condition covered

Process Corner	**Voltage**	**Temperature**
Faster	Vmax	Cold
Typical	Vtypical	Nominal
Slow	Vmin	Hot

The IO standards covered in this research are 1.5V-LVCMOS 8 mA, SSTL15 with 34 ohm termination and 1.2V HSTL Class I 8 mA. IO standard is a protocol used to connect between devices. This research will only focus on the three protocols mentioned above. SSTL is commonly used on DDR memory while LVCMOS is used on low power application devices.

Thus, the bench setup will be constant throughout the research for AC IO Buffer measurement purpose. Stability of the bench will be ensured from time to time. Bench platform consists of power supplies, pulse generator, oscilloscope, characterization board and Rosenberger cables. All equipment is verified accordingly, calibrated and in good conditions to ensure correct measurements are obtained. For creation of the HSPICE simulation file, Linux environment computer which included HSPICE library are used. Besides this, Matlab software was used to develop the correlation model and to correlate between HSPICE model and silicon measurement.

1.5 Research Contributions

The development of correlation methodology between HSPICE simulation model and silicon measurement is to ensure the miscorrelation percentage between this two components fewer minutes. Manual correlation methodology will take longer time to correlate one file but with this methodology, fewer files could correlate within few minutes depending on the number of files used for the process. In normal situation, manual correlation is used to plot both waveforms and a manual calculation is done for rise time and fall time. Based on the 20% and 80% of rising and falling points of each waveform, the correlation percentage will be computed. It takes more time and human error could impact the results as well. Besides that, by ensuring the correlation methodology is valid and efficient, it will help designers to narrow down their debugging based on correlation results. In industry perspectives, the resources can be reduced by cutting down the time to do manual correlation.

1.6 Thesis Organization

The remainder of this dissertation is organized as follows:

Chapter 1 is an introduction to this research that briefly defines research background, problem statement, objectives, research scope and contribution of this research in efficient correlation methodology in semiconductor industries.

Chapter 2 reviews some basic theories on Output buffers and their impact on output signals. IBIS model which is commonly used in industries and SPICE models are explained widely. Since correlation is conducted between HSPICE simulation model and silicon measurement, the methodology to develop data for these two elements were huge. Few researches were conducted in the past to improve this methodology. Those methodologies which are implemented in this research are also discussed in this chapter.

In Chapter 3, methodology of this research is discussed. Firstly, the preliminary test to establish HSPICE simulation model and silicon measurement is explained extensively. Then, the traditional methods used to calculate correlation percentage between HSPICE simulation model and silicon measurement are explained. Finally, at the end of Chapter 3, the new methodology which is developed using MATLAB tools is presented.

Chapter 4 begins with the experimental results from the developed method of correlation between HSPICE simulation model and silicon measurement. This chapter validates the manual correlation method and a newer developed method with expectations that both results show similar numbers with some tolerances.

Finally, Chapter 5 concludes this entire research. The research findings are summarized and discussed here. Besides that, the limitations, suggestions and future directions of this research are also included.

CHAPTER 2

Theoretical Background and Literature Review

2.1 Introduction

This chapter provides the background of IO buffer, IBIS model and HSPICE model for better understanding before this study is conducted. Besides that, the correlation methodology implemented on IO buffer and its related works are also discussed in this chapter. Section 2.2 elaborates the component used in this research such as IO buffer, IBIS model and HSPICE model. While Section 2.3 discusses the correlation of measurement and simulation towards related work and reviews pass studies as well. Finally, Section 2.4 summarized the chapter.

2.2 Background of IO Buffer

2.2.1 Input/Output Buffer

IO buffer is the process of temporarily storing data that is passing between a processor and a peripheral. The usual purpose is to smooth out the difference in rates at which the two devices can handle data. In FPGA, the IO buffer circuit is placed near general purpose Input/Output circuit. The signal drive from core and

peripheral is driven by the IO buffer. Figure below shows High-Level View of Single-Ended General Purpose Input/Output of Altera devices.

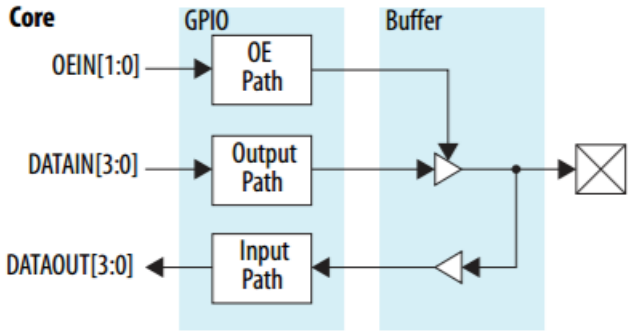

Figure 2.1. High-Level view of Single-Ended GPIO [2]

Output path will be enabled when the devices communicate with external interface for writing process, such as device writes on memory. For output path, output enabled circuit enables the buffer and the data from the core drives the signal to peripheral to complete the writing process. On the other hand, during the read process which is device read from the external devices, the input buffer is used. The data is driven from the memory to devices to be processed. In this phase, the buffer plays a role as a gate to allow data in and out from the circuit.

GPIO consists of various type of IO buffer such as LVDS, DDR and 3V IO bank. LVDS IO bank supports differential and single-ended IO standards up to 1.8 V. The LVDS IO pins form pairs of true differential LVDS channels. Each pair supports a parallel input/output termination between the two pins. LVDS channel can be used as transmitter only or receiver only. Each LVDS channel supports transmit SERDES and receive SERDES with DPA circuitry. For example, if you use 30 channels of the available 72 channels as transmitters, you can use the balance 42 channels as receivers.

Next, 3V IO bank supports only single-ended IO standards up to 3 V [3]. Each adjacent IO pair also supports Differential SSTL and Differential HSTL IO standards. The single-ended output of the 3 V IO supports all programmable IO element (IOE) features except Programmable pre-emphasis, RD on-chip termination (OCT), Calibrated RS and RT OCT and Internal VREF generation.

Finally, DDR IO buffer support differential and single-ended IO standards. For LVDS, the DDR IO buffers support only LVDS receiver and emulated LVDS transmitter buffers. For DDR, the DDR IO buffers on the right side of the device only supports DDR3 external memory interfaces [4].

2.2.2 IBIS Model

Input/Output Buffer Information Specification (IBIS) model is a behavioral modeling method which provides the information of input/output buffer without revealing the underlying circuit's structure. These modeling methods were based on I-V and V-t curves which is obtained from silicon measurement or circuit simulation of IO buffer designer [1].

While high speed application is a must in this growing technology world, it starts to create timing issues. As a result, simulation of IO buffer with an accentuation on signal integrity has been a vital angle in the design of integrated circuits (IC). For vendors, this means divulging exclusive data about their IO buffer which would incorporate a full transistor-level schematic as well as full process data, for example, transistor oxide thickness. Moreover, for designer to play out a full transistor-level reproduction it would take hours utilizing

conventional circuit simulation, such as, SPICE. As a solution, the IBIS model was initiated by Intel in early 1990's [5].

Generally, an IBIS model is characterized by the following electrical dc data, ac data and parameters:

- Pullup and pulldown curves
- Power and ground clamp curves
- Ramp rate
- Rising and falling waveforms
- The buffer's capacitances
- Package parameter

2.2.2.1 V-t Curve

The AC IO buffer refers to V-t curve. The ramp rate (dV/dt) depicts the move time when the output is changing from the present logic state to another logic state. It is measured at the 20% and 80% points with a default resistive load of 50 ohm.

The falling and rising waveforms demonstrate the time it takes the devices to go from high to low and from low to high, respectively when driving a resistive load associated with the ground and Vdd. For a standard push/pull CMOS, four unique waveforms can be created: two rising and two falling. For every situation, one is with the load connected with Vdd and another connected to GND. Nonetheless, it is extremely normal to see just two of these waveforms in the

model. Figure 2.2 shows the measurement setup for V-t waveform [6].

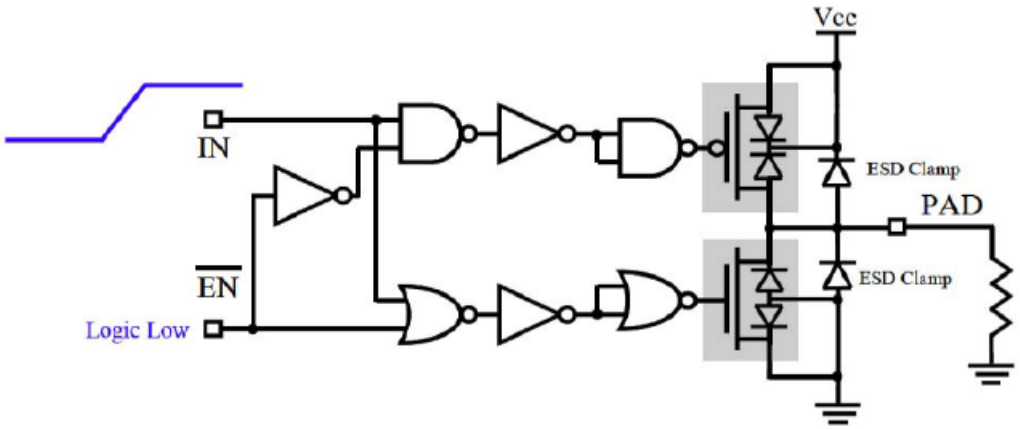

Figure 2.2. V-t Data Measurement setup [6]

This information is then used to build the Rising Waveform and Falling Waveform tables in the IBIS document.

2.2.2.2 I-V Curve

The pull-up and pull-down information characterizes the drive quality of the devices. These curves are acquired by describing the two transistors in the output. The pull-up information portrays the I/V conduct when the output is in logic high state which is the PMOS transistor is ‘ON’ while NMOS transistor is ‘OFF’. The pull-down information demonstrates the DC electrical attributes when the output is in a logic low state which is NMOS transistor is ‘ON’ while PMOS transistor is ‘OFF’. Figure 2.3 shows a single stage 3-state buffer with ESD

protection. This figure helps to demonstrate how the I-V data is measured [2].

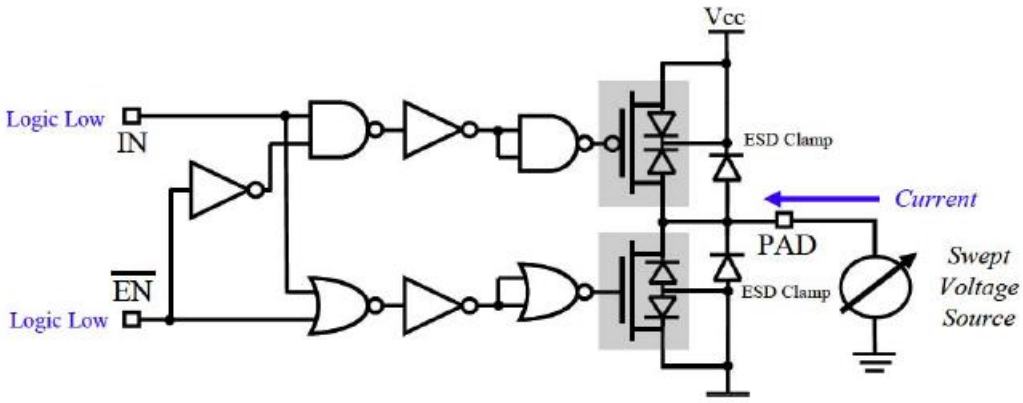

Figure 2.3. I-V Data Measurement setup [6]

All estimations are made at the yield hub (PAD). The buffer's information is then set to either logic low or logic high in the event that we are developing the pull down or pullup, respectively, information tables separately. The voltage source is then swept over - Vdd to 2Vdd while recording the current into the support. The full voltage run at the output is covered along these lines.

2.2.3 HSPICE Model

SPICE (Simulation Program with Integrated Circuit Emphasis) is a broadly used, open source analogue electronic circuit test system. It is a program utilized as part of the incorporated circuit and board-level plan to check the validity of a circuits outlines and to foresee circuit conduct [7]. The most conspicuous business forms of SPICE is HSPICE which initially popularized by Shawn and Kim Hailey of Meta Software, but is now claimed by Synopsys and PSPICE which is currently possessed by Cadence Design Systems [8].