UNIVERSITI SAINS MALAYSIA

First Semester Examination
2016/2017 Academic Session

December 2016 / January 2017

EEE 445 – DESIGN OF INTEGRATED ANALOG CIRCUITS

[REKABENTUK LITAR ANALOG BERSEPADU]

Duration 3 hours
[Masa : 3 jam]

Please check that this examination paper consists of **FIFTEEN (15)** pages of printed material before you begin the examination. This examination paper consist of two versions, The English version and Malay version. The English version from page **TWO (2)** to page **EIGHT (8**) and Malay version from page **NINE (9)** to page **FIFTEEN (15)**.

*Sila pastikan bahawa kertas peperiksaan ini mengandungi **LIMA BELAS (15)** muka surat bercetak sebelum anda memulakan peperiksaan ini. Kertas peperiksaan ini mengandungi dua versi, versi Bahasa Inggeris dan Bahasa Melayu. Versi Bahasa Inggeris daripada muka surat **DUA (2)** sehingga muka surat **LAPAN (8**) dan versi Bahasa Melayu daripada muka surat **SEMBILAN (9)** sehingga muka surat **LIMA BELAS (15)**.*

Instructions: This question paper consists of **SIX (6)** questions. Answer **FIVE (5)** questions. All questions carry the same marks.

*[**Arahan:** Kertas soalan ini mengandungi **ENAM (6)** soalan. Jawab **LIMA (5)** soalan. Semua soalan membawa jumlah markah yang sama]*

Use separate answer booklets for **PART A** and **PART B**
*[Gunakan dua buku jawapan yang berasingan bagi **BAHAGIAN A** dan **BAHAGIAN B**]*

Answer to any question must start on a new page.
[Mulakan jawapan anda untuk setiap soalan pada muka surat yang baru]

"In the event of any discrepancies, the English version shall be used".
[Sekiranya terdapat sebarang percanggahan pada soalan peperiksaan, versi Bahasa Inggeris hendaklah diguna pakai]

...2/-

ENGLISH VERSION

PART A

1. (a) Given Figure 1(a), derive the expression to relate I_{out} with I_{REF}. Neglect the channel-length modulation (λ = 0) effect for both transistors M_1 and M_2.

(20 marks)

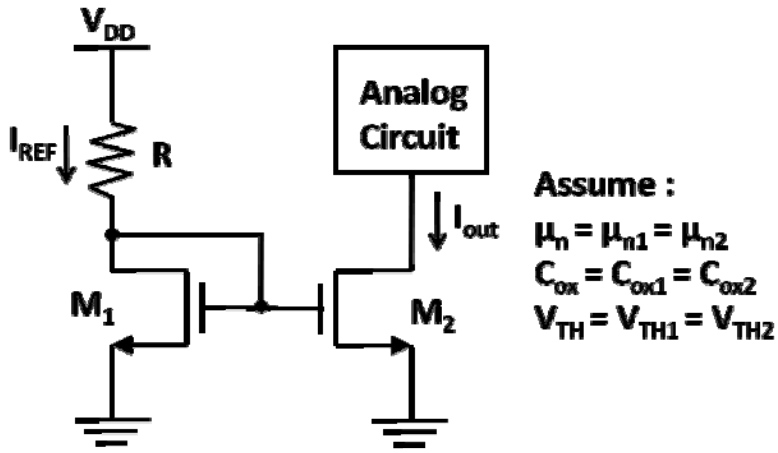

Figure 1(a)

(b) Referring to Figure 1(a) and the derived expression in question 1 (a), neglect the channel-length modulation (λ = 0) effect for both transistors M_1 and M_2. Calculate the required parameters in (i), (ii), (iii) and (iv). Given:

$$I_{REF} = 40\ \mu A,\ \mu_n C_{ox} = 120\ \mu A/V^2,\ V_{TH} = 0.3\ V,\ L_1 = L_2 = 0.2\ \mu m,$$
$$W_1 = 2\ \mu m,\ V_A' = 20\ V/\mu m$$

(i) Transistor M_2 channel width (W_2) so that I_{out} = 20 μA.

(10 marks)

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(ii) Output resistance (r_{02}) of current source. (10 marks)

(iii) Lowest possible of output voltage (V_{out}) to keep M_2 operating in saturation mode.

(15 marks)

(iv) Change of I_{out} (ΔI_{out}) if the change of V_{out} (ΔV_{out}) is + 1 V.

(15 marks)

(c) Figure 1(b) shows a complex design of analog circuits with single current mirror. If all of the transistors are operating in saturation mode, determine drain current (I_D) of each transistor i.e. M_2 to M_5 with respect to the reference current (I_{REF}). Neglect the channel-length modulation ($\lambda = 0$) effect for all the transistors.

(30 marks)

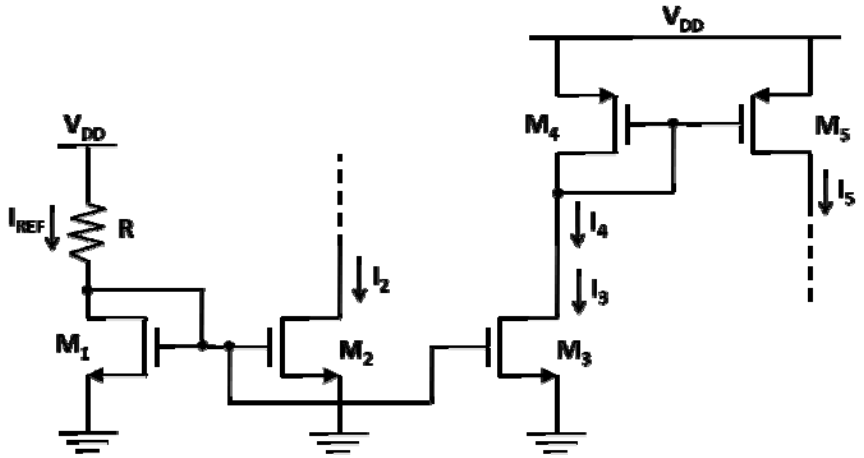

Figure 1(b)

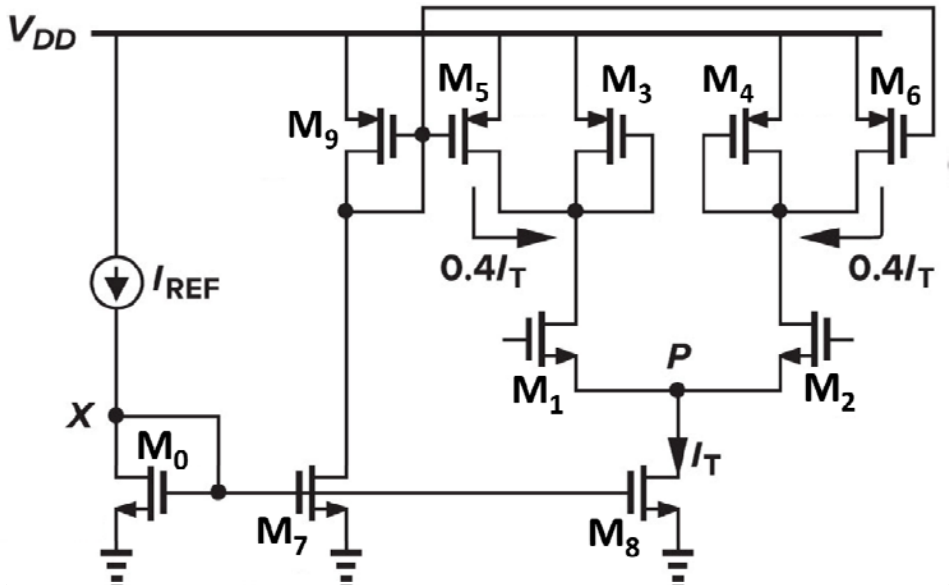

Figure 2

2 Given a differential amplifier with its corresponding current mirror as in Figure 2. By neglecting the channel-length modulation (λ = 0) effect for all the transistors, analyze the circuits and give your answer to the following questions. Given:

$$\mu_n = 294\ cm^2/V.s,\ \mu_p = 98\ cm^2/V.s,\ L = 0.13\ \mu m,\ C_{ox} = 13\ fF/um^2,$$
$$V_{eff,M0} = 0.101\ V,\ (W/L)_0 = (2/0.13)\ \mu/\mu$$

(a) What is the drain current I_D required for transistor M_0? (25 marks)

(b) Suppose if the tail current I_T is 150 μA, what are the drain currents required for the transistors M_7 and M_9.

(25 marks)

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(c) Find widths for transistors M_7, M_8 and M_9. Explain differences between sizes of pMOS and nMOS transistors.

(50 marks)

3.

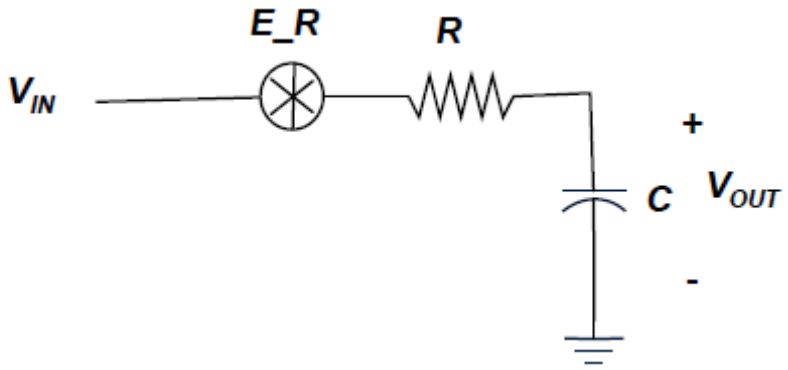

Figure 3

Based on Figure 3,

(a) Prove that, even though resistor provides the noise source, capacitor sets the total power of the total noise.

(70 marks)

(b) Calculate the thermal noise of the RC filter (R = 4 kΩ, C = 1 nF)

(30 marks)

PART B

4.

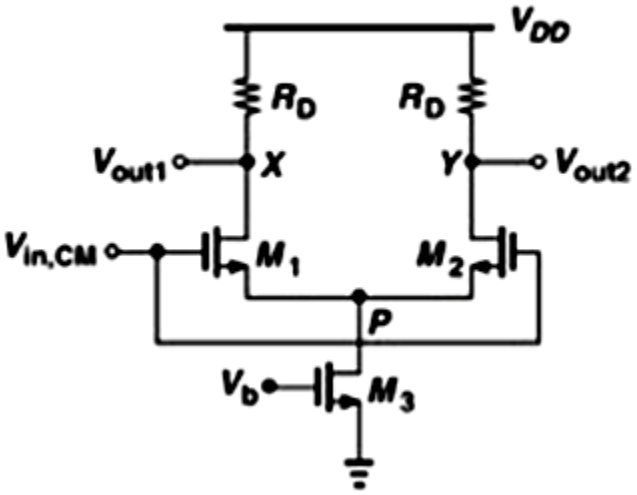

Figure 4

(a) Sketch the small signal differential voltage gain of the circuit shown in Figure 4, if V_{DD} varies from 0 to 3 V. Assume $(W/L)_{MI-3}$ = 50/0.5, V_{th} = 0.7 V, $\mu_n C_{ox}$ = 134 $\mu A/V^2$, $V_{in,CM}$ = 1.3 V, and V_b = 1 V.

(50 marks)

(b) Construct the plots of circuit in Figure 4 for a differential pair using PMOS transistor.

(50 marks)

5. (a) Transition frequency of a transistor defined as the frequency when the current gain is 1. Based on the given parameter associated to transistor (C_{gs} = 0.1 pF, g_m = 0.02 A/V, C_{gd} = 0.01 pF and C_{db} = 0.001 pF) in Figure 5, calculate the transition frequency.

(25 marks)

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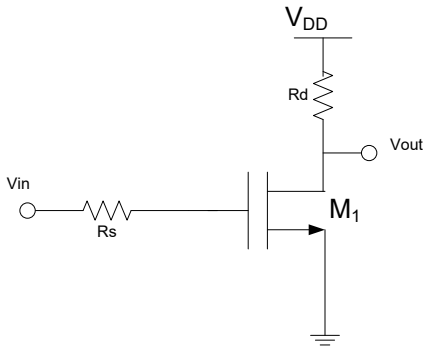

Figure 5

(b) The transfer function of above circuit (Figure 5) is,

$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{-g_m R_D}{(1+\frac{s}{\omega_{in}})(1+\frac{s}{\omega_{out}})}$$

(i) Determine the expression for input pole and calculate the value if Rs = 50 Ω, C_{gs} = 0.1 pF, g_m = 0.02 A/V, Rd = 500 Ω, C_{gd} = 0.01 pF and C_{db} = 0.001 pF .

(25 marks)

(ii) Determine the expression for output pole and calculate the value if Rs = 50 Ω, C_{gs} = 0.1 pF, g_m = 0.02 A/V, Rd = 500 Ω, C_{gd} = 0.01 pF and C_{db} = 0.001 pF.

(25 marks)

(iii) What is the required gain if the desired bandwidth is 20 MHz and the external load is 10 pF? With the capacitive load, what is your prediction of the stability of the circuit?

(25 marks).

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6. (a) Draw a simple resistor divider with gain = 0.5 followed by an amplifier (Gain =1) and low pass filter (fc = 1 MHz). ($R_1 = R_2 = 100$ k Ω, $R_{LP} = 100$ Ω).)

(10 marks)

(b) Find the noise density at low frequencies by assuming the low pass filter has no effect.

(50 marks)

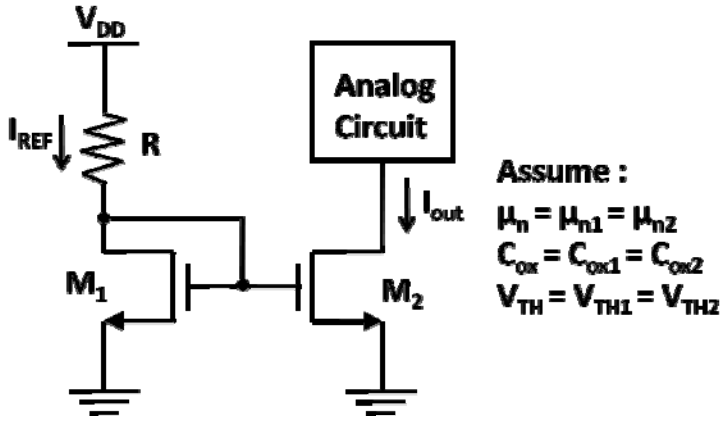
(c) Given a wafer cost is MYR 3600, a wafer yield = 70 %, a wafer diameter is 6 inch and estimated one die cost is MYR 16. With the details of the information of an Integrated Circuit (IC) design project , calculate the die area of the IC.

(40 marks)

VERSI BAHASA MALAYSIA
BAHAGIAN A

1. (a) Diberi Rajah 1(a), terbitkan persamaan untuk mengaitkan I_{out} dengan I_{REF}. Abaikan kesan pemodulatan panjang saluran (λ = 0) bagi kedua-dua transistor M_1 dan M_2.

(20 markah)



Rajah 1(a)

(b) Merujuk kepada Rajah 1(a) dan persamaan yang telah diterbitkan di soalan 1 (a), abaikan kesan pemodulatan panjang saluran (λ = 0) bagi kedua-dua transistor M_1 dan M_2. Kirakan parameter-parameter di (i), (ii), (iii) dan (iv). Diberi:

$$I_{REF} = 40\ \mu A,\ \mu_n C_{ox} = 120\ \mu A/V^2,\ V_{TH} = 0.3\ V,\ L_1 = L_2 = 0.2\ \mu m,$$
$$W_1 = 2\ \mu m,\ V_A' = 20\ V/\mu m$$

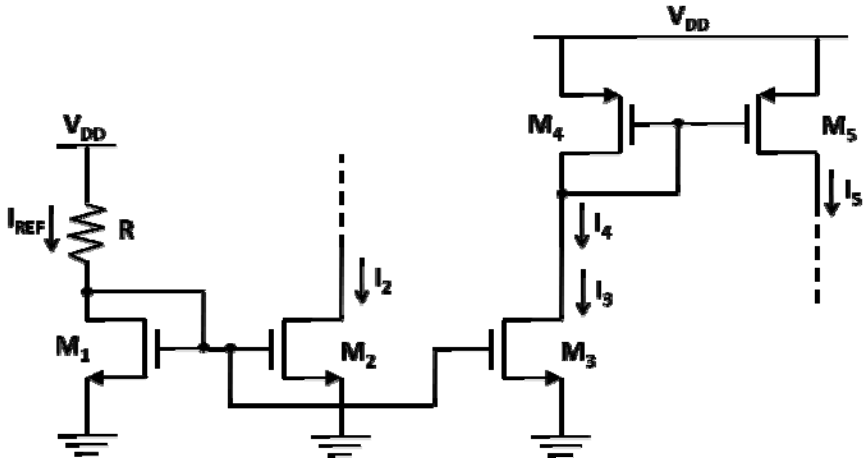
(i) Lebar saluran (W_2) transistor M_2 supaya I_{out} = 20 μA. (10 markah)

(ii) Rintangan keluaran (r_{02}) sumber arus. (10 markah)

(iii) Nilai terendah yang mungkin untuk voltan keluaran (V_{out}) untuk memastikan transistor M_2 beroperasi di dalam mod tepu. (15 markah)

(iv) Perubahan I_{out} (ΔI_{out}) jika perubahan V_{out} (ΔV_{out}) ialah + 1 V. (15 markah)

(c) Rajah 1(b) menunjukkan rekabentuk kompleks litar-litar analog dengan satu cermin arus. Jika kesemua transistor beroperasi di dalam mod tepu,tentukan arus salir untuk setiap transistor M_2 sehingga M_5 berpandukan arus rujukan (I_{REF}). Abaikan kesan pemodulatan panjang saluran (λ = 0) untuk kesemua transistor. (30 markah)



Rajah 1(b)

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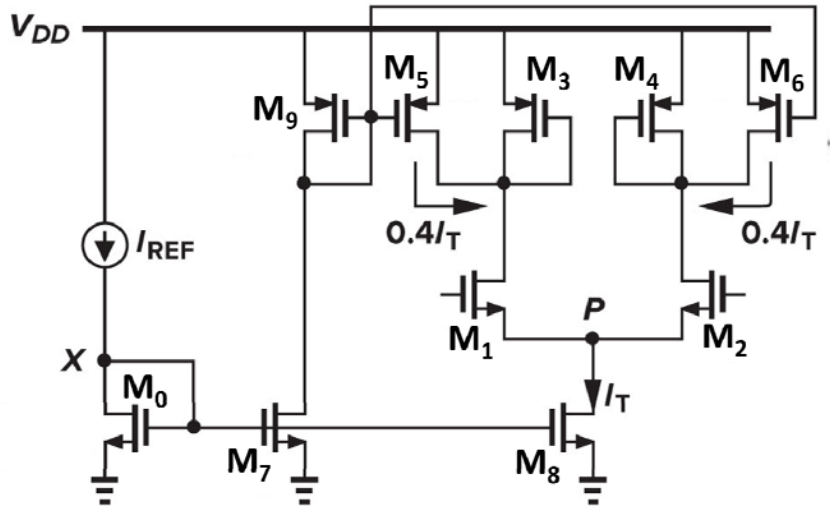

Rajah 2

2 Diberi sebuah penguatkuasa kebezaan dengan cermin arus seperti pada Rajah 2. Dengan mengabaikan kesan pemodulatan panjang saluran (λ = 0) untuk kesemua transistor, analisakan litar-litar tersebut dan jawab soalan-soalan berikut. Diberi :

$$\mu_n = 294\ cm^2/V.s,\ \mu_p = 98\ cm^2/V.s,\ L = 0.13\ \mu m,\ C_{ox} = 13\ fF/um^2,$$
$$V_{eff,M0} = 0.101\ V,\ (W/L)_0 = (2/0.13)\ \mu/\mu$$

(a) Apakah arus salir I_D yang diperlukan untuk transistor M_0? (25 markah)

(b) Diberi arus ekor I_T adalah 150 μA, apakah arus-arus salir yang diperlukan untuk transistor-transistor M_7 dan M_9.

(25 markah)

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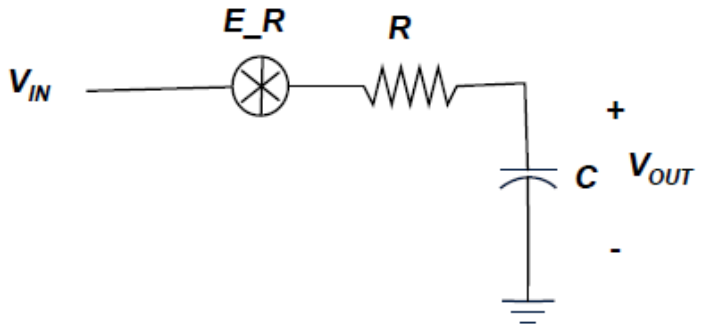
(c) Cari kelebaran-kelebaran bagi transistor M_7, M_8 dan M_9. Terangkan perbezaan di antara saiz transistor pMOS dan nMOS.

(50 markah)

3.



Rajah 3

(a) Buktikan bahawa, walaupun perintang adalah sumber hingar, kapasitor menetapkan jumlah kuasa bagi hingar voltan.

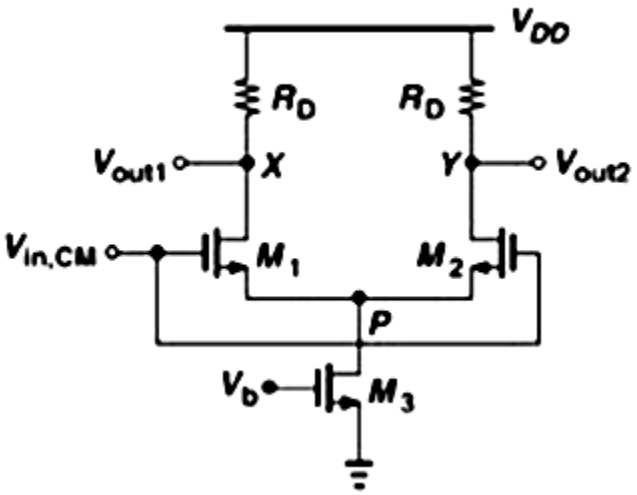
(70 markah)

(b) Kirakan hingar termal bagi penuras RC di atas. (R = 4 kΩ, C = 1 nF).

(30 markah)

BAHAGIAN B:

4.



Rajah 4

(a) Lukiskan gandaan voltan kebezaan isyarat kecil untuk litar seperti di Rajah 4 apabila V_{DD} diubah bermula 0 hingaa 3 V. Andaikan, $(W/L)_{MI-3}$ = 50/0.5, V_{th} = 0.7 V, $\mu_n C_{ox}$ = 134 μA/V^2, $V_{in,CM}$ = 1.3 V, and V_b = 1 V.

(50 markah)

(b) Bina atau lukis plot-plot untuk litar bagi Rajah 4 sekiranya NMOS digantikan dengan PMOS transistor.

(50 markah)

5. (a) Frekuensi alihan untuk transistor adalah frekuensi apabila gandaan arus menjadi 1. Berdasarkan parameter yang diberikan untuk transistor bagi Rajah 5 di bawah (C_{gs} = 0.1 pF, g_m = 0.02 A/V, C_{gd} = 0.01 pF and C_{db} = 0.001 pF). Kirakan alihan frekuensi.

(25 markah)

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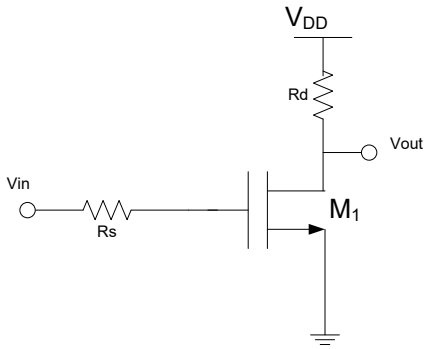

Rajah 5

(b) Rangkap pindah untuk litar di atas ialah,

$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{-g_m R_D}{(1+\frac{s}{\omega_{in}})(1+\frac{s}{\omega_{out}})}$$

(i) Tentukan ungkapan untuk kutub masukan dan kirakan nilai ia sekiranya Rs = 50 Ω, C_{gs} = 0.1 pF, g_m = 0.02 A/V, Rd = 500 Ω, C_{gd} = 0.01 pF dan C_{db} = 0.001 Pf.

(25 markah)

(ii) Tentukan ungkapan untuk kutub keluaran dan kirakan nilai ia sekiranya Rs = 50 Ω, C_{gs} = 0.1 pF, g_m = 0.02 A/V, Rd = 500 Ω, C_{gd} = 0.01 pF dan C_{db} = 0.001 pF.

(25 markah)

(iii) Apakan nilai gandaan yang diperlukan sekiranya jalur yang ditentukan ialah 20 MHz?. Beban ialah 10 pF. Dengan bebanan tersebut, apa pandangan anda mengenai kestabilan litar itu?

(25 markah).

... 15/-

6. (a) Lukiskan satu pembahagi perintang mudah dengan gandaan = 0.5 dan diikuti dengan satu penguat (gandaan = 1) dan penuras laluan-rendah (fc = 1 MHz). ($R_1 = R_2$, R_{LP} = 100 Ω).

(10 markah)

(b) Carikan ketumpatan hingar pada frekuensi-frekuensi rendah dengan menganggap penuras laluan-rendah tidak memberi kesan kepada hingar tersebut.

(50 markah)

(c) Diberikan kos wafer ialah RM 3600, hasil wafer = 70 %, diameter wafer ialah 6 inci dan anggaran kos untuk satu dadu ialah RM 16. Dengan maklumat yang terperinci untuk satu projek rekabentuk litar bersepadu, kirakan luas untuk dadu litar bersepadu tersebut.

(40 markah)

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