UNIVERSITI SAINS MALAYSIA

First Semester Examination
2016/2017 Academic Session

December 2016 / January 2017

EEE 241 – ANALOG ELECTRONIC I

[ELEKTRONIK ANALOG I]

Duration 3 hours
[Masa : 3 jam]

Please check that this examination paper consists of **THIRTEEN (13)** pages of printed material before you begin the examination. This examination paper consist of two versions, The English version and Malay version. The English version from page **TWO (2)** to page **SEVEN (7**) and Malay version from page **EIGHT (8)** to page **THIRTEEN (13)**.

*Sila pastikan bahawa kertas peperiksaan ini mengandungi **TIGA BELAS (13)** muka surat bercetak sebelum anda memulakan peperiksaan ini. Kertas peperiksaan ini mengandungi dua versi, versi Bahasa Inggeris dan Bahasa Melayu. Versi Bahasa Inggeris daripada muka surat **DUA (2)** sehingga muka surat **TUJUH (7)** dan versi Bahasa Melayu daripada muka surat **LAPAN (8)** sehingga muka surat **TIGA SEBELAS (13)**.*

Instructions: This question paper consists of **SIX (6)** questions. Answer **FIVE (5)** questions. All questions carry the same marks.

*[**Arahan:** Kertas soalan ini mengandungi **ENAM (6)** soalan. Jawab **LIMA (5)** soalan. Semua soalan membawa jumlah markah yang sama]*

Use separate answer booklets for **PART A** and **PART B**
*[Gunakan dua buku jawapan yang berasingan bagi **BAHAGIAN A** dan **BAHAGIAN B**]*

Answer to any question must start on a new page.
[Mulakan jawapan anda untuk setiap soalan pada muka surat yang baru]

"In the event of any discrepancies, the English version shall be used".
[Sekiranya terdapat sebarang percanggahan pada soalan peperiksaan, versi Bahasa Inggeris hendaklah diguna pakai]

ENGLISH VERSION

PART A

1. (a) The difference between passive and active circuits for low pass filter and high pass filter is essential in analog design. Therefore,

(i) Draw the circuits for both active and passive low pass and high pass filters.

(20 marks)

(ii) Write down the expression for cut-off frequencies for all the four circuits.

(20 marks)

(b) Design a passive single-pole single-zero high-pass filter. Given value for the circuit: $R_1 = 8.2\ k\Omega$, $R_2 = 20\ k\Omega$ and $C = 0.01\ \mu F$.

(i) Find the mid-band gain, A_o and cut-off frequency, f_L for the filter.

(30 marks)

(ii) Based on the calculated values of A_o and f_L in (i), write the transfer function, $A_V(s)$ for the circuit.

(20 marks)

(iii) Sketch the bode (magnitude) plot and label the gain, A_o and the cut-off frequency f_L of the filter clearly.

(10 marks)

2. Consider the circuit in Figure 2. Op amp has an open-loop gain of 80 dB, an input resistance, R_{id} of 25 kΩ, and output resistance, R_o of 1 kΩ. Assume that the op amp is driven by a signal voltage with 100-kΩ source resistance, and output voltage is connected to load resistance of 5-kΩ. Feedback network is implemented with R_F = 36 kΩ. Hence,

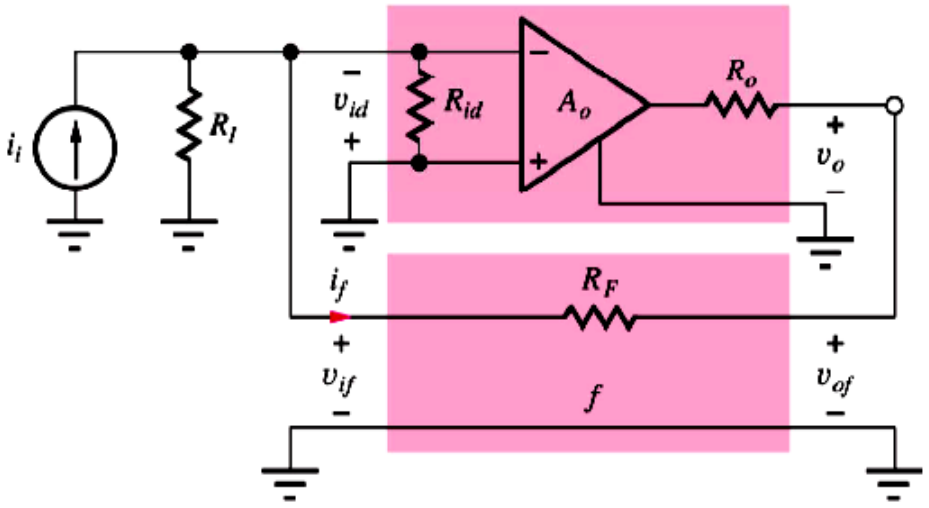

Figure 2

(a) Calculate input resistance, R_{in} of the circuit. (30 marks)

(b) Calculate output resistance, R_{out} of the circuit. (30 marks)

(c) Calculate closed loop gain, A_v of the circuit. (40 marks)

3. (a) Define finite common-mode rejection ratio. Use relevant expressions to support your explanation.

(30 marks)

(b) Consider digital multi-meter circuit (DMM) as in Figure 3. Based on that figure, find the value for:

(i) Differential-mode input voltage (V_{DM}). (15 marks)

(ii) Common-mode input voltage (V_{CM}). (15 marks)

(iii) CMRR (in dB) if the percentage of error of the DMM of 0.2 % is needed.

(20 marks)

(iv) Output voltage, v_o if the DMM is having the differential-mode gain of 32 dB.

(20 marks)

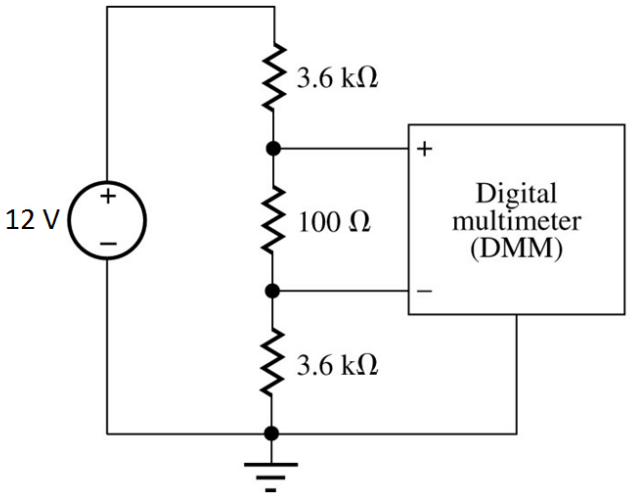

Figure 3

PART B

4. Derive:

(a) The output resistance of common gate configuration as in Figure 4.

(50 marks)

(b) Transconductance Gm of the common gate configuration as in Figure 4.

(50 marks)

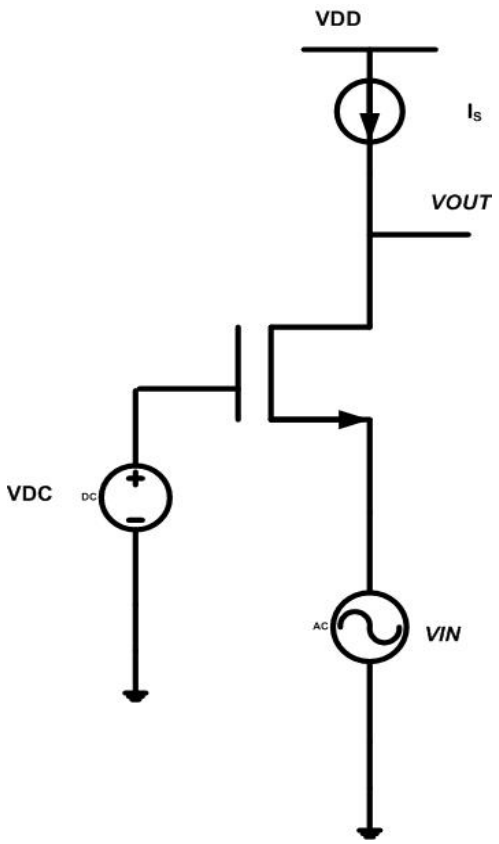

Figure 4

5. (a) Referring to Figure 5, state whether C_1, C_2 and C_3 are coupling or bypass capacitors. What are the functions of these capacitors?

(40 marks)

(b) Calculate the voltage gain of the common-emitter amplifier in Figure 1 with and without capacitor C_2, if the transistor has $\beta_o = 150$, $\beta_F = 160$, $V_T = 26$ mV and $V_{BE} = 0.7$ V.

(60 marks)

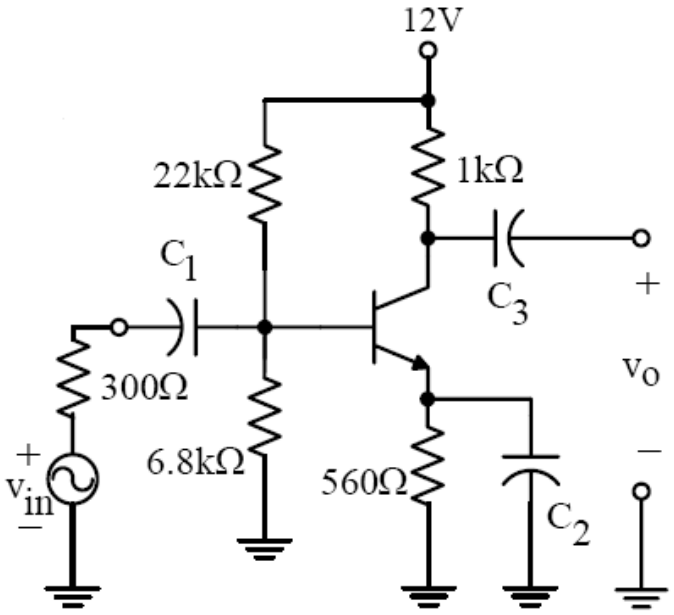

Figure 5

6. Figure 5 shown MN1 has gate connected to the drain.

(a) Draw small signal equivalent circuit. (30 marks)

(b) Derive the expression of R_{out}. (50 marks)

(c) Does diode provide high or low resistive path ? (20 marks)

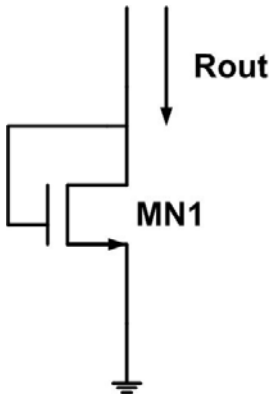

Figure 6

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VERSI BAHASA MELAYU

BAHAGIAN A

1. (a) Perbezaan di antara litar pasif dan aktif bagi penapis laluan rendah dan tinggi adalah penting di dalam rekabentuk analog. Maka,

(i) Lakarkan litar-litar aktif dan pasif penapis laluan rendah dan tinggi.

(20 markah)

(ii) Nyatakan ungkapan-ungkapan bagi frekuensi potong bagi kesemua empat litar tersebut.

(20 markah)

(b) Rekabentuk satu litar penapis laluan tinggi pasif 'single-pole single-zero'. Nilai bagi komponen litar adalah: $R_1 = 8.2\ k\Omega$, $R_2 = 20\ k\Omega$ and $C = 0.01\ \mu F$.

(i) Kirakan gandaan jalur-tengah, A_o dan frekuensi potong, f_L bagi penapis tersebut.

(30 markah)

(ii) Berdasarkan nilai kiraan A_o dan juga f_L, dalam (i), tentukan fungsi pindah $A_V(s)$ bagi litar tersebut.

(20 markah)

(iii) Lakarkan plot Bode (magnitud) dan labelkan gandaan A_o dan frekuensi potong, f_L bagi penapis tersebut dengan jelas.

(10 markah)

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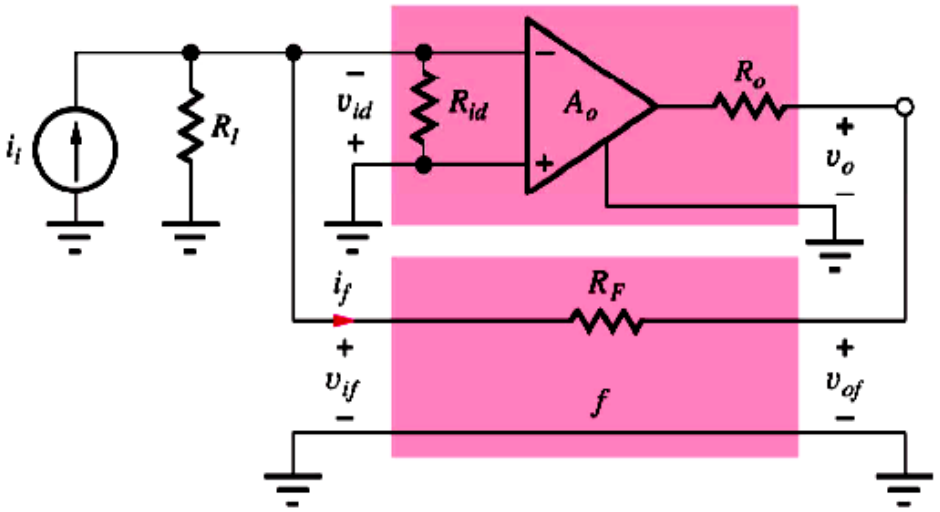
2. Pertimbangkan litar Rajah 2. Penguat kendalian mempunyai nilai gandaan gelung-terbuka sebanyak 80 dB, rintangan masukan, R_{id} 25 kΩ dan juga rintangan keluaran, R_o 1 kΩ. Andaikan bahawa penguat kendalian tersebut dipacu oleh isyarat voltan masukan dengan rintangan sumber bernilai 100-kΩ, dan voltan keluaran disambungkan kepada rintangan beban 5-kΩ. Rangkaian suapbalik dilaksanakan menggunakan R_F = 36 kΩ. Maka,



Rajah 2

(a) Kirakan rintangan masukan, R_{in} bagi litar. (30 markah)

(b) Kirakan rintangan keluaran, R_{out} bagi litar. (30 markah)

(c) Kirakan gandaan gelung-tertutup, A_v bagi litar. (40 markah)

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3. (a) Takrifkan had nisbah penolakan ragam sepunya. Gunakan formula-formula berkaitan untuk menjelaskan lagi penerangan anda.

(30 markah)

(b) Pertimbangkan litar multi-meter digital (DMM) seperti di dalam Rajah 3. Berdasarkan litar tersebut, dapatkan nilai bagi:

(i) Voltan masukan mod-beza (V_{DM}). (15 markah)

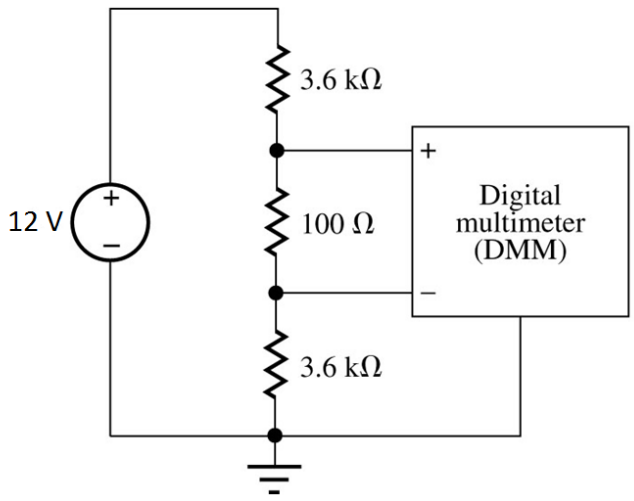
(ii) Voltan masukan ragam sepunya (V_{CM}). (15 markah)

(iii) CMRR (dalam dB) jika peratus ralat sebanyak 0.2 % diperlukan oleh DMM tersebut.

(20 markah)

(iv) Voltan keluaran, v_o jika DMM mempunyai nilai gandaan mod-beza sebanyak 32 dB.

(20 markah)



Rajah 3

BAHAGIAN B

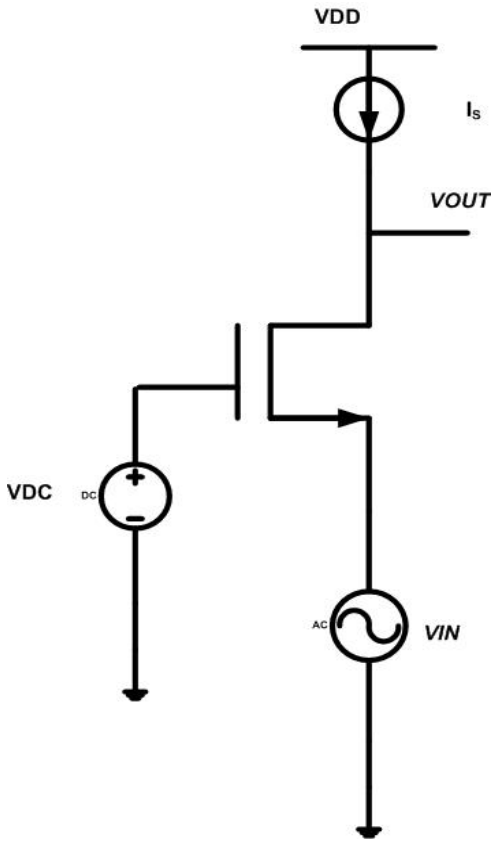
4. Terbitkan

(a) Rintangan keluaran konfigurasi get sama seperti di dalam Rajah 4.

(50 markah)

(b) Transkonduktans Gm bagi konfigurasi get sama seperti di dalam Rajah 4.

(50 markah)



Rajah 4

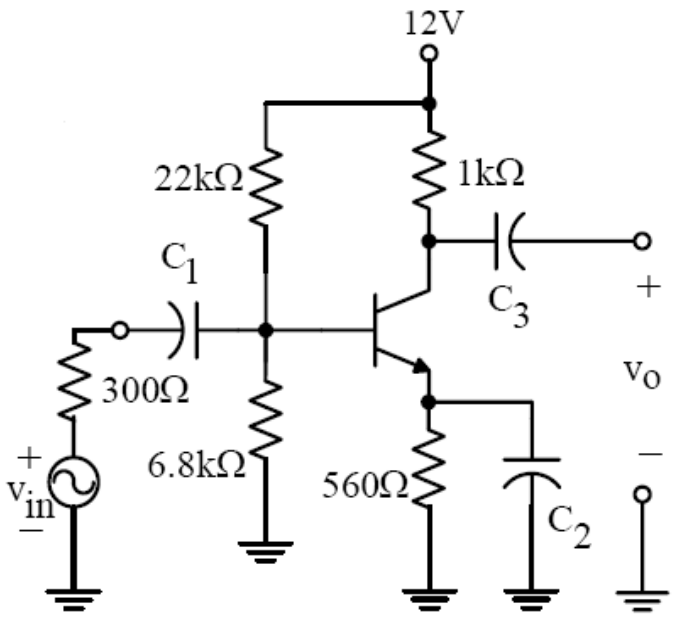
5. (a) Merujuk kepada Rajah 5, nyatakan sama ada C_1,C_2 dan C_3 adalah kapasitor gandingan atau pirau. Apakah fungsi kapasitor-kapasitor ini?

(40 markah)

(b) Kirakan gandaan voltan bagi penguat pemancar-sepunya dalam Rajah 5 dengan dan tanpa kapasitor C_2, jika transistor mempunyai $\beta_o = 150$, $\beta_F = 160$,

$V_T = 26$ mV dan $V_{BE} = 0.7$ V.

(60 markah)



Rajah 5

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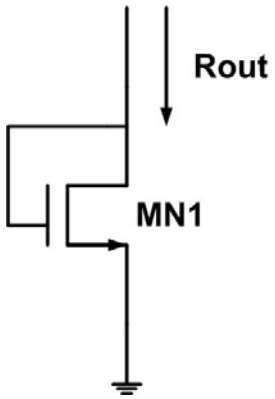
6. Rajah 6 menunjukkan MN1 pintu dihubungkan ke parit.

(a) Lukis isyarat kecil litar. (30 markah)

(b) Dapatkan persamaan R_{out}. (50 markah)

(c) Adakah diod menyediakan laluan berintangan tinggi ataupun rendah? (20 markah)



Rajah 6

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