TIMING PERFORMANCE ENHANCE FOR ROUTING CHANNEL IN 28NM FPGA CHIP

By

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List of Abbreviations

Abbreviation	Meaning
ASIC	Application Specific Integration Circuit
Best Case	High Voltage, Low Temperature, Fast Process
DRC	Design Rule Check
ECO	Engineering Change Order
Fast Corner	Faster Process for Hold Time Analysis
FPGA	Field Programmable Gate Array
ICC	IC Compiler Tool
IP Owner	Intellectual Property Owner
LVS	Layout versus Schematic
MCMM	Multi-Corners Multi-Modes
Max Delay	Maximum Delay
Min Delay	Minimum Delay
PVT	Process Voltage Temperature
PT	Prime Time Tool
PERL	Practical Extraction and Report Language
RC	Resistance and Capacitance
RCbest	Minimum Resistance Minimum Capacitance
RCworst	Maximum Resistance Maximum Capacitance
SPEF	Standard Parasitic Extended Format
STA	Static Timing Analysis
SDC	Synopsys Design Constraints
Slow Corner	Slowest Process for Setup Time Analysis
TCL	Tool Command Language
TAT	Turnaround Time
Verilog Netlist	Gate Level Netlist (Hardware Description Language)
Worst Case	Low Voltage, High Temperature, Slow Process

PENINGKATAN PRESTASI MASA UNTUK SALURAN LALUAN DALAM 28NM CIP FPGA

ABSTRAK

Dalam reka bentuk FPGA, saluran laluan bertindak sebagai penyambung antara kawasan dalaman dan luaran. Dengan pertumbuhan get kiraan yang semakin pantas serta rumit dalam proses nod 28nm, keperluan masa daripada reka bentuk ini adalah sukar untuk mencapai perubahan untuk semua PVT. Penganggaran masa yang terlebih bukan sahaja menyebabkan kegagalan dalam pencapaian masa malahan mengakibatkan penampan yang tidak realistik wujud dalam saluran reka bentuk. Laluan berkemungkinan dinyatakan dengan pelbagai kekangan masa oleh pemilik IP. Laluan masa tidak akan dianalisis dan dioptimumkan apabila kekangan masa hilang dan sambungan yang tidak sah muncul dalam saluran reka bentuk. Secara tidak langsung, ini mengakibatkan analisis prestasi masa tidak mencapai tahap yang dikehendaki. Kewujudan pelanggaran masa yang banyak dalam saluran reka bentuk akan memanjangkan masa pembangunan reka bentuk. Masa pengesahan aliran dibangunkan untuk mengesahkan isu-isu masa pada peringkat permulaan reka bentuk dan bertujuan untuk menghasilkan keputusan masa yang lebih bagus dan seterusnya meningkatkan prestasi masa. Lelaran ECO dan usaha pencapaian masa boleh diperbaiki dengan melaksanakan aliran pengesahan masa dan aliran pelanggaran masa secara automatik. Contoh digunakan ujian kes untuk menilai aliran pengesahan masa dan aliran pelanggaran masa secara automatik. Dengan melaksanakan aliran pengesahan masa, keputusan masa boleh meningkat sebanyak 65.26% dalam memenuhi penyediaan masa dan peningkatan sebanyak 65.38% dalam memenuhi penahanan masa. Kesimpulannya, satu proses berjaya dihasilkan yang mampu mengenal pasti isu-isu masa dan meningkatkan prestasi masa.

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ABSTRACT

In FPGA design, the routing channel acts as the access area for interconnect in between the core and the periphery. With the rapid growth of gate counts and complexity of routing channel design in 28nm process node, the timing requirement of the design has difficulty to be met across entire PVT corner variations. Among the timing closure issue occurs due to over-estimation of timing windows gets worse and cause unrealistic guard-banding occurs in routing channel design. A path might be also specified to multiple timing constraints by IP owners. The timing paths will not be analyzed and optimized when the missing timing constraints and invalid connection arisen in routing channel design. Consequently, the timing performance analysis is not performed. Due to the complication mentioned, timing verification flows are developed to verify the timing issues at initial design stage with the intention to produce better timing results to enhance timing performance.ECO iterations and timing convergence efforts are improved by timing verification flows and automated fixing timing violations flow. The timing verification flows are classified as missing timing verification flow, timing constraints conflict verification flow, unrealistic timing constraints verification flow and stage delay calculator. A design example is used as a test case to evaluate the timing verification flows and automated fixing timing violations flow. Significant timing improvement is observed in this test case. The timing results after timing verification flows shows 65.26% improvement on setup time closure and 65.38% improvement on hold time closure. In conclusion, the timing verification flows and automated fixing flow are successfully developed to identify the timing issues to improve timing performance.

CHAPTER 1

INTRODUCTION

1.1 Introduction

A Field Programmable Gate Array (FPGA) is a general-purpose, multi-level programmable logic device that is customizable by the end users. FPGA combines the logic integration benefits of custom very large scale integration (VLSI) with the design, production, and time-to-market advantages of standard logic integrated circuit (IC). Nowadays FPGA has become a new approach to application-specific integrated circuit (ASIC) design, which can dramatically reduce manufacturing turn-around time and cost for low volume manufacturing(Lipo Wang, 2005). Overall Altera FPGA architecture consists of core and periphery section. The core comprises the array of logic blocks called Logic Array Block (LAB), memory and digital signal processing (DSP).Periphery section contains the input/output (I/O) buffers circuitry. Depending on the design, multiple I/O pads may fit into the height of one row or the width of one column in the array (Toronto, 2000). A layer of space called routing channel exists in between of the core and periphery. The routing channel acts as the public-access area for interconnect in between the core and the periphery. Generally routing channel consists of variation of wire widths and buffers insertion due to performance and signal integrity purpose. A buffer is a gate with typically two serially-connected inverter to regenerate a signal without changing

functionality. Buffers can improve timing delays, signal integrity and coupling-induced delay variation.(Kahng, et al., 2011)

Intellectual property (IP) serves as the building blocks to construct the full chip design**.** Each defined IP is designed specifically and is optimized in terms of power and area.(ALTERA, 2011). With the rapid growth of gate counts and complexity of routing channel in 28nm process node, it is difficult to meet the timing requirement of the design across process-voltage-temperature (PVT) corners. PVT is source of variation that can be process variation, supply voltage and operating temperature. This induced a challenge in timing convergence across all the PVT. Other than that, it also leads to increase of timing closure effort in analyzing multi-corners and multi-modes (MCMM) during phase of static timing analysis (STA). With MCMM technique, it can achieve timing closure across all design modes and process corners. Static timing analysis is a method of computing the expected timing of a digital circuit without requiring simulation (Chadha, 2009). Timing constraints files for routing channel design consist of max delay constraints and min delay constraints for specifying to timing paths. Max delay is maximum amount of delay for the timing paths. Min delay is the minimum amount of delay for the timing paths.

The routing channel is divided into top routing channel, bottom routing channel, left routing channel and right routing channel as shown in figure 1-1. Indirectly the routing channel establishes an interconnection in between of intellectual property (IP) blocks as shown in figure 1-2.With numerous IP blocks spread between the FPGA core and periphery, the routing channel is a heavily

congested highway. With this phenomenon, the number of routing tracks in routing channel design is affected.

Each of the paths in routing channel design in 28nm process node is specified by max delay constraints and min delay constraints for timing optimization. Thus, the timing performance will be enhanced after timing optimization for routing channel design. The timing constraints issue occurs when the timing paths are unconstrained in routing channel design. The missing timing constraints issue leads to unconstraint paths are not be optimized. Therefore, the timing performance in routing channel will be affected due to missing timing constraints issue. Due to design complexity, a path is specified with multiple constraints by different owners. The situation leads to timing constraints conflict issue occurs in routing channel design. The timing performance is affected due to invalid timing constraints are specified in routing channel design. Due to process variation and dynamic effects in 28nm process node, the over-estimation of timing windows gets worse. As a result, unrealistic guard-banding occurs.(Drew Plant, 2012). Unrealistic timing constraints are no exception to routing channel design. Therefore, timing performance in routing channel design may not be performed as intended.

In order to enhance timing performance for routing channel, the timing verification flows are developed to identify the timing issues mentioned as above. The timing verification flows are able to identify the missing timing constraint paths. Besides that, the timing verification flows can identify timing constraints conflict issue in routing channel design. In order to prevent unrealistic timing

constraints issue occurs, the timing verification flow can estimate max delay constraints in slow corner and min delay constraints in fast corner for owners as reference and compute the ratio of max delay in slow corner and min delay in fast corner for each of the paths. The ratio is to determine whether the paths have realistic timing margin to achieve timing closure.

Automated fixing timing violations flows are developed to align with achieving engineering change order (ECO) turnaround time. Automated fixing timing violations flow is mainly automatically fixing the setup time violations and hold time violations.

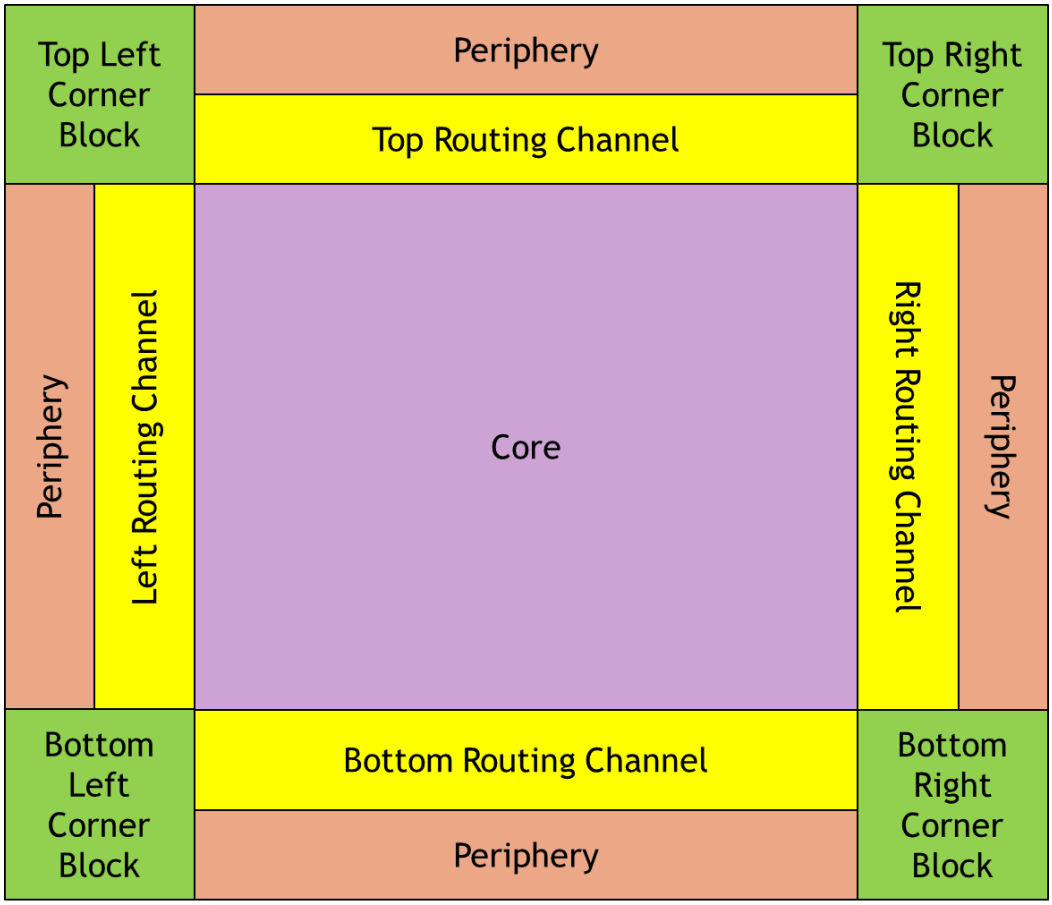

Figure 1-1 Abstract of Routing Channel Design

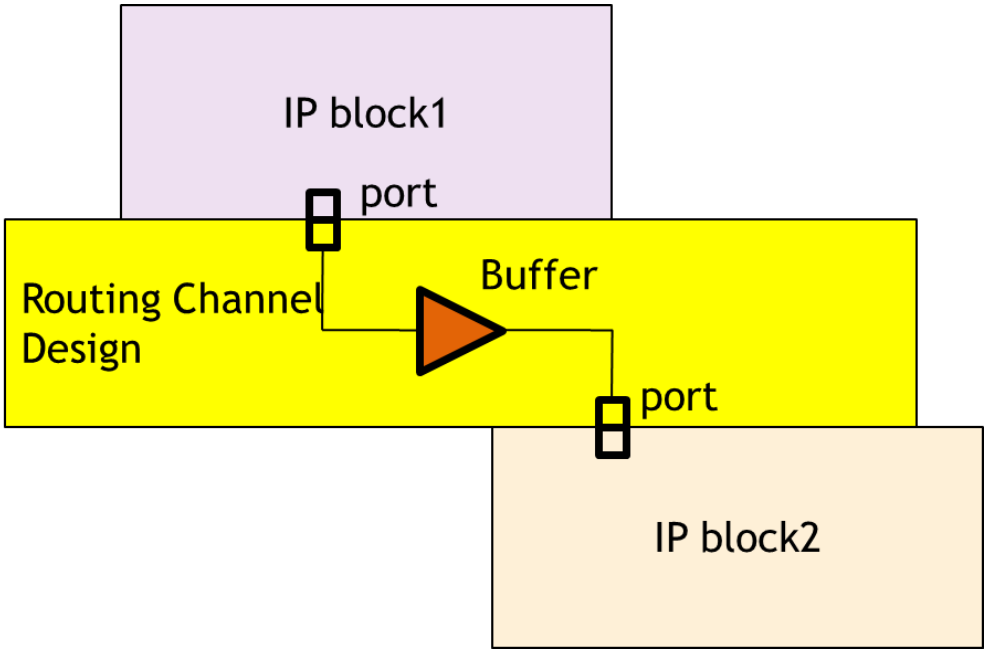

Figure 1-2 Abstract of Intellectual Property Connectivity through Routing Channel Design

1.2 Problem statement

To obtain a high quality timing constraint is a main goal for routing channel. Timing closure issue occurs due to pessimistic timing constraints are being specified. For example the ratio of max delay path in process slow corner and min delay path in process fast corner is over constrained. There are two problems occur in routing channel design.

1) Pessimistic timing constraints
2) False timing constraint definition

The routing channel path might be specified to multiple timing constraints. The situation often leads to design conflict which occurs in the routing channel. As example, Figure 1-3 shows different intellectual property (IP) blocks connect to a single routing channel net. Therefore, it can make timing closure difficult to achieve due to invalid timing constraint is specified in the design. Table 1-1 shows the scenario of conflict timing constraints that occur in the design.

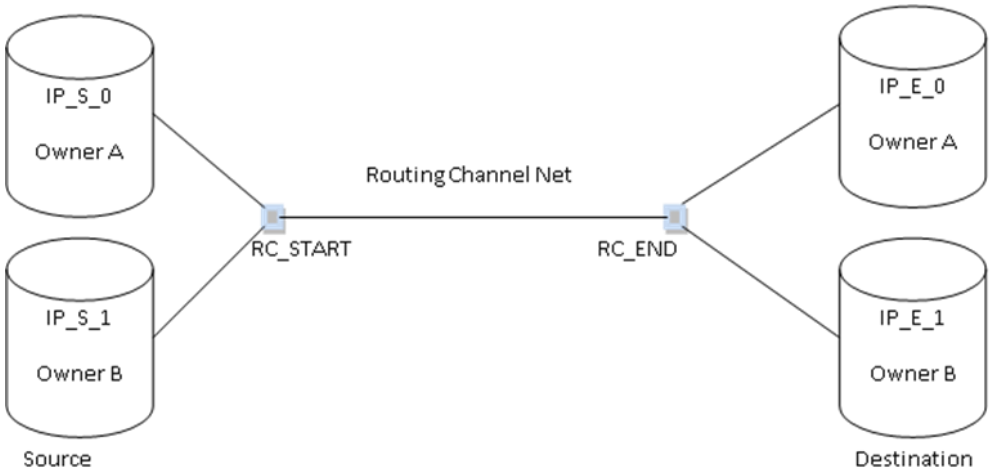

Figure 1-3Conflict Timing Constraints Issue

Table 1-1 Scenario of Conflict Timing Constraints

Mode	Constraints	RC_FROM	RC_TO	IP_FROM	IP_TO	OWNER_NAME
set_max_delay	0.12	RC_START	RC_END	IP_S_0	IP_E_0	Owner A
set_max_delay	0.22	RC_START	RC_END	IP_S_1	IP_E_1	Owner B
set_min_delay	0.01	RC_START	RC_END	IP_S_0	IP_E_0	Owner A
set_min_delay	0.02	RC_START	RC_END	IP_S_1	IP_E_1	Owner B

Missing timing constraint is another part of quality timing issue observed. The result will be invalid if missing timing constraints is discovered after physical implementation stage. The path will not be analyzed and timing optimization will

not be performed if its timing constraints not specified. Therefore missing timing constraints issue influences the timing performance in FPGA.

Another situation which causes the path not analyzed is due to false timing constraint definition. This constraint that is not set correctly will be discarded during the simulation. For example in synthesis stage, bidirectional bus ports will be translated to be output ports in the Verilog netlist. Figure 1-4 shows the net connectivity before synthesis. After synthesis, the portB[10] is unintentionally translated to be output instead of input port as shown in figure 1-5. Therefore, output port is explicitly being driver in the Verilog netlist.

Figure 1-4 Connectivity before Synthesis

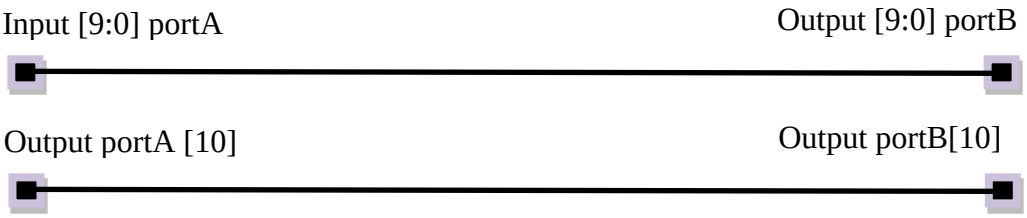

Figure 1-5 Connectivity after Synthesis

The cell performances are typically analyzed at different point of the parameter space, denoted as process-voltage-temperature corners (Manfred Dietrich,Joachim Haase, 2012). Therefore, the different cells have an individual

delay value stored in the different process-voltage-temperature corners library. As total delay path is caused by cell delay and RC parasitic delay across process-voltage-temperature corners. Cell delay mainly contributes to total path delay regardless of RC parasitic delay. Design complexity, process and manufacturing variability have been triggered the needs of multi-corners multi-modes (MCMM) for achieving timing closure (MULGAONKAR, 2009). There are more than 20 of process-voltage-temperature (PVT) corners timing analysis required to perform for routing channel design in 28nm. As a result, more effort to achieve timing convergence is needed due to unique timing violations across different PVT. It also leads to numerous timing violations exist in the routing channel design during phase of static timing analysis (STA). Design cycle turnaround time (TAT) is also a concern due to numerous timing violations exist in routing channel design.

1.3 Objective

The objective of this thesis is to develop timing verification flows to detect timing issues at an initial design stage in 28nm process node. The lesser false timing violations will be seen in static timing analysis if the developed timing verification flows can help to produce better timing results. It may improve engineering change order iterations and lesser timing convergence effort. The methodology of timing verification flowsis created to verify the timing across the entire PVT corners. The flow will be able to detect:-

1) Unrealistic timing constraints due to timing over constraint.
2) Timing constraints conflicting due to human inconsistency.

3) Missing timing constraints.

4) Invalid definition for timing constraints which causes it is not fulfilled.

The flows will also able to run multiple process-voltage-temperature (PVT) corners and complete in reasonable duration.

1.4 The Project Development Scope

The project development scope is covered as follow:

1) Develop the methodology of timing verification flows.
    a) The timing verification flows are classified as four types of verification flows, such as
        i) Missing timing constraints verification flow
        ii) Timing constraints conflict verification flow
        iii) Unrealistic timing constraints verification flow
        iv) Stage delay calculator
2) Develop the methodology of automated fixing timing violations flows.
3) Create test case to verify timing results before and after implemented timing verification flows.
4) Create test case to verify timing results before and after implemented automated fixing timing violations flows.

1.5 Project Contribution

The contribution of this project leads to two things. The first thing is avoiding numerous timing violations to enhance timing performance in routing channel design in 28nm process node. The second thing is achieving less that 60 percent error on true result to improve ECO turnaround time and lesser timing convergence effort.

1.6 Thesis Outline

Five chapters are covered by the thesis, as well as entire chapters are interpreted in the following.

Chapter 1 discusses about overall of thesis that is covered by introduction, problem statement, and objective and project development scope.

Chapter 2 discusses about three types of relevant methods comparison such as method of detecting missing timing constraints, method of detecting timing constraints conflict and method of automated repair of crosstalk violations and timing violations. Besides that, timing violations, design rule check violations and process-voltage-temperature variations are discussed. The method and definition of Elmore Delay Model are briefly described.

Chapter 3 mainly describes the present invention relates to methods of the timing verification flows. The flow chart of the timing verification flows is also presented. The relation in timing verification flows is also discussed in details. The methods for each of the timing verification flows are described. Besides that, the flow charts for each of timing verification flows are also illustrated.

Chapter 4 initially presents the ways for analyzing maximum delay for setup time and minimum delay for hold time in Prime Time are also described in details and illustrated in figures. The effectiveness of timing convergence is evaluated by comparing before and after implemented timing verification flows. The viability and effectiveness for each of the timing verification flows is also evaluated. Besides that, the effectiveness of timing closure after implemented automated fixing timing violations is described in details as well.

Chapter 5 is the last chapter to presents the conclusions of the thesis. The result improvements for timing verification flows and automated fixing timing violations flow are concluded in chapter 5. The results improvements for each of the timing verification flows are also discussed. Besides that, the enhancement of future works is briefly discussed.

CHAPTER 2

LITERATURE REVIEW

The previous methods were developed to avoid the timing violations and design rule check (DRC) violations existing in design during static timing analysis (STA) phase. There are unique timing violations and DRC violations across different process-voltage-temperature variations. Chapter 2 presents existing methods for detecting missing constraints, detecting timing conflict and automated repair of crosstalk violations and timing violations. The timing violations, design rule check violations and process-voltage-temperature variations are also briefly explained. Besides that, the Elmore delay model is an analytical model for RC interconnects delay estimation. The discussion of Elmore delay model is presented in this chapter.

2.1 Existing Methods for Detecting Timing Issues

Previously, there were various methods developed to perform turnaround time optimization and verification for ASIC design. However, there are three types of methods found which are most suitable to the thesis in the following.

1) Method for detecting missing timing constraints (ALTERA, 2009).
2) Method for detecting timing constraints conflict (Suo Ming Pu, 2010).