UNIVERSITI SAINS MALAYSIA

Supplementary Semester Examination
Academic Session 2004/2005

May 2005

EEE 520 – EMBEDDED MICROPROCESSOR SYSTEM

Duration: 3 hours

Please check that this examination paper consists of FIVE (5) pages of printed material before you begin the examination.

This paper contains SIX questions.

Instructions: Answer **FIVE** questions. If a candidate answer more than five questions, only the first five answered will be examined and awarded marks.

Answer to any question must start on a new page.

All questions must be answered in English.

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1. (a) What is the difference between a standard microprocessor and a micro-controller system.

(20%)

(b) List and describe four design metrics for an embedded system design process.

(40%)

(c) Describe the differences between an SRAM and DRAM-type memory. Draw the basic memory circuit for each type of memory as an examples.

(40%)

2. (a) Describe what is a 'Wait States' and how it is utilized in an embedded microprocessor system by using a suitable timing diagram.

(30%)

(b) Describe I2C Bus and its importance in port-to-port communication between peripherals.

(30%)

(c) What is a problem of data bus loading? Describe one method to overcome this problem (draw a suitable diagram if applicable).

(40%)

3. (a) Explain the difference between a level sensitive and an edge sensitive interrupt input?

(25%)

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(b) Explain the difference between a maskable and a nonmaskable interrupt input. In what situations is each type appropriate?

(25%)

(c) While as ISR is executing, no other maskable interrupts will be responded to unless the ISR itself makes this response possible. But, when the ISR has completed its execution, the microprocessor will again respond to maskable interrupts. Explain the mechanism that makes this possible and how the ISR itself can make it possible for maskable interrupts to be responded to during its execution.

(50%)

4. The four EPROMs in Figure 1 are set up in consecutive memory locations between 0 to 16K and are individually enabled by the 74LS138 address decoder. The 4K x 8 EPROMs each require 12 address lines for internal memory selection, leaving the four HIGH-order address lines (A_{12} to A_{15}) free for chip selection by the 74LS138.

(a) When testing the EPROM memory system in Figure 1, the microprocessor reads valid data from all EPROMs except the second EPROM. What are two probable causes?

(35%)

(b) Determine the address range for each EPROM and which EPROM address are accessed when the microprocessor of Figure 1 issues a Read command for the following hex addresses:

(i) READ 0007H
(ii) READ 26C4H
(iii) READ 3FFFH
(iv) READ 5007H (15%)

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(c) Based on Figure 1, design and sketch an address decoding scheme for the 64KB of memory system. Briefly describe how your memory system can be done.

(50%)

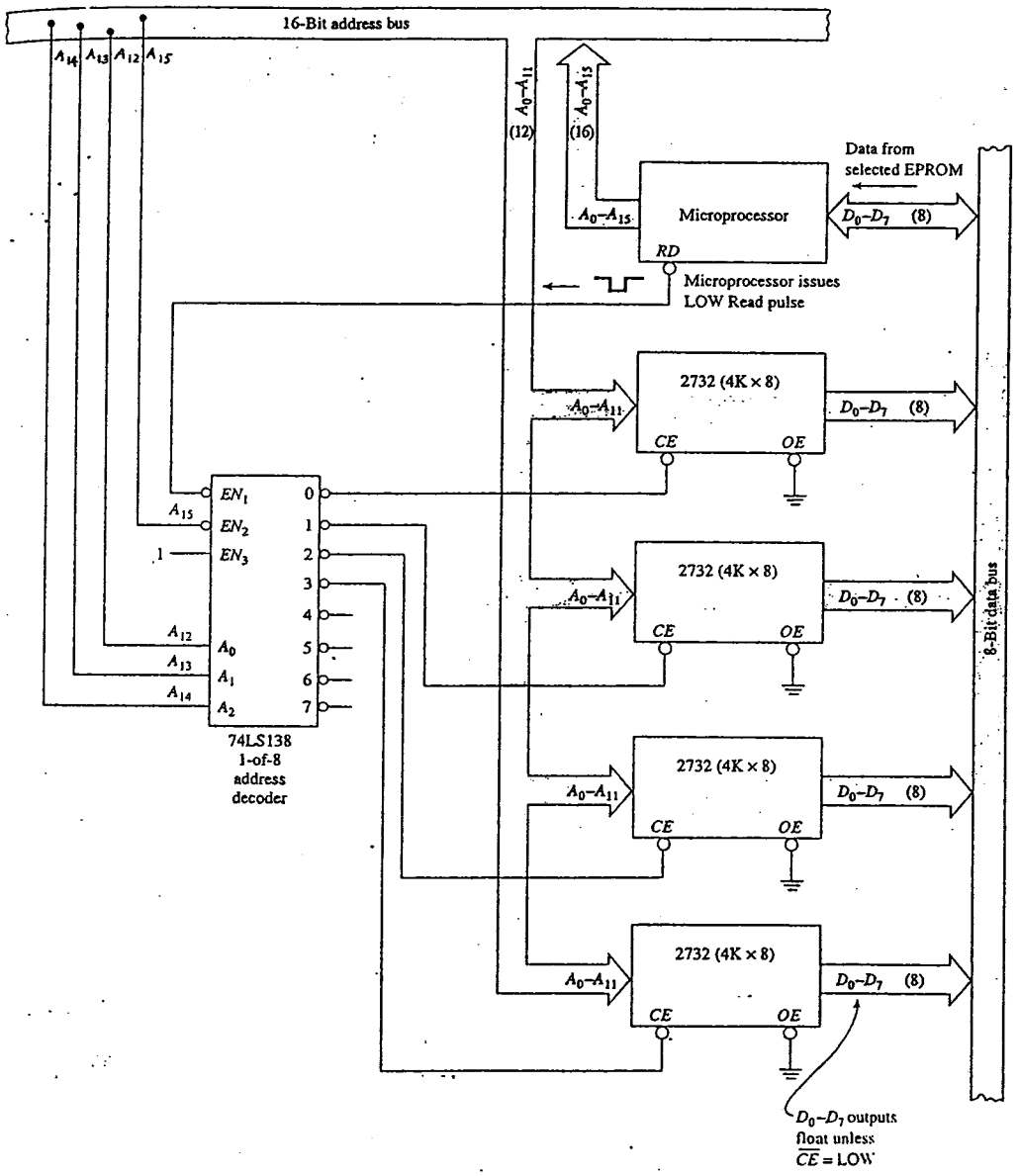

Figure 1

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5. In a multiprocessor system, the need to transfer and send data is crucial for system processor intercommunication. There are various techniques/methods can be used. One of the methods is using register.

(a) Draw and explain the operations of using register. (50%)

(b) Another alternative is to add Flip-Flop for Question 5(a). Explain the operations and the advantages or disadvantages. (50%)

6. (a) Explain three (3) ways on how to describe software design. (50%)

(b) Design any system and draw the corresponding State Diagram. (50%)

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