UNIVERSITI SAINS MALAYSIA

First Semester Examination
Academic Session 2004/2005

October 2004

EEE 510 – ANALOG INTEGRATED CIRCUIT DESIGN

Time : 3 Hours

INSTRUCTION TO CANDIDATE:-

Please ensure that this examination paper contains **<u>TEN</u> (10)** printed pages including **Appendices (15 pages)** and **<u>SIX</u> (6)** questions before answering.

Answer **<u>FIVE</u> (5)** questions.

Distribution of marks for each question is given accordingly.

All questions must be answered in English.

1.

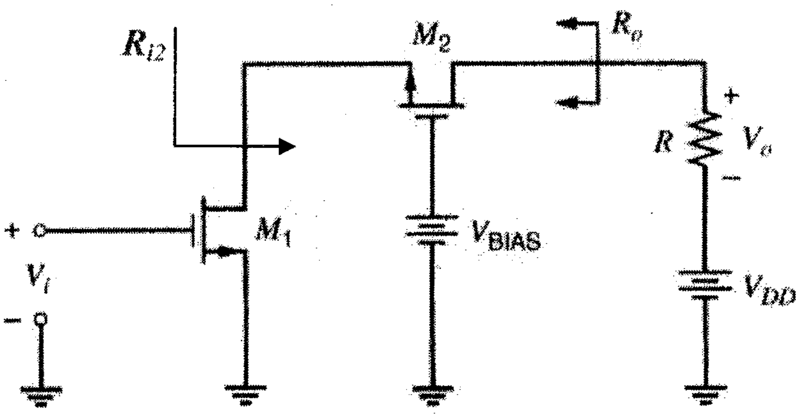


Figure 1

Figure 1 : Above shows a cascode amplifier of CS-CG configuration.

(a) Find the small signal equivalent circuit for the above cascode amplifier and derive its components for cascode transconductance G_m, output resistance R_o, resistance looking in the source of transistor M_2 R_{i2}, and output voltage gain A_v [Refer Appendix B]

(50%)

(b) Explain briefly the condition needed for considering

$$G_m \approx g_{m1} \text{ and } R_o \approx (g_{m2}+g_{mb2})r_{01}r_{02}$$

(10%)

(c) Explain briefly the condition needed for considering

$$R_{i2} \approx \frac{1}{g_{m2}+g_{mb2}} + \frac{R}{(g_{m2}+g_{mb2})\, r_{o2}}$$

(10%)

(d) Calculate the value for G_m and R_{i2} of the circuit and compare both results with the approximation made in (b) and (c) when both transistors operate in the active region with $g_m = 1\text{mA/V}$, $\chi = g_{mb}/g_m = 0.5$, and $r_o = 20\text{K}\Omega$. [Refer Appendix B]

(30%)

2.

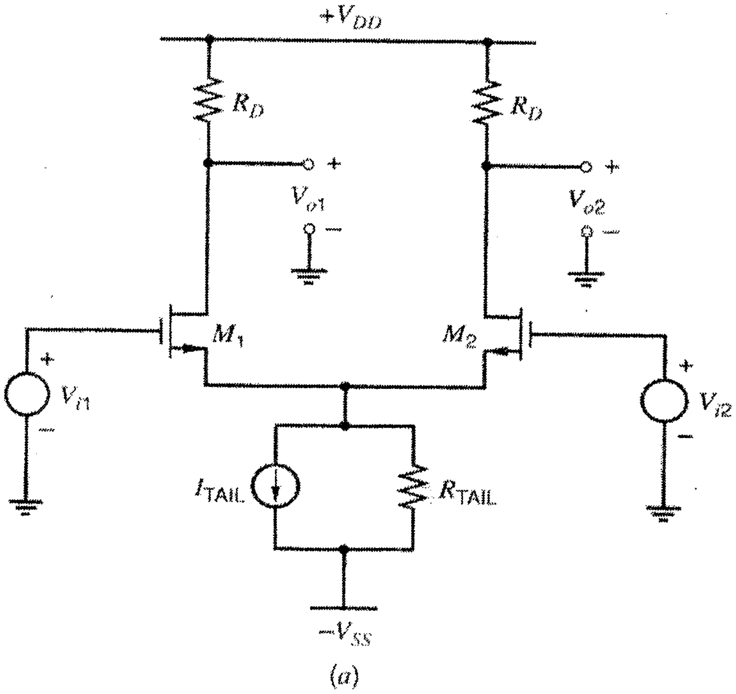


Figure 2: MOSFET source-couple pair

(a) Given a source-couple identical M_1 and M_2 differential pair above, derive specific equations for each V_{id} and V_{od} by using KVL at the input loop and KCL at the source of M_1 and M_2 that conclude,

$$V_{id} = \frac{\sqrt{I_{d1}} - \sqrt{I_{d2}}}{\sqrt{\frac{k'}{2}\frac{W}{L}}}$$

$$V_{od} = -(\Delta I_d)\, R_D$$

Where,

$$I_{d1} = \frac{I_{TAIL}}{2} + \frac{k'}{4}\frac{W}{L} V_{id}\sqrt{\frac{4I_{TAIL}}{k'(W/L)} - V_{id}^2}$$

$$\Delta I_d = I_{d1} - I_{d2} = \frac{k'}{2}\frac{W}{L} V_{id}\sqrt{\frac{4I_{TAIL}}{k'(W/L)} - V_{id}^2}$$

(40%)

(b) Explain briefly the switching state (ON and OFF swinging) phenomenon between M_1 and M_2 in relation with the swinging of I_{d1} and I_{d2} for different overdrive voltage biasing as shown in Figure 3.

(30%)

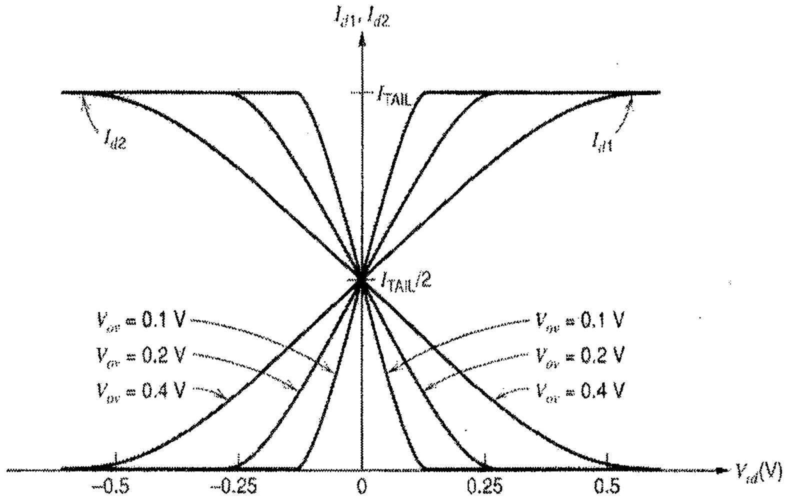
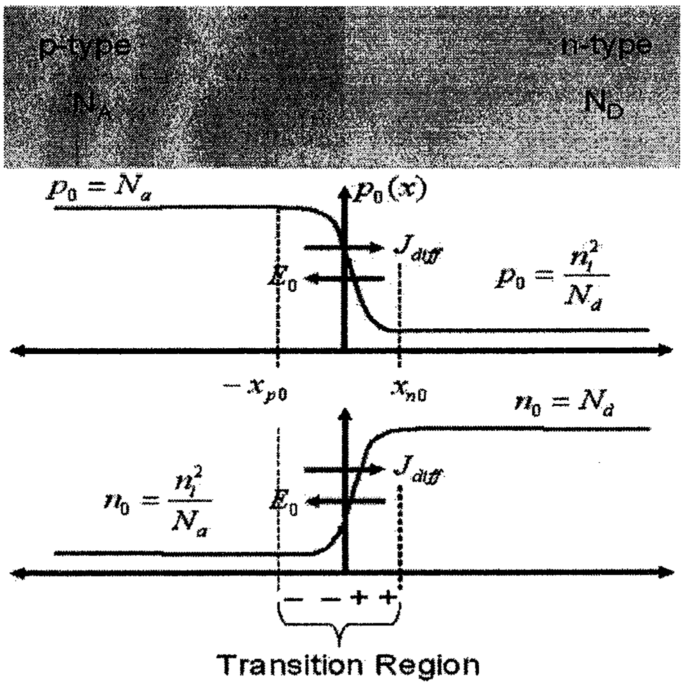


Figure 3

(c) Explain the reason for designing a ***Perfect Symmetry Balanced Differential Amplifier*** by stating its quantitative measures, also explain how does it relate to the actual differential amplifier when A_{dm}/A_{cm}, $A_{dm}/A_{dm\text{-}cm}$, $A_{dm}/A_{cm\text{-}dm}$

(30%)

3. The following Figure 4 illustrates the formation of depletion region for a simple uniformly doped p-n junction at thermal equilibrium.



$$\frac{dE_0}{dx} = -\frac{d^2\phi}{dx^2} = \frac{\rho_0(x)}{\varepsilon_s}$$

$$\rho_0(x) \cong \begin{cases} -qN_a & -x_{po} < x < 0 \\ +qN_d & 0 < x < x_{no} \end{cases}$$

Figure 4

(a) Solve the equations for depletion region width (***W*** = W_1 + W_2 = X_{no} + X_{po}), built in potential barrier (V_{bi}), and the electric field (E_o) for a uniformly doped p-n junction at thermal equilibrium.

(30%)

(b) Sketch out the plots for each E_o, V_{bi}, and ρ_o versus depletion region width by stating specific parameters and functions involved.

(10%)

[Refer Appendix B]

(c) To design a pn junction to meet maximum electric field and voltage specifications, one must consider a silicon pn junction at 27°C with a p-type doping concentration of $N_a=10^{18}$cm-3.

Determine the n-type doping concentration such that the maximum electric field is $|E_{max}| = 3X10^5$ V/cm at a reverse-bias voltage $V_R = 25$V.

(30%)

(d) What can you conclude of $|E_{max}|$ by having smaller value of N_d ?

(10%)

(e) Calculate the shot noise current power and shot noise current rms for a p-n junction of 1mA in a bandwidth of 1MHz.

(20%)

4. (a) Derive the complete small-signal model for an NMOS transistor with I_D=100µA, V_{SB}=1V, V_{DS}=2V. Device parameters are φ_f = 0.3V, W=10µm, L=1µm, γ = 0.5V$^{1/2}$, k'= 200 µA/V^2, λ = 0.02 V^{-1}, t_{ox} = 100 angstrom, ψ_o= 0.6V, C_{sbo} = C_{dbo}= 10 fF. Overlap capacitance from gate to source and gate to drain is 1 fF. Assume C_{gb}=5fF and

$V_{ov} = V_{GS} - V_t = \sqrt{\dfrac{2I_D}{k'(W/L)}}$	$g_m = \sqrt{2k'\dfrac{W}{L}I_D}$	$g_{mb} = \gamma\sqrt{\dfrac{k'(W/L)I_D}{2(2\phi_f + V_{SB})}}$

(40%)

[Refer Appendix B]

(b) Calculate the value for transition frequency of the short circuit current unity gain frequency, f_T

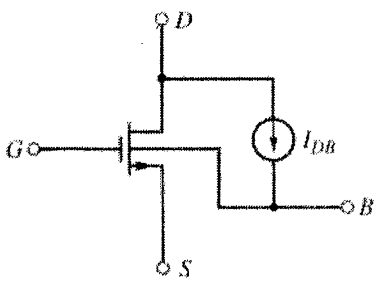
(10%)

(c) Calculate the overdrive and the transition frequency for NMOS transistor operates at room temperature (T = 27°C) with I_D =1μA, I_t = 0.1μA, $V_{DS} >> V_T$. Device parameters are W=10μm, L=1μm, n = 1.5, k'= 200 μA/V^2, t_{ox} = 100 angstrom. Assume the transistor is operating in strong inversion.

(30%)

(d) Calculate $r_{db} = 1/g_{db}$ for V_{DS}=2V and 4 V, and then compare with the device r_o. Assume I_d=100μA, λ = 0.05 V^{-1}, $V_{DS\,(active)}$ = 0.3V, K_1 = 5V^{-1}, and K_2 = 30V. The drain to bulk substrate relationships are given by the following equations (Refer to Figure 5).

(20%)



$$I_{DB} = K_1(V_{DS} - V_{DS(act)})I_D \exp\left(-\frac{K_2}{V_{DS} - V_{DS(act)}}\right)$$

$$g_{db} = \frac{\partial I_{DB}}{\partial V_D} = \frac{I_{DB}}{V_{DS} - V_{DS(act)}}\left(\frac{K_2}{V_{DS} - V_{DS(act)}} + 1\right) \approx \frac{K_2 I_{DB}}{(V_{DS} - V_{DS(act)})^2}$$

Figure 5: Representation of impact ionization in an MOSFET by drain-substrate current generator

(b) The ac schematic of a shunt-shunt feed-back amplifier is shown in Figure 7. All transistors have $I_D = 1\, mA, W/L = 100, k' = 60 \mu A/V^2$, and $\lambda = 1/(50\, V)$.

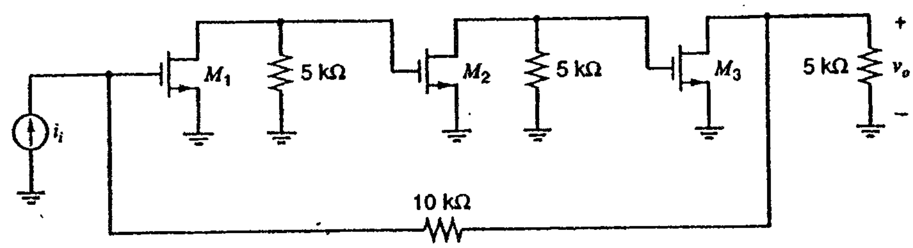


Figure 7 : An ac schematic of a shunt-shunt feedback amplifier

Calculate the overall gain v_o / i_i, the loop transmission, the input impedance, and the output impedance at low frequencies. Use the formulas from two-port analysis (see Appendix C).

(50 %)

6. An amplifier has a low-frequency forward gain of 5000 and its transfer function has three negative real poles with magnitudes 300 kHz, 2 MHz, and 25 MHz.

(a) Calculate the dominant-pole magnitude required to give unity-gain compensation of this amplifier with a 45° phase margin if the original amplifier poles remain fixed. What is the resulting bandwidth of the circuit with the feedback applied?

(50%)

(b) Repeat (a) for compensation in a feedback loop with a forward gain of 20 dB and 45° phase margin.

(50%)

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Frequency Response of Integrated Circuits

7.1 Introduction

The analysis of integrated-circuit behavior in previous chapters was concerned with low-frequency performance, and the effects of parasitic capacitance in transistors were not considered. However, as the frequency of the signal being processed by a circuit increases, the capacitive elements in the circuit eventually become important.

In this chapter, the small-signal behavior of integrated circuits at high frequencies is considered. The frequency response of single-stage amplifiers is treated first, followed by an analysis of multistage amplifiers. Finally, the frequency response of the 741 operational amplifier is considered, and those parts of the circuit that limit its frequency response are identified.

7.2 Single-Stage Amplifiers

The basic topology of the small-signal equivalent circuits of bipolar and MOS single-stage amplifiers are similar. Therefore in the following sections, the frequency-response analysis for each type of single-stage circuit is initially carried out using a general small-signal model that applies to both types of transistors, and the general results are then applied to each type of transistor. The general small-signal transistor model is shown in Fig. 7.1. Table 7.1 lists the parameters of this small-signal model and the corresponding parameters that transform it into a bipolar or MOS model. For example, C_{in} in the general model becomes C_π in the bipolar model and C_{gs} in the MOS model. However, some device-specific small-signal elements are not included in the general model. For example, the g_{mb} generator and capacitors C_{sb} and C_{gb} in the MOS models are not incorporated in the general model. The effect of such device-specific elements will be handled separately in the bipolar and MOS sections.

The common-emitter and common-source stages are analyzed in the sections below on differential amplifiers.

7.2.1 Single-Stage Voltage Amplifiers and the Miller Effect

Single-transistor voltage-amplifier stages are widely used in integrated circuits. Figures 7.2*a* and 7.2*b* show the ac schematics for common-emitter and common-source amplifiers with resistive loads, respectively. Resistance R_S is the source resistance, and R_L is the load resistance. A simple linear model that can be applied to both of these circuits is shown in Fig. 7.2*c*. The elements in the dashed box form the general small-signal transistor model from Fig. 7.1 without r_o. We will assume that the output resistance of the transistor r_o is much larger than R_L. Since these resistors are connected in parallel in the small-signal

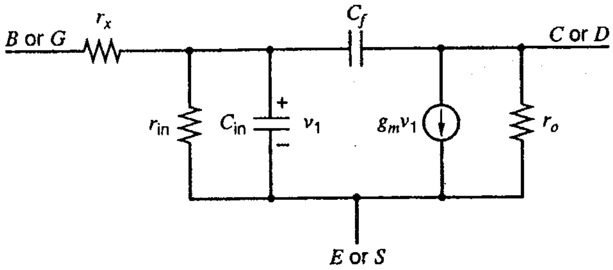


Figure 7.1 A general small-signal transistor model.

circuit, r_o can be neglected. An approximate analysis of this circuit can be made using the *Miller-effect* approximation. This analysis is done by considering the input impedance seen looking across the plane AA in Fig. 7.2*c*. To find this impedance, we calculate the current i_1 produced by the voltage v_1.

$$i_1 = (v_1 - v_o)sC_f \tag{7.1}$$

KCL at the output node gives

$$g_m v_1 + \frac{v_o}{R_L} + (v_o - v_1)sC_f = 0 \tag{7.2}$$

From (7.2), the voltage gain A_v from v_1 to v_o can be expressed as

$$A_v(s) = \frac{v_o}{v_1} = -g_m R_L \left(\frac{1 - s\dfrac{g_m}{C_f}}{1 + sR_L C_f} \right) \tag{7.3}$$

Using $v_o = A_v(s)v_1$ from (7.3) in (7.1) gives

$$i_1 = [1 - A_v(s)]sC_f v_1 \tag{7.4}$$

Equation 7.4 indicates that the admittance seen looking across the plane AA has a value $[1 - A_v(s)]sC_f$. This modification to the admittance sC_f stems from the voltage gain across C_f and is referred to as the Miller effect. Unfortunately, this admittance is complicated, due to the frequency dependence of $A_v(s)$. Replacing the voltage gain $A_v(s)$ in (7.4) with its low-frequency value $A_{v0} = A_v(0)$, (7.4) indicates that a capacitance of value

$$C_M = (1 - A_{v0})C_f \tag{7.5}$$

Table 7.1 Small-Signal Model Elements

General Model	Bipolar Model	MOS Model
r_x	r_b	0
r_{in}	r_π	∞
C_{in}	C_π	C_{gs}
C_f	C_μ	C_{gd}
r_o	r_o	r_o

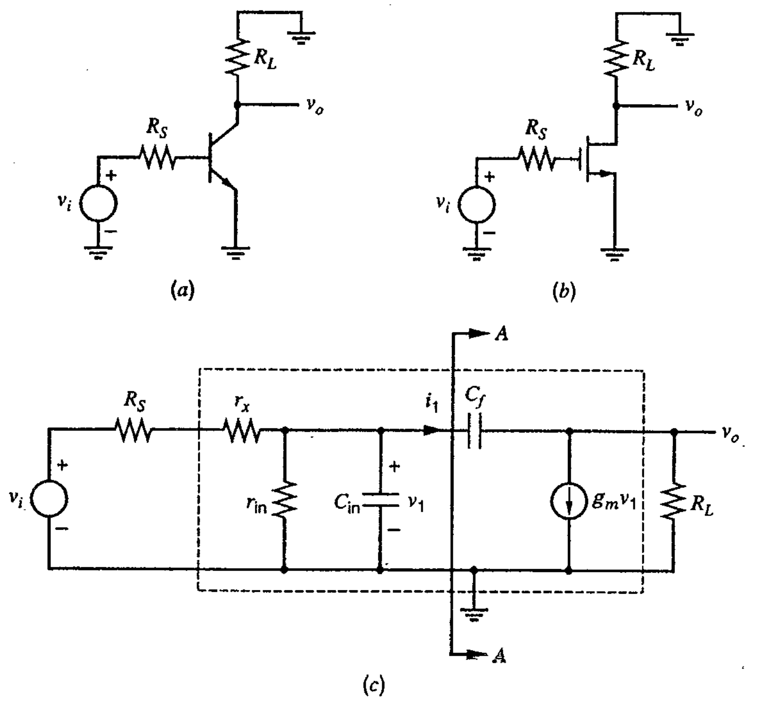


Figure 7.2 (*a*) An ac schematic of a common-emitter amplifier. (*b*) An ac schematic of a common-source amplifier. (*c*) A general model for both amplifiers.

is seen looking across plane AA. The use of the low-frequency voltage gain here is called the *Miller approximation,* and C_M is called the *Miller capacitance.* From (7.3), $A_{v0} = A_v(0) = -g_m R_L$; therefore, (7.5) can be written as

$$C_M = (1 + g_m R_L)C_f \tag{7.6}$$

The Miller capacitance is often much larger than C_f because usually $g_m R_L \gg 1$.

We can now form a new equivalent circuit that is useful for calculating the *forward transmission* and input impedance of the circuit. This is shown in Fig. 7.3 using the Miller-effect approximation. Note that this equivalent circuit is *not* useful for calculating high-frequency reverse transmission or output impedance. From this circuit, we can see that at high frequencies the input impedance will eventually approach r_x.

The physical origin of the Miller capacitance is found in the voltage gain of the circuit. At low frequencies, a small input voltage v_1 produces a large output voltage $v_o = A_{v0}v_1 = -g_m R_L v_1$ of *opposite polarity.* Thus the voltage across C_f in Fig. 7.2*c* is $(1 + g_m R_L)v_1$ and a correspondingly large current i_1 flows in this capacitor. The voltage across C_M

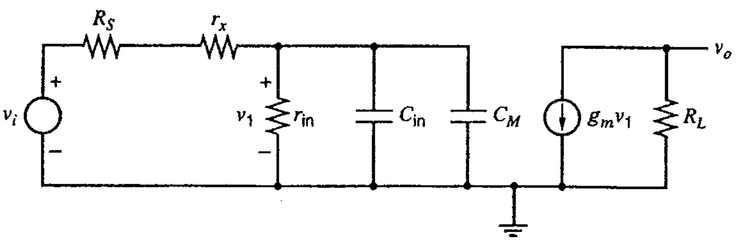


Figure 7.3 Equivalent circuit for Fig. 7.2*c* using the Miller approximation.

in Fig. 7.3 is only v_1, but C_M is larger than C_f by the factor $(1 + g_m R_L)$; therefore, C_M conducts the same current as C_f.

In Fig. 7.3, the Miller capacitance adds directly to C_{in} and thus reduces the bandwidth of the amplifier, which can be seen by calculating the gain of the amplifier as follows:

$$v_1 = \frac{\dfrac{r_{in}}{1 + sr_{in}C_t}}{\dfrac{r_{in}}{1 + sr_{in}C_t} + R_S + r_x} v_i \tag{7.7}$$

$$v_o = -g_m R_L v_1 \tag{7.8}$$

where

$$C_t = C_M + C_{in} \tag{7.9}$$

Substitution of (7.7) in (7.8) gives the gain

$$A(s) = \frac{v_o}{v_i} = -g_m R_L \frac{r_{in}}{R_S + r_x + r_{in}} \frac{1}{1 + sC_t \dfrac{(R_S + r_x)r_{in}}{R_S + r_x + r_{in}}} \tag{7.10a}$$

$$= K \frac{1}{1 - \dfrac{s}{p_1}} \tag{7.10b}$$

where K is the low-frequency voltage gain and p_1 is the pole of the circuit. Comparing (7.10a) and (7.10b) shows that

$$K = -g_m R_L \frac{r_{in}}{R_S + r_x + r_{in}} \tag{7.11a}$$

$$p_1 = -\frac{R_S + r_x + r_{in}}{(R_S + r_x)r_{in}} \cdot \frac{1}{C_t} = -\frac{1}{[(R_S + r_x)\|r_{in}]C_t}$$

$$= -\frac{1}{[(R_S + r_x)\|r_{in}] \cdot [C_{in} + C_f(1 + g_m R_L)]} \tag{7.11b}$$

This analysis indicates that the circuit has a single pole, and setting $s = j\omega$ in (7.10b) shows that the voltage gain is 3 dB below its low-frequency value at a frequency

$$\omega_{-3dB} = |p_1| = \frac{R_S + r_x + r_{in}}{(R_S + r_x)r_{in}} \cdot \frac{1}{C_t} = \frac{1}{[(R_S + r_x)\|r_{in}] \cdot [C_{in} + C_f(1 + g_m R_L)]} \tag{7.12}$$

As C_t, R_L, or R_S increase, the -3-dB frequency of the amplifier is reduced.

The exact gain expression for this circuit can be found by analyzing the equivalent circuit shown in Fig. 7.4. The poles from an exact analysis can be compared to the pole found using the Miller effect. In Fig. 7.4, a Norton equivalent is used at the input where

$$R = (R_S + r_x)\|r_{in} \tag{7.13}$$

$$i_i = \frac{v_i}{R_S + r_x} \tag{7.14}$$

KCL at node X gives

$$i_i = \frac{v_1}{R} + v_1 sC_{in} + (v_1 - v_o)sC_f \tag{7.15}$$

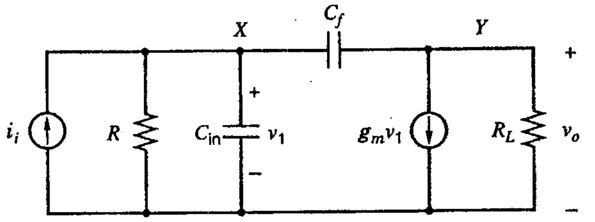


Figure 7.4 Figure 7.2*c* redrawn using a Norton equivalent circuit at the input.

KCL at node Y gives

$$g_m v_1 + \frac{v_o}{R_L} + (v_o - v_1)sC_f = 0 \tag{7.16a}$$

Equation 7.16a can be written as

$$v_1(g_m - sC_f) = -v_o\left(\frac{1}{R_L} + sC_f\right) \tag{7.16b}$$

and thus

$$v_1 = -v_o \frac{\dfrac{1}{R_L} + sC_f}{g_m - sC_f} \tag{7.17}$$

Substitution of (7.17) in (7.15) gives

$$i_i = -\left(\frac{1}{R} + sC_{\text{in}} + sC_f\right)\frac{\dfrac{1}{R_L} + sC_f}{g_m - sC_f}v_o - sC_f v_o$$

and the transfer function can be calculated as

$$\frac{v_o}{i_i} = -\frac{RR_L(g_m - sC_f)}{1 + s(C_f R_L + C_f R + C_{\text{in}} R + g_m R_L R C_f) + s^2 R_L R C_f C_{\text{in}}} \tag{7.18}$$

Substitution of i_i from (7.14) in (7.18) gives

$$\frac{v_o}{v_i} = -\frac{g_m R_L R}{R_S + r_x}\frac{1 - s\dfrac{C_f}{g_m}}{1 + s(C_f R_L + C_f R + C_{\text{in}} R + g_m R_L R C_f) + s^2 R_L R C_f C_{\text{in}}} \tag{7.19}$$

Substitution of R from (7.13) into (7.19) gives, for the low-frequency gain,

$$\left.\frac{v_o}{v_i}\right|_{\omega=0} = -g_m R_L \frac{r_{\text{in}}}{R_S + r_x + r_{\text{in}}} \tag{7.20}$$

as obtained in (7.10).

Equation 7.19 shows that the transfer function v_o/v_i has a positive real zero with magnitude g_m/C_f. This zero stems from the transmission of the signal directly through C_f to the output. The effect of this zero is small except at very high frequencies, and it will be neglected here. However, this positive real zero can be important in the stability analysis of some operational amplifiers, and it will be considered in detail in Chapter 9. The denominator of (7.19) shows that the transfer function has two poles, which are usually real and widely separated in practice. If the poles are at p_1 and p_2, we can write the denominator of (7.19) as

$$D(s) = \left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right) \tag{7.21}$$

and thus

$$D(s) = 1 - s\left(\frac{1}{p_1} + \frac{1}{p_2}\right) + \frac{s^2}{p_1 p_2} \tag{7.22}$$

We now assume that the poles are real and widely separated, and we let the lower frequency pole be p_1 (the dominant pole) and the higher frequency pole be p_2 (the non-dominant pole). Then $|p_2| \gg |p_1|$ and (7.22) becomes

$$D(s) \approx 1 - \frac{s}{p_1} + \frac{s^2}{p_1 p_2} \tag{7.23}$$

If the coefficient of s in (7.23) is compared with that in (7.19), we can identify

$$\begin{aligned} p_1 &= -\frac{1}{C_{\text{in}}R + C_f(R + g_m R_L R + R_L)} \\ &= -\frac{1}{R\left[C_{\text{in}} + C_f\left(1 + g_m R_L + \frac{R_L}{R}\right)\right]} \end{aligned} \tag{7.24}$$

If the value of R from (7.13) is substituted in (7.24), then the dominant pole is

$$\begin{aligned} p_1 &= -\frac{R_S + r_x + r_{\text{in}}}{(R_S + r_x)r_{\text{in}}} \frac{1}{\left[C_{\text{in}} + C_f\left(1 + g_m R_L + \frac{R_L}{R}\right)\right]} \\ &= -\frac{1}{[(R_S + r_x)\|r_{\text{in}}] \cdot \left[C_{\text{in}} + C_f\left(1 + g_m R_L + \frac{R_L}{R}\right)\right]} \end{aligned} \tag{7.25}$$

This value of p_1 is almost identical to that given in (7.11b) by the Miller approximation. The only difference between these equations is in the last term in the denominator of (7.25), R_L/R, and this term is usually small compared to the $(1 + g_m R_L)$ term. This result shows that the Miller-effect calculation is nearly equivalent to calculating the dominant pole of the amplifier and neglecting higher frequency poles. The Miller approximation gives a good estimate of $\omega_{-3\text{dB}}$ in many circuits.

Let us now calculate the nondominant pole by equating the coefficient of s^2 in (7.23) with that in (7.19), giving

$$p_2 = \frac{1}{p_1} \frac{1}{R_L R C_f C_{\text{in}}} \tag{7.26}$$

Substitution of p_1 from (7.24) in (7.26) gives

$$p_2 = -\left(\frac{1}{R_L C_f} + \frac{1}{R C_{\text{in}}} + \frac{1}{R_L C_{\text{in}}} + \frac{g_m}{C_{\text{in}}}\right) \tag{7.27}$$

The results in this section were derived using a general small-signal model. The general model parameters and the corresponding parameters for a bipolar and MOS transistor are listed in Table 7.1. By substituting values from Table 7.1, the general results of this section will be extended to the bipolar common-emitter and MOS common-source amplifiers, which appear in the half-circuits for differential amplifiers in the following sections.

A.1.1 SUMMARY OF ACTIVE-DEVICE PARAMETERS

(a) *npn* Bipolar Transistor Parameters

Quantity	Formula
Large-Signal Forward-Active Operation	
Collector current	$I_c = I_S \exp \dfrac{V_{be}}{V_T}$
Small-Signal Forward-Active Operation	
Transconductance	$g_m = \dfrac{qI_C}{kT} = \dfrac{I_C}{V_T}$
Transconductance-to-current ratio	$\dfrac{g_m}{I_C} = \dfrac{1}{V_T}$
Input resistance	$r_\pi = \dfrac{\beta_0}{g_m}$
Output resistance	$r_o = \dfrac{V_A}{I_C} = \dfrac{1}{\eta g_m}$
Collector-base resistance	$r_\mu = \beta_0 r_o$ to $5\beta_0 r_o$
Base-charging capacitance	$C_b = \tau_F g_m$
Base-emitter capacitance	$C_\pi = C_b + C_{je}$
Emitter-base junction depletion capacitance	$C_{je} \simeq 2C_{je0}$
Collector-base junction capacitance	$C_\mu = \dfrac{C_{\mu 0}}{\left(1 - \dfrac{V_{BC}}{\psi_{0c}}\right)^{n_c}}$

(continued)

Quantity	Formula
Small-Signal Forward-Active Operation	
Collector-substrate junction capacitance	$C_{cs} = \dfrac{C_{cs0}}{\left(1 - \dfrac{V_{SC}}{\psi_{0s}}\right)^{n_s}}$
Transition frequency	$f_T = \dfrac{1}{2\pi} \dfrac{g_m}{C_\pi + C_\mu}$
Effective transit time	$\tau_T = \dfrac{1}{2\pi f_T} = \tau_F + \dfrac{C_{je}}{g_m} + \dfrac{C_\mu}{g_m}$
Maximum gain	$g_m r_o = \dfrac{V_A}{V_T} = \dfrac{1}{\eta}$

(b) *NMOS* Transistor Parameters

Quantity	Formula
Large-Signal Operation	
Drain current (active region)	$I_d = \dfrac{\mu C_{ox}}{2} \dfrac{W}{L} (V_{gs} - V_t)^2$
Drain current (triode region)	$I_d = \dfrac{\mu C_{ox}}{2} \dfrac{W}{L} [2(V_{gs} - V_t)V_{ds} - V_{ds}^2]$
Threshold voltage	$V_t = V_{t0} + \gamma\left[\sqrt{2\phi_f + V_{sb}} - \sqrt{2\phi_f}\right]$
Threshold voltage parameter	$\gamma = \dfrac{1}{C_{ox}} \sqrt{2q\epsilon N_A}$
Oxide capacitance	$C_{ox} = \dfrac{\epsilon_{ox}}{t_{ox}} = 3.45\ \text{fF}/\mu\text{m}^2$ for $t_{ox} = 100$ Å
Small-Signal Operation (Active Region)	
Top-gate transconductance	$g_m = \mu C_{ox} \dfrac{W}{L} (V_{GS} - V_t) = \sqrt{2 I_D \mu C_{ox} \dfrac{W}{L}}$
Transconductance-to-current ratio	$\dfrac{g_m}{I_D} = \dfrac{2}{V_{GS} - V_t}$
Body-effect transconductance	$g_{mb} = \dfrac{\gamma}{2\sqrt{2\phi_f + V_{SB}}} g_m = \chi g_m$
Channel-length modulation parameter	$\lambda = \dfrac{1}{V_A} = \dfrac{1}{L_{\text{eff}}} \dfrac{dX_d}{dV_{DS}}$
Output resistance	$r_o = \dfrac{1}{\lambda I_D} = \dfrac{L_{\text{eff}}}{I_D} \left(\dfrac{dX_d}{dV_{DS}}\right)^{-1}$
Effective channel length	$L_{\text{eff}} = L_{\text{drwn}} - 2L_d - X_d$
Maximum gain	$g_m r_o = \dfrac{1}{\lambda} \dfrac{2}{V_{GS} - V_t} = \dfrac{2V_A}{V_{GS} - V_t}$
Source-body depletion capacitance	$C_{sb} = \dfrac{C_{sb0}}{\left(1 + \dfrac{V_{SB}}{\psi_0}\right)^{0.5}}$

(*continued*)

Quantity	Formula
Small-Signal Operation (Active Region)	
Drain-body depletion capacitance	$C_{db} = \dfrac{C_{db0}}{\left(1 + \dfrac{V_{DB}}{\psi_0}\right)^{0.5}}$
Gate-source capacitance	$C_{gs} = \dfrac{2}{3} W L C_{ox}$
Transition frequency	$f_T = \dfrac{g_m}{2\pi(C_{gs} + C_{gd} + C_{gb})}$

Table B.2 | Conversion factors

	Prefixes		
1 Å (angstrom) $= 10^{-8}$ cm $= 10^{-10}$ m	10^{-15}	femto-	= f
1 μm (micron) $= 10^{-4}$ cm	10^{-12}	pico-	= p
1 mil $= 10^{-3}$ in. $= 25.4$ μm	10^{-9}	nano-	= n
2.54 cm = 1 in.	10^{-6}	micro-	= μ
1 eV $= 1.6 \times 10^{-19}$ J	10^{-3}	milli-	= m
1 J $= 10^{7}$ erg	10^{+3}	kilo-	= k
	10^{+6}	mega-	= M
	10^{+9}	giga-	= G
	10^{+12}	tera	= T

Table B.3 | Physical constants

Avogadro's number	$N_A = 6.02 \times 10^{+23}$ atoms per gram molecular weight
Boltzmann's constant	$k = 1.38 \times 10^{-23}$ J/K $= 8.62 \times 10^{-5}$ eV/K
Electronic charge (magnitude)	$e = 1.60 \times 10^{-19}$ C
Free electron rest mass	$m_0 = 9.11 \times 10^{-31}$ kg
Permeability of free space	$\mu_0 = 4\pi \times 10^{-7}$ H/m
Permittivity of free space	$\epsilon_0 = 8.85 \times 10^{-14}$ F/cm $= 8.85 \times 10^{-12}$ F/m
Planck's constant	$h = 6.625 \times 10^{-34}$ J-s $= 4.135 \times 10^{-15}$ eV-s
	$\dfrac{h}{2\pi} = \hbar = 1.054 \times 10^{-34}$ J-s
Proton rest mass	$M = 1.67 \times 10^{-27}$ kg
Speed of light in vacuum	$c = 2.998 \times 10^{10}$ cm/s
Thermal voltage ($T = 300$ K)	$V_t = \dfrac{kT}{e} = 0.0259$ volt
	$kT = 0.0259$ eV

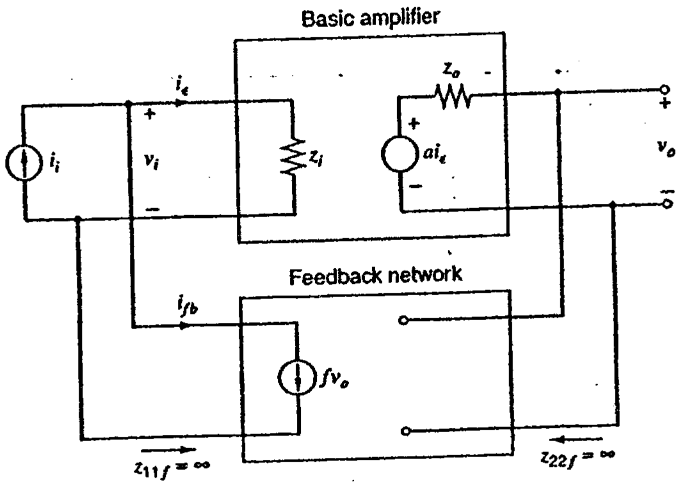


Figure 8.9 Shunt-shunt feedback configuration.

8.5 Practical Configurations and the Effect of Loading

In practical feedback amplifiers, the feedback network causes loading at the input and output of the basic amplifier, and the division into basic amplifier and feedback network is not as obvious as the above treatment implies. In such cases, the circuit can always be analyzed by writing circuit equations for the whole amplifier and solving for the transfer function and terminal impedances. However, this procedure becomes very tedious and difficult in most practical cases, and the equations so complex that one loses sight of the important aspects of circuit performance. Thus it is profitable to identify a basic amplifier and feedback network in such cases and then to use the ideal feedback equations derived above. In general it will be necessary to include the loading effect of the feedback network on the basic amplifier, and methods of including this loading in the calculations are now considered. The *method* will be developed through the use of two-port representations of the circuits involved, although this method of representation is not necessary for practical calculations, as we will see.

8.5.1 Shunt-Shunt Feedback

Consider the shunt-shunt feedback amplifier of Fig. 8.9. The effect of nonideal networks may be included as shown in Fig. 8.13*a*, where finite input and output admittances are assumed in both forward and feedback paths, as well as reverse transmission in each. Finite source and load admittances y_S and y_L are assumed. The most convenient two-port

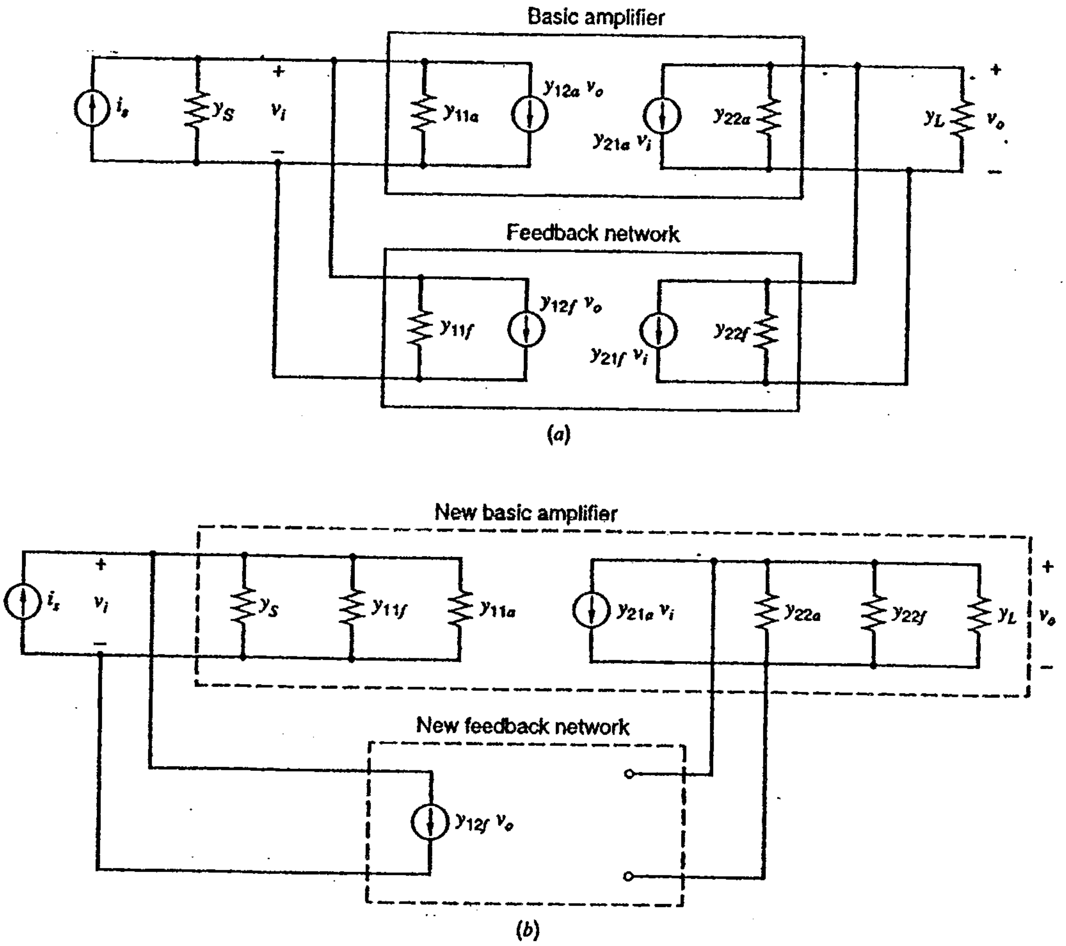


Figure 8.13 (*a*) Shunt-shunt feedback configuration using the *y*-parameter representation. (*b*) Circuit of (*a*) redrawn with generators $y_{21f}v_i$ and $y_{12a}v_o$ omitted.

representation in this case is the short-circuit admittance parameters or *y* parameters,[1] as used in Fig. 8.13*a*. The reason for this is that the basic amplifier and the feedback network are connected in parallel at input and output, and thus have identical *voltages* at their terminals. The *y* parameters specify the response of a network by expressing the terminal currents in terms of the terminal voltages, and this results in very simple calculations when two networks have identical terminal voltages. This will be evident in the circuit calculations to follow. The *y*-parameter representation is illustrated in Fig. 8.14.

From Fig. 8.13*a*, at the input

$$i_s = (y_S + y_{11a} + y_{11f})v_i + (y_{12a} + y_{12f})v_o \tag{8.46}$$

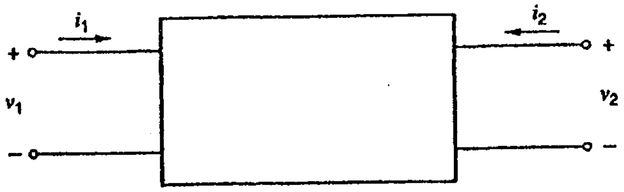
Summation of currents at the output gives

$$0 = (y_{21a} + y_{21f})v_i + (y_L + y_{22a} + y_{22f})v_o \tag{8.47}$$

It is useful to define

$$y_i = y_S + y_{11a} + y_{11f} \tag{8.48}$$

$$y_o = y_L + y_{22a} + y_{22f} \tag{8.49}$$



$$i_1 = y_{11} v_1 + y_{12} v_2$$
$$i_2 = y_{21} v_1 + y_{22} v_2$$
$$y_{11} = \frac{i_1}{v_1}\bigg|_{v_2 = 0} \qquad y_{12} = \frac{i_1}{v_2}\bigg|_{v_1 = 0}$$
$$y_{21} = \frac{i_2}{v_1}\bigg|_{v_2 = 0} \qquad y_{22} = \frac{i_2}{v_2}\bigg|_{v_1 = 0}$$

Figure 8.14 The y-parameter representation of a two-port.

Solving (8.46) and (8.47) by using (8.48) and (8.49) gives

$$\frac{v_o}{i_s} = \frac{-(y_{21a} + y_{21f})}{y_i y_o - (y_{21a} + y_{21f})(y_{12a} + y_{12f})} \tag{8.50}$$

The equation can be put in the form of the ideal feedback equation of (8.35) by dividing by $y_i y_o$ to give

$\hookrightarrow \frac{v_o}{i_1} = \frac{a}{1+af} = A$

$$\frac{v_o}{i_s} = \frac{\dfrac{-(y_{21a} + y_{21f})}{y_i y_o}}{1 + \dfrac{-(y_{21a} + y_{21f})}{y_i y_o}(y_{12a} + y_{12f})} \tag{8.51}$$

Comparing (8.51) with (8.35) gives

$$a = -\frac{y_{21a} + y_{21f}}{y_i y_o} \tag{8.52}$$

$$f = y_{12a} + y_{12f} \tag{8.53}$$

At this point, a number of approximations can be made that greatly simplify the calculations. First, we assume that the signal transmitted by the basic amplifier is much greater than the signal fed forward by the feedback network. Since the former has gain (usually large) while the latter has loss, this is almost invariably a valid assumption. This means that

$$|y_{21a}| \gg |y_{21f}| \tag{8.54}$$

Second, we assume that the signal fed back by the feedback network is much greater than the signal fed back through the basic amplifier. Since most active devices have very small reverse transmission, the basic amplifier has a similar characteristic, and this assumption is almost invariably quite accurate. This assumption means that

$$|y_{12a}| \ll |y_{12f}| \tag{8.55}$$

Using (8.54) and (8.55) in (8.51) gives

$$\frac{v_o}{i_s} = A \simeq \frac{\dfrac{-y_{21a}}{y_i y_o}}{1 + \left(\dfrac{-y_{21a}}{y_i y_o}\right) y_{12f}} \tag{8.56}$$

Comparing (8.56) with (8.35) gives

$$a = -\frac{y_{21a}}{y_i y_o} \tag{8.57}$$

$$f = y_{12f} \tag{8.58}$$

A circuit representation of (8.57) and (8.58) can be found as follows. Equations 8.54 and 8.55 mean that in Fig. 8.13*a* the feedback generator of the basic amplifier and the forward-transmission generator of the feedback network may be neglected. If this is done the circuit may be redrawn as in Fig. 8.13*b*, where the terminal admittances y_{11f} and y_{22f} of the feedback network have been absorbed into the basic amplifier, together with source and load impedances y_S and y_L. The new basic amplifier thus *includes the loading effect* of the original feedback network, and the new feedback network is an ideal one as used in Fig. 8.9. If the transfer function of the basic amplifier of Fig. 8.13*b* is calculated (by first removing the feedback network), the result given in (8.57) is obtained. Similarly, the transfer function of the feedback network of Fig. 8.13*b* is given by (8.58). Thus Fig. 8.13*b* is a *circuit representation* of (8.57) and (8.58).

Since Fig. 8.13*b* has a direct correspondence with Fig. 8.9, all the results derived in Section 8.4.2 for Fig. 8.9 can now be used. The loading effect of the feedback network on the basic amplifier is now included by simply shunting input and output with y_{11f} and y_{22f}, respectively. As shown in Fig. 8.14, these terminal admittances of the feedback network are calculated with the other port of the network short-circuited. In practice, loading term y_{11f} is simply obtained by shorting the output node of the amplifier and calculating the feedback circuit input admittance. Similarly, term y_{22f} is calculated by shorting the input node in the amplifier and calculating the feedback circuit output admittance. The feedback transfer function f given by (8.58) is the short-circuit reverse transfer admittance of the feedback network and is defined in Fig. 8.14. This is readily calculated in practice and is often obtained by inspection. Note that the use of y parameters in further calculations is *not* necessary. Once the circuit of Fig. 8.13*b* is established, any convenient network analysis method may be used to calculate gain a of the basic amplifier. We have simply used the two-port representation as a general means of illustrating how loading effects may be included in the calculations.

For example, consider the common shunt-shunt feedback circuit using an op amp as shown in Fig. 8.15*a*. The equivalent circuit is shown in Fig. 8.15*b* and is redrawn in 8.15*c* to allow for loading of the feedback network on the basic amplifier. The y parameters of the feedback network can be found from Fig. 8.15*d*.

$$y_{11f} = \left.\frac{i_1}{v_1}\right|_{v_2=0} = \frac{1}{R_F} \tag{8.59}$$

$$y_{22f} = \left.\frac{i_2}{v_2}\right|_{v_1=0} = \frac{1}{R_F} \tag{8.60}$$

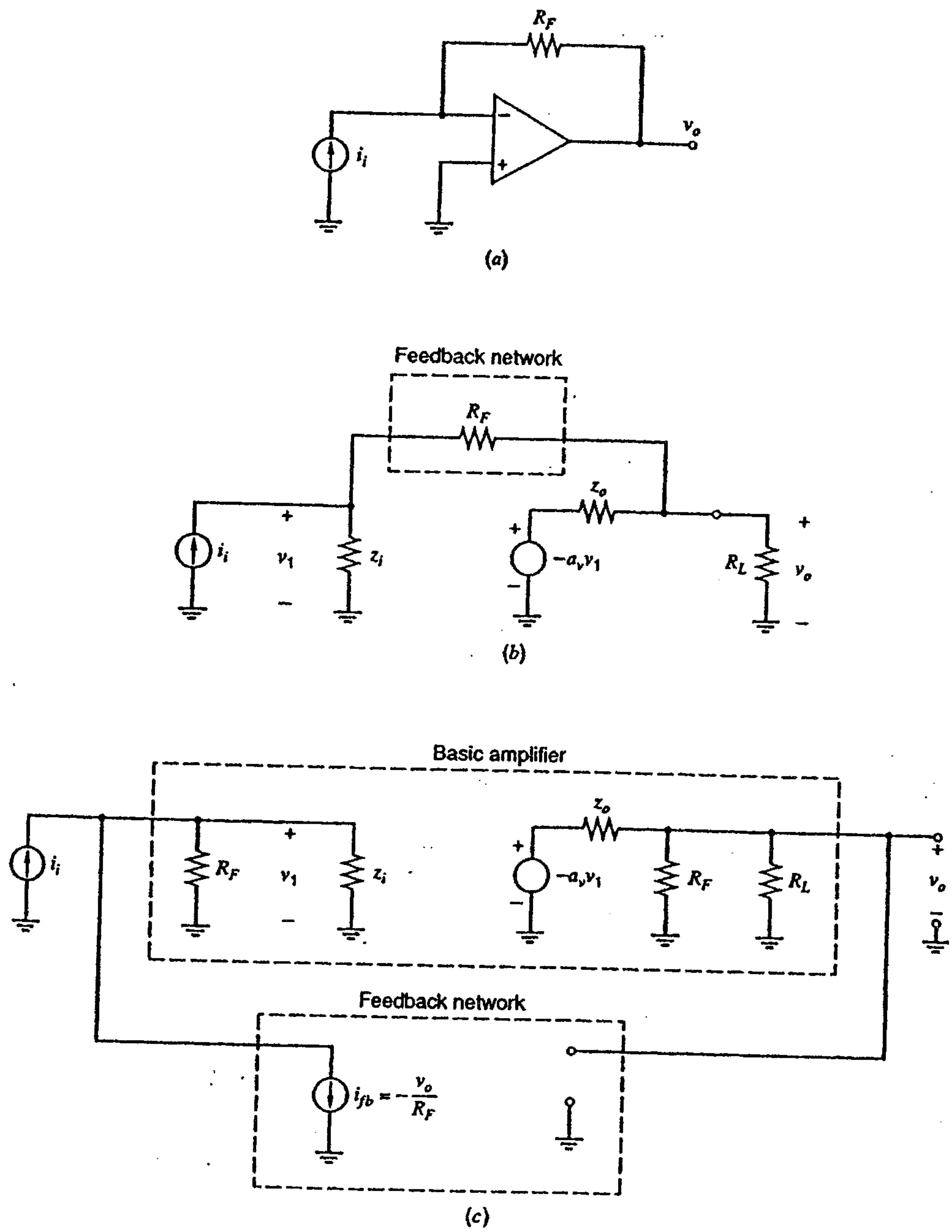
$$y_{12f} = \left.\frac{i_1}{v_2}\right|_{v_1=0} = -\frac{1}{R_F} = f \tag{8.61}$$

Using (8.54), we neglect y_{21f}.

The basic-amplifier gain a can be calculated from Fig. 8.15*c* by putting $i_{fb} = 0$ to give

$$v_1 = \frac{z_i R_F}{z_i + R_F} i_i \tag{8.62}$$

$$v_o = -\frac{R}{R + z_o} a_v v_1 \tag{8.63}$$



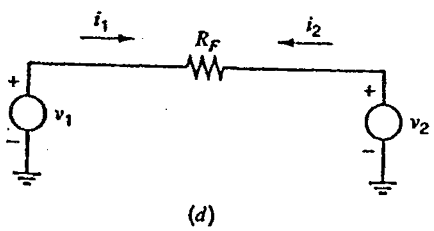


Figure 8.15 (*a*) Shunt-shunt feedback circuit using an op amp as the gain element. (*b*) Equivalent circuit of (*a*). (*c*) Division of the circuit in (*b*) into forward and feedback paths. (*d*) Circuit for the calculation of the *y* parameters of the feedback network of the circuit in (*b*).

where

$$R = R_F \| R_L \tag{8.64}$$

Substituting (8.62) in (8.63) gives

$$\frac{v_o}{i_i} = a = -\frac{R}{R + z_o} a_v \frac{z_i R_F}{z_i + R_F} \tag{8.65}$$

Using the formulas derived in Section 8.4.2 we can now calculate all parameters of the feedback circuit. The input and output impedances of the basic amplifier now *include* the effect of feedback loading, and it is *these impedances* that are divided by $(1 + T)$ as described in Section 8.4.2. Thus the input impedance of the basic amplifier of Fig. 8.15*c* is

$$z_{ia} = R_F \| z_i = \frac{R_F z_i}{R_F + z_i} \tag{8.66}$$

When feedback is applied, the input impedance is

$$Z_i = \frac{z_{ia}}{1 + T} \tag{8.67}$$

Similarly for the output impedance of the basic amplifier

$$z_{oa} = z_o \| R_F \| R_L \tag{8.68}$$

When feedback is applied, this becomes

$$Z_o = \frac{z_o \| R_F \| R_L}{1 + T} \tag{8.69}$$

Note that these calculations can be made using the circuit of Fig. 8.15*c* *without* further need of two-port y parameters.

Since the loop gain T is of considerable interest, this is now calculated using (8.61) and (8.65):

$$T = af = \frac{R_F R_L}{R_F R_L + z_o R_F + z_o R_L} a_v \frac{z_i}{z_i + R_F} \tag{8.70}$$