
UNIVERSITI SAINS MALAYSIA

Peperiksaan Semester Pertama
Sidang Akademik 2004/2005

Oktober 2004

EEE 320 – MIKROPEMROSES II

Masa : 2 jam

ARAHAN KEPADA CALON:

Sila pastikan bahawa kertas peperiksaan ini mengandungi **LIMA (5)** muka surat berserta Lampiran (6 mukasurat) bercetak dan **EMPAT (4)** soalan sebelum anda memulakan peperiksaan ini.

Jawab **TIGA (3)** soalan.

Agihan markah bagi soalan diberikan disudut sebelah kanan soalan berkenaan.

Jawab semua soalan di dalam Bahasa Malaysia.

1. (a) Nyatakan keutamaan sampukan dalam sistem berasaskan 8051.
State the interrupt priority in 8051- based system.
- (10%)
- (b) Bagaimana hendak mengubah keutamaan sampukan dalam 8051?
Terangkan bersama contoh dan pendaftar yang perlu digunakan.
How to change the interrupt priority in 8051 system? Give an example and register that must be used.
- (10%)
- (c) Dapatkan nilai TH dan TL (pendaftar pemasa) untuk menghasilkan satu gelombang segiempat yang berkala $200\mu\text{s}$ sekiranya frekuensi berikut digunakan dalam sistem berasaskan 8051.
Find the value of TH and TL (timer register) to produce one square wave of $200\mu\text{s}$ with the following frequencies in 8051 based system:
- (i) 11.059MHz
(ii) 5MHz
- (10%)
- (d) Anda dikehendaki merekabentuk satu sistem berasaskan 8051 yang dapat membaca data daripada satu pengesan analog setiap 1 milisaat dan menghantar data tersebut kepada PC. Cadangan mestilah mengandungi gambarajah dan aturcara.
You are required to design one system using microcontroller to read data from one analog sensor for every 1 millisecond and send the data to PC. The proposal should have block diagrams and software.
- (70%)

2. Anda dikehendaki merekabentuk litar pengekod pilihan cip menggunakan 74LS138 untuk mengkod julat alamat berikut:

You are required to design a chip select decoder circuit using 74LS138 to decode the following address ranges:

ROM 1	F000 – FFFF
ROM 2	E000 – EFFF
RAM 1	0000 – 1FFF
RAM 2	2000 – 3FFF
PIA 1	8000 – 8003
UART 1	A000 – A007

- (a) Tunjukkan jadual alamat bagi julat alamat untuk setiap peranti yang akan didekodkan sebagaimana dinyatakan di atas.

Show an address table of the address range for each device to be decoded as mentioned above.

(20%)

- (b) Berdasarkan kepada jadual tersebut, tentukan alamat yang manakah diperlukan untuk memilih setiap peranti di atas. Terangkan.

Based on at the table, determine which address lines are required to select any one of the six devices. Explain.

(20%)

- (c) Daripada (a) dan (b), lukiskan gambarajah litar.
From (a) and (b), draw the schematic circuit.

(60%)

...4/-

3. (a) Untuk memperolehi satu struktur asas bersama, sistem terbenam juga berkongsi satu kitar pembangunan bersama. Apakah itu kitar pembangunan? Terangkan.

In addition to have a common fundamental structure, embedded systems also share a common development cycle. What is development cycle? Explain.

(40%)

- (b) Kebanyakan keadaan memerlukan pengumpulan data bagi sesuatu tempoh dengan jangka masa yang berpanjangan. Contohnya adalah keadaan persekitaran pada tapak kawalan, keadaan persekitaran di dalam pejabat dan rumah atau keadaan yang lain di mana sampel bagi tempoh yang panjang diperlukan. Untuk tujuan ini, anda dikehendaki merekabentuk satu sistem pelbagai tujuan untuk mengumpul data analog bagi tempoh masa tertentu. Sistem ini boleh digunakan untuk pelbagai kerja merekod dengan menambahkan antaramuka analog yang sesuai. Rekabentuk anda seharusnya mengandungi satu gambarajah blok sistem, konsep operasi dan satu carta alir perisian untuk keseluruhan sistem. Anda boleh membuat sebarang andaian untuk rekabentuk tersebut.

Many situations require the collection of data over intervals covering an extended period of time. Examples are environmental conditions at control sites, environmental conditions in an office or home, or other situations in which samples over a long interval are required. For this aim, you are required to design a multipurpose system to gather analog data over a period of time. This system can be adapted to a variety of recording tasks by addition of suitable analog interfaces. Your design should contains a block diagram of the system, operational concept and a software flow chart for the overall system. You can make any assumptions for this design.

(60%)

4. (a) Terangkan istilah-istilah berikut:

Explain the following terms:

- (i) EMC – Electromagnetic Compatibility
- (ii) EMI – Electromagnetic Interference
- (iii) ESD – Electrostatic Discharge

(20%)

- (b) Terangkan langkah-langkah yang diperlukan untuk mengekalkan EMC.
Explain the basic checklist to be compliant with EMC.

(40%)

- (c) Bincangkan tentang persekitaran hingar secara elektrik dan kaedah-kaedah pencegahan untuk mengurangkannya.

Discuss about the electrically noisy environments and the preventive methods that might help to minimize the noise.

(40%)



MCS[®]-51 INSTRUCTION SET

Table 10. 8051 Instruction Set Summary

Interrupt Response Time: Refer to Hardware Description Chapter.					
Instructions that Affect Flag Settings⁽¹⁾					
Instruction	Flag			Instruction	Flag
	C	OV	AC		C OV AC
ADD	X	X	X	CLR C	O
ADDC	X	X	X	CPL C	X
SUBB	X	X	X	ANL C,bit	X
MUL	O	X		ANL C,/bit	X
DIV	O	X		ORL C,bit	X
DA	X			ORL C,bit	X
RRC	X			MOV C,bit	X
RLC	X			CJNE	X
SETB C	1				
(1)Note that operations on SFR byte address 208 or bit addresses 209-215 (i.e., the PSW or bits in the PSW) will also affect flag settings.					
Note on instruction set and addressing modes:					
Rn	— Register R7–R0 of the currently selected Register Bank.				
direct	— 8-bit internal data location's address. This could be an Internal Data RAM location (0–127) or a SFR [i.e., I/O port, control register, status register, etc. (128–255)].				
@Ri	— 8-bit internal data RAM location (0–255) addressed indirectly through register R1 or R0.				
#data	— 8-bit constant included in instruction.				
#data 16	— 16-bit constant included in instruction.				
addr 16	— 16-bit destination address. Used by LCALL & LJMP. A branch can be anywhere within the 64K-byte Program Memory address space.				
addr 11	— 11-bit destination address. Used by ACALL & AJMP. The branch will be within the same 2K-byte page of program memory as the first byte of the following instruction.				
rel	— Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is –128 to +127 bytes relative to first byte of the following instruction.				
bit	— Direct Addressed bit in Internal Data RAM or Special Function Register.				

Mnemonic	Description	Byte	Oscillator Period
ARITHMETIC OPERATIONS			
ADD	A,Rn	Add register to Accumulator	1 12
ADD	A,direct	Add direct byte to Accumulator	2 12
ADD	A,@Ri	Add indirect RAM to Accumulator	1 12
ADD	A,#data	Add immediate data to Accumulator	2 12
ADDC	A,Rn	Add register to Accumulator with Carry	1 12
ADDC	A,direct	Add direct byte to Accumulator with Carry	2 12
ADDC	A,@Ri	Add indirect RAM to Accumulator with Carry	1 12
ADDC	A,#data	Add immediate data to Acc with Carry	2 12
SUBB	A,Rn	Subtract Register from Acc with borrow	1 12
SUBB	A,direct	Subtract direct byte from Acc with borrow	2 12
SUBB	A,@Ri	Subtract indirect RAM from ACC with borrow	1 12
SUBB	A,#data	Subtract immediate data from Acc with borrow	2 12
INC	A	Increment Accumulator	1 12
INC	Rn	Increment register	1 12
INC	direct	Increment direct byte	2 12
INC	@Ri	Increment direct RAM	1 12
DEC	A	Decrement Accumulator	1 12
DEC	Rn	Decrement Register	1 12
DEC	direct	Decrement direct byte	2 12
DEC	@Ri	Decrement indirect RAM	1 12

All mnemonics copyrighted ©Intel Corporation 1980

intel.

MCS[®]-51 PROGRAMMER'S GUIDE AND INSTRUCTION SET

Table 10. 8051 Instruction Set Summary (Continued)

Mnemonic	Description	Byte	Oscillator Period	Mnemonic	Description	Byte	Oscillator Period
ARITHMETIC OPERATIONS (Continued)				LOGICAL OPERATIONS (Continued)			
INC DPTR	Increase Data Pointer	1	24	RL A	Rotate Accumulator Left	1	12
MUL AB	Multiply A & B	1	48	RLC A	Rotate Accumulator Left through the Carry	1	12
DIV AB	Divide A by B	1	48	RR A	Rotate Accumulator Right	1	12
DA A	Decimal Adjust Accumulator	1	12	RRC A	Rotate Accumulator Right through the Carry	1	12
LOGICAL OPERATIONS				DATA TRANSFER			
ANL A,Rn	AND Register to Accumulator	1	12	MOV A,Rn	Move register to Accumulator	1	12
ANL A,direct	AND direct byte to Accumulator	2	12	MOV A,direct	Move direct byte to Accumulator	2	12
ANL A,@Ri	AND indirect RAM to Accumulator	1	12	MOV A,@Ri	Move indirect RAM to Accumulator	1	12
ANL A,#data	AND immediate data to Accumulator	2	12	MOV A,#data	Move immediate data to Accumulator	2	12
ANL direct,A	AND Accumulator to direct byte	2	12	MOV Rn,A	Move Accumulator to register	1	12
ANL direct,#data	AND immediate data to direct byte	3	24	MOV Rn,direct	Move direct byte to register	2	24
ORL A,Rn	OR register to Accumulator	1	12	MOV Rn,#data	Move immediate data to register	2	12
ORL A,direct	OR direct byte to Accumulator	2	12	MOV direct,A	Move Accumulator to direct byte	2	12
ORL A,@Ri	OR indirect RAM to Accumulator	1	12	MOV direct,Rn	Move register to direct byte	2	24
ORL A,#data	OR immediate data to Accumulator	2	12	MOV direct,direct	Move direct byte to direct	3	24
ORL direct,A	OR Accumulator to direct byte	2	12	MOV direct,@Ri	Move indirect RAM to direct byte	2	24
ORL direct,#data	OR immediate data to direct byte	3	24	MOV direct,#data	Move immediate data to direct byte	3	24
XRL A,Rn	Exclusive-OR register to Accumulator	1	12	MOV @Ri,A	Move Accumulator to indirect RAM	1	12
XRL A,direct	Exclusive-OR direct byte to Accumulator	2	12				
XRL A,@Ri	Exclusive-OR indirect RAM to Accumulator	1	12				
XRL A,#data	Exclusive-OR immediate data to Accumulator	2	12				
XRL direct,A	Exclusive-OR Accumulator to direct byte	2	12				
XRL direct,#data	Exclusive-OR immediate data to direct byte	3	24				
CLR A	Clear Accumulator	1	12				
CPL A	Complement Accumulator	1	12				

All mnemonics copyrighted ©Intel Corporation 1980

MCS[®]-51 PROGRAMMER'S GUIDE AND INSTRUCTION SET

Table 10. 8051 Instruction Set Summary (Continued)

Mnemonic	Description	Byte	Oscillator Period	Mnemonic	Description	Byte	Oscillator Period
DATA TRANSFER (Continued)				BOOLEAN VARIABLE MANIPULATION			
MOV	@Ri,direct	2	24	CLR	C	1	12
	Move direct byte to indirect RAM			CLR	bit	2	12
MOV	@Ri,#data	2	12	SETB	C	1	12
	Move immediate data to indirect RAM			SETB	bit	2	12
MOV	DPTR,#data16	3	24	CPL	C	1	12
	Load Data Pointer with a 16-bit constant				Complement Carry		
MOVC	A,@A+DPTR	1	24	CPL	bit	2	12
	Move Code byte relative to DPTR to Acc				Complement direct bit		
MOVC	A,@A+PC	1	24	ANL	C,bit	2	24
	Move Code byte relative to PC to Acc				AND direct bit to CARRY		
MOVX	A,@Ri	1	24	ANL	C,/bit	2	24
	Move External RAM (8-bit addr) to Acc				AND complement of direct bit to Carry		
MOVX	A,@DPTR	1	24	ORL	C,bit	2	24
	Move External RAM (16-bit addr) to Acc				OR direct bit to Carry		
MOVX	@Ri,A	1	24	ORL	C,/bit	2	24
	Move Acc to External RAM (8-bit addr)				OR complement of direct bit to Carry		
MOVX	@DPTR,A	1	24	MOV	C,bit	2	12
	Move Acc to External RAM (16-bit addr)				Move direct bit to Carry		
PUSH	direct	2	24	MOV	bit,C	2	24
	Push direct byte onto stack				Move Carry to direct bit		
POP	direct	2	24	JC	rel	2	24
	Pop direct byte from stack				Jump if Carry is set		
XCH	A,Rn	1	12	JNC	rel	2	24
	Exchange register with Accumulator				Jump if Carry not set		
XCH	A,direct	2	12	JB	bit,rel	3	24
	Exchange direct byte with Accumulator				Jump if direct Bit is set		
XCH	A,@Ri	1	12	JNB	bit,rel	3	24
	Exchange indirect RAM with Accumulator				Jump if direct Bit is Not set		
XCHD	A,@Ri	1	12	JBC	bit,rel	3	24
	Exchange low-order Digit indirect RAM with Acc				Jump if direct Bit is set & clear bit		
				PROGRAM BRANCHING			
				ACALL	addr11	2	24
					Absolute Subroutine Call		
				LCALL	addr16	3	24
					Long Subroutine Call		
				RET		1	24
					Return from Subroutine		
				RETI		1	24
					Return from interrupt		
				AJMP	addr11	2	24
					Absolute Jump		
				LJMP	addr16	3	24
					Long Jump		
				SJMP	rel	2	24
					Short Jump (relative addr)		

All mnemonics copyrighted © Intel Corporation 1980

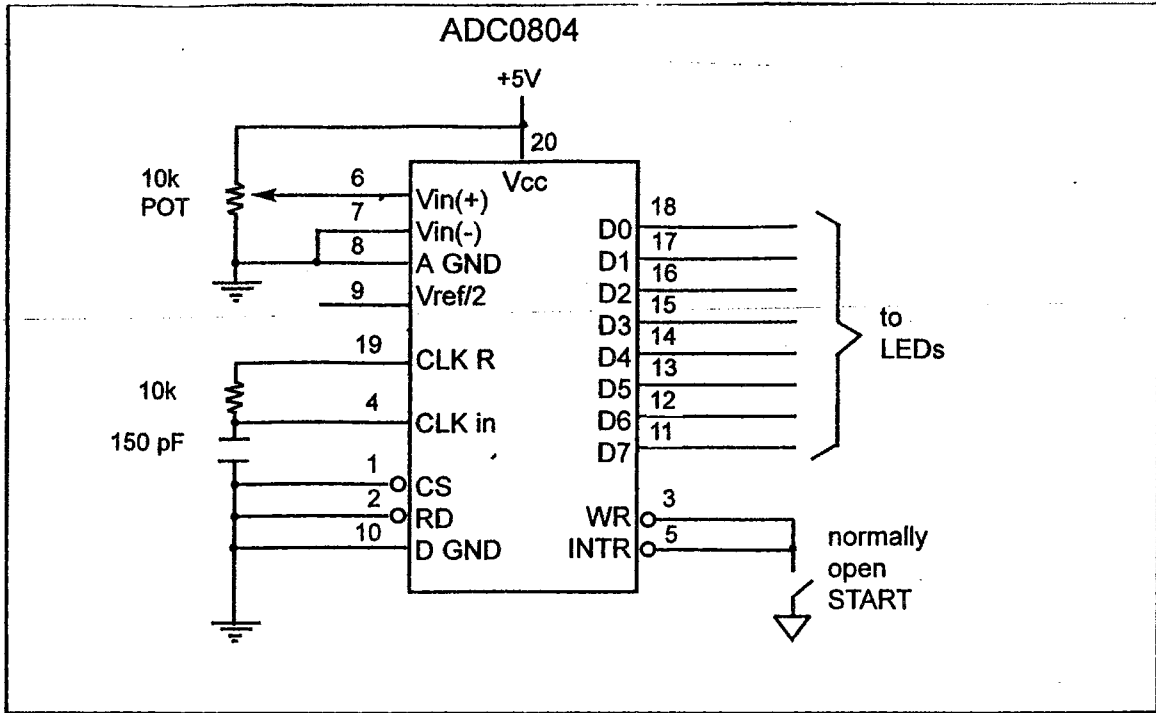
MCS[®]-51 PROGRAMMER'S GUIDE AND INSTRUCTION SET

Table 10. 8051 Instruction Set Summary (Continued)

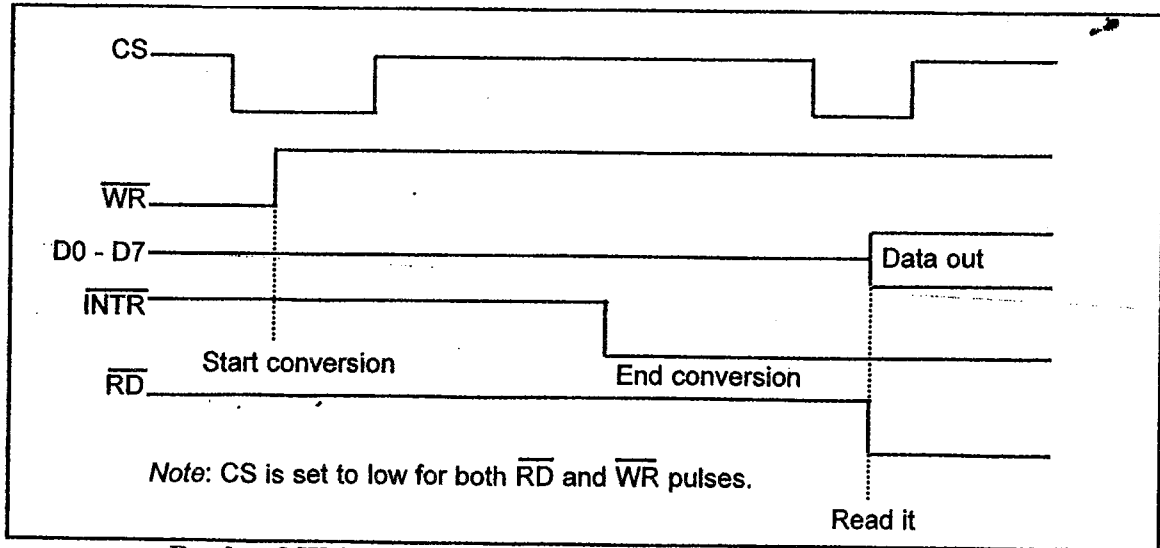
Mnemonic	Description	Byte	Oscillator Period
PROGRAM BRANCHING (Continued)			
JMP	@A + DPTR Jump indirect relative to the DPTR	1	24
JZ	rel Jump if Accumulator is Zero	2	24
JNZ	rel Jump if Accumulator is Not Zero	2	24
CJNE	A, direct, rel Compare direct byte to Acc and Jump if Not Equal	3	24
CJNE	A, # data, rel Compare immediate to Acc and Jump if Not Equal	3	24

Mnemonic	Description	Byte	Oscillator Period
PROGRAM BRANCHING (Continued)			
CJNE	Rn, # data, rel Compare immediate to register and Jump if Not Equal	3	24
CJNE	@Ri, # data, rel Compare immediate to indirect and Jump if Not Equal	3	24
DJNZ	Rn, rel Decrement register and Jump if Not Zero	2	24
DJNZ	direct, rel Decrement direct byte and Jump if Not Zero	3	24
NOP	No Operation	1	12

All mnemonics copyrighted ©Intel Corporation 1980



Testing ADC804 in Free Running Mode



Read and Write Timing for ADC804

1.

GATE	C/T	M1	M0	GATE	C/T	M1	M0
Timer 1				Timer 0			

TMOD Register

2.

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
-----	-----	-----	-----	-----	-----	-----	-----

TCON Register

3.

--	--	PT2	PS	PT1	PX1	PT0	PX0
----	----	-----	----	-----	-----	-----	-----

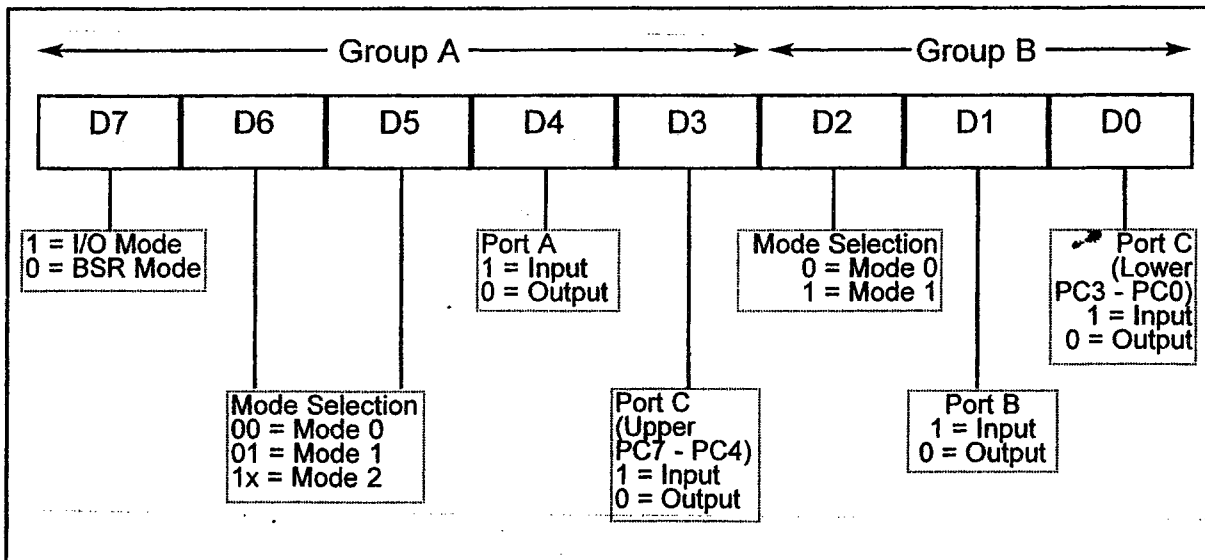
IP Register

4.

EA	--	ET2	ES	ET1	EX1	ET0	EX0
----	----	-----	----	-----	-----	-----	-----

IE Register

5.



8255 Control Word Format (I/O Mode)