UNIVERSITI SAINS MALAYSIA

Peperiksaan Kursus Semasa Cuti Panjang
Sidang Akademik 2004/2005

Mei 2005

EEE 320 – MIKROPEMPROSES II

Masa : 2 jam

ARAHAN KEPADA CALON:

Sila pastikan bahawa kertas peperiksaan ini mengandungi **TUJUH (7)** muka surat berserta **Lampiran (7 mukasurat)** bercetak dan **EMPAT (4)** soalan sebelum anda memulakan peperiksaan ini.

Jawab **TIGA (3)** soalan.

Agihan markah bagi soalan diberikan disudut sebelah kanan soalan berkenaan.

Jawab semua soalan di dalam Bahasa Malaysia.

...2/-

1. Rajah 1 adalah satu sistem mikropengawal 8031 dengan beberapa peranti luaran.
Figure 1 is an 8031 microcontroller system with several external devices.

(a) Dari Rajah 1, terangkan dengan JELAS bagaimana sistem ini dapat direkabentuk bagi menyokong kapasiti ingatan sebanyak 16K x 8 bit RAM.
From Figure 1, explain in DETAIL how the system can be designed to support the memory capacity up to 16K x 8 bits of RAM.

(20%)

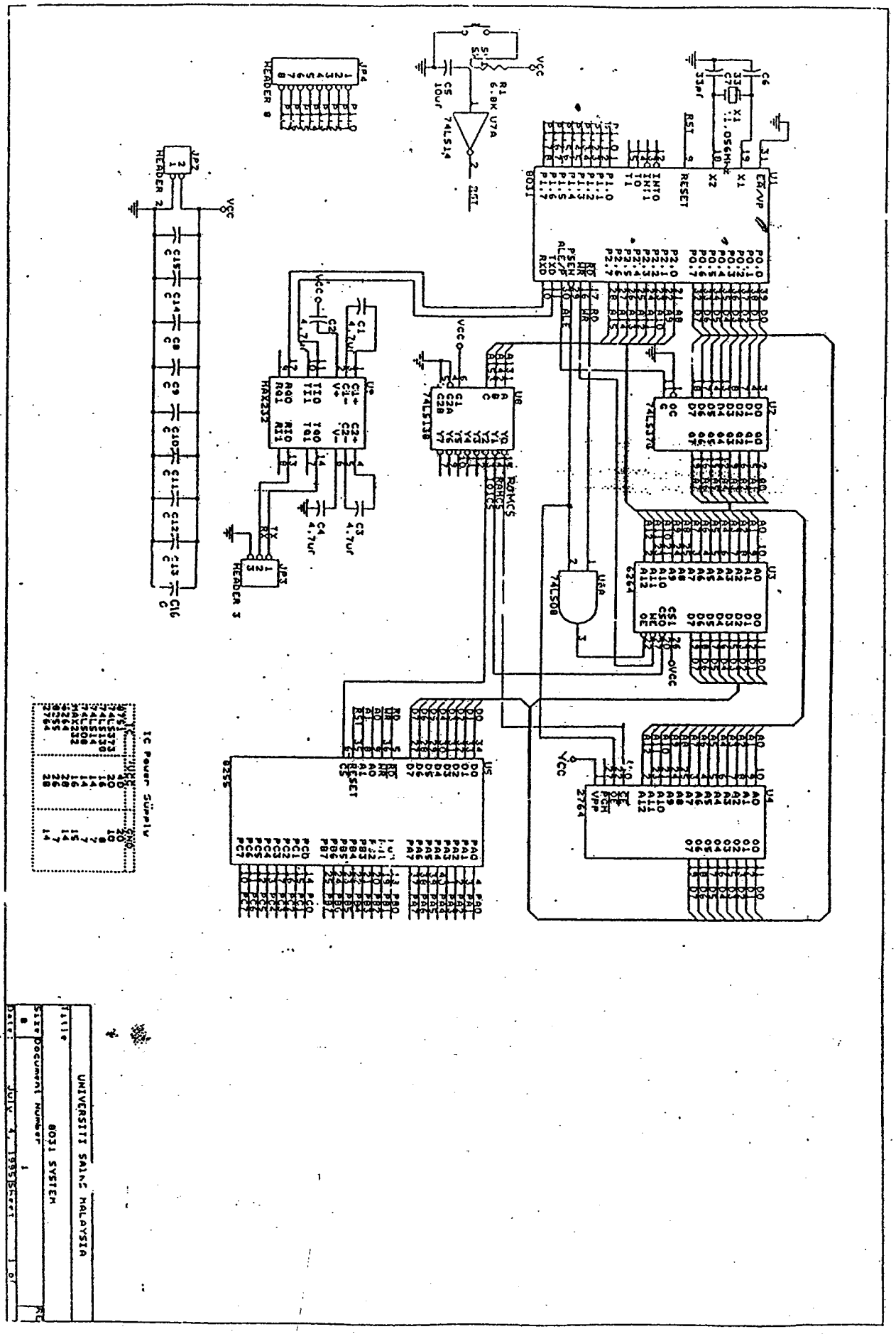
(b) Berdasarkan penjelasan yang diberikan dalam 1(a) dengan menggunakan Rajah 1, tambahkan bilangan peranti ingatan yang sesuai. Sila lakarkan sambungan yang lengkap.

Based on the explanation given in 1(a), using Figure 1, add the suitable numbers of memory. Please make connection perfectly.

(40%)

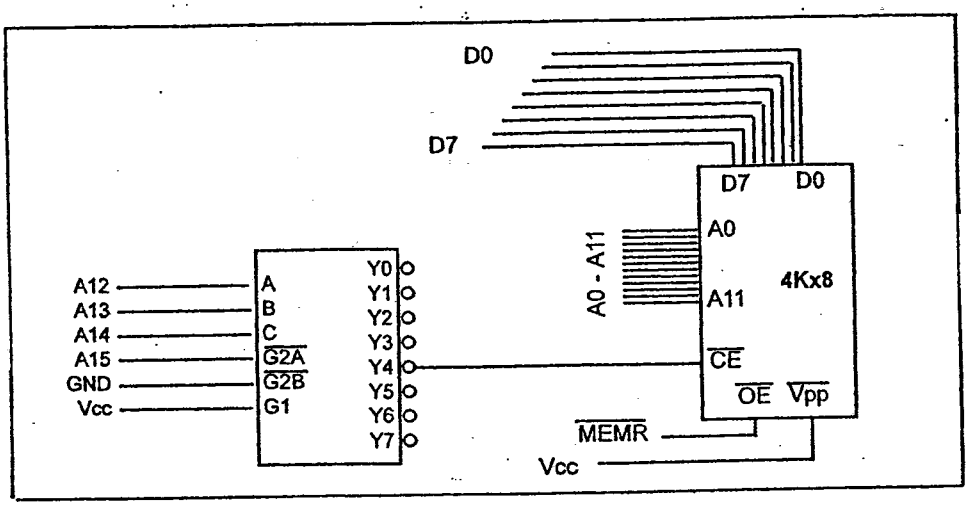
(c) Berdasarkan Rajah 2, dapatkan julat alamat bagi yang berikut:
Based on Figure 2, find the address range for the following:

(i) Y3
(ii) Y6
(iii) Y0 (40%)



Rajah 1
Figure 1

...4/-



Rajah 2
Figure 2

2. (a) Bagi sistem berasaskan 8031 dengan program ROM luaran:
For an 8031 system with external program ROM:

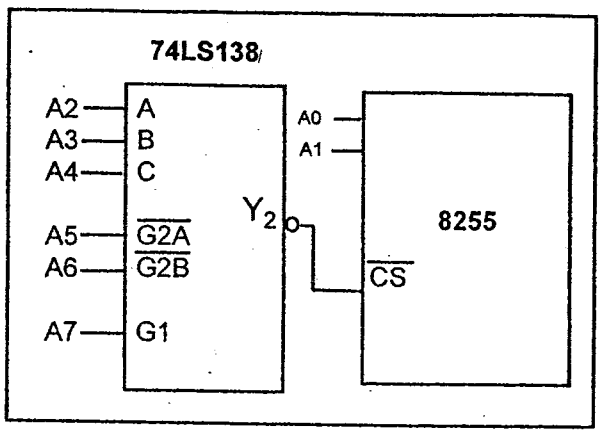
(i) Apabila mikropengawal dihidupkan, nyatakan alamat manakah 8031 akan mula membaca untuk arahan yang pertama dan terangkan apakah langkah berikutnya yang diambil oleh mikropengawal.

When microcontroller is powered up, state which address an 8031 will start read for the first instruction and explain what the next step will be taken by microcontroller.

(20%)

(b) Dari Rajah 3, dapatkan alamat asas untuk 8255.
From Figure 3, find the base address for 8255.

(20%)



Rajah 3
Figure 3

(c) Untuk Rajah 4,
For Figure 4,

(i) Dapatkan alamat port I/O yang ditetapkan untuk port A, B, C dan daftar kawalan.
Find the I/O port addresses assigned to ports A, B, C and control register.

(ii) Dapatkan bait kawalan bagi 8255 jika PA=keluaran, PB=keluaran, PC atas=masukan dan PC bawah=keluaran.

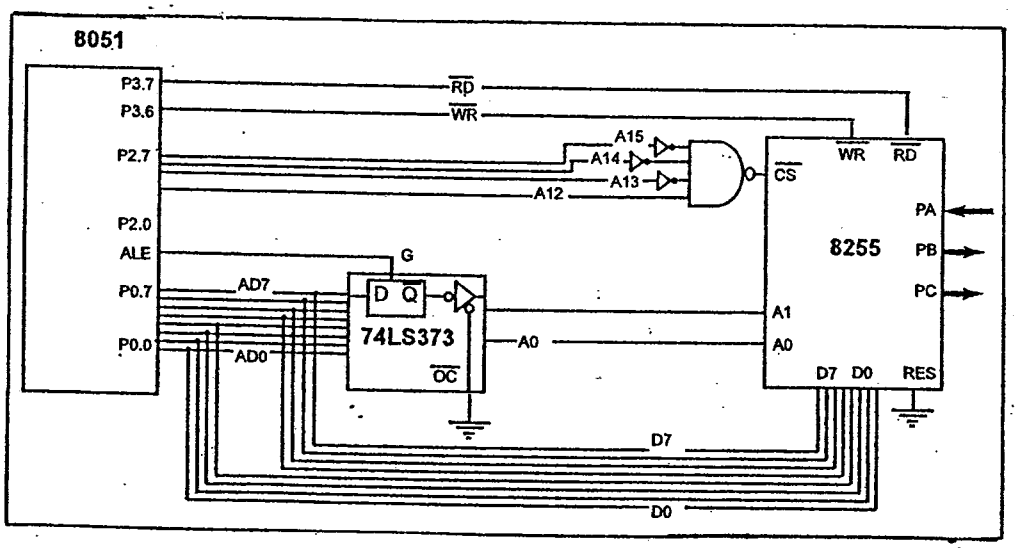
Find the control byte for 8255 if PA=output, PB=output, PC upper=input and PC lower=output.

...6/-

(iii) Tulis satu aturcara untuk mendapatkan data dari PB dan menghantar kepada PA.

Write a program to get data from PB and send it to PA.

(60%)



Rajah 4
Figure 4

3. (a) Nyatakan langkah-langkah yang perlu diambil bagi menghasilkan lengahan masa menggunakan pemasa mode 0.
State the steps that need to be taken to generate time delay using timer mode 0.

(30%)

(b) Anda dikehendaki merekabentuk satu sistem pengesan karbon monoksida menggunakan mikropengawal. Huraikan proses merekabentuk sistem tersebut. Cadangan mestilah mengandungi gambarajah blok, konsep operasi dan carta alir perisian untuk mengawal keseluruhan sistem. Anda bebas untuk membuat sebarang andaian.

You are required to design a carbon monoxide detector using microcontroller. Explain the process of designing of the system. The proposal should have block diagram, concept of operation and software flow chart to control all the system. You can make any assumptions.

(70%)

4. Daripada topik-topik yang dinyatakan di bawah, pilih 4 topik yang sesuai untuk membincangkan masalah-masalah yang terlibat dalam merekabentuk sistem pengawal terbenam untuk persekitaran hingar secara elektrik.

From the topics stated below, choose 4 suitable topics to discuss the problems which involved in designing embedded controller systems for electrically noisy environments.

(i) jenis dan sumber hingar elektrik
types and sources f electrical noise

(ii) kesan hingar
effects of noise

(iii) perlindungan
shielding

(iv) bumi
grounds

(v) agihan sumber kuasa dan nyahgandingan
power supply distribution and decoupling

(vi) strategi bentangan PCB
PCB layout strategy

(100%)

oooOooo

MCS®-51 INSTRUCTION SET

Table 10. 8051 Instruction Set Summary

Interrupt Response Time: Refer to Hardware Description Chapter.

Instructions that Affect Flag Settings(1)

Instruction	Flag			Instruction	Flag		
	C	OV	AC		C	OV	AC
ADD	X	X	X	CLR C	0		
ADDC	X	X	X	CPL C	X		
SUBB	X	X	X	ANL C,bit	X		
MUL	0	X		ANL C,/bit	X		
DIV	0	X		ORL C,bit	X		
DA	X			ORL C,bit	X		
RRC	X			MOV C,bit	X		
RLC	X			CJNE	X		
SETB C	1						

(1)Note that operations on SFR byte address 208 or bit addresses 209-215 (i.e., the PSW or bits in the PSW) will also affect flag settings.

Note on instruction set and addressing modes:

Rn — Register R7–R0 of the currently selected Register Bank.

direct — 8-bit internal data location's address. This could be an Internal Data RAM location (0–127) or a SFR [i.e., I/O port, control register, status register, etc. (128–255)].

@Ri — 8-bit internal data RAM location (0–255) addressed indirectly through register R1 or R0.

#data — 8-bit constant included in instruction.

#data 16 — 16-bit constant included in instruction.

addr 16 — 16-bit destination address. Used by LCALL & LJMP. A branch can be anywhere within the 64K-byte Program Memory address.space.

addr 11 — 11-bit destination address. Used by ACALL & AJMP. The branch will be within the same 2K-byte page of program memory as the first byte of the following instruction.

rel — Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is −128 to +127 bytes relative to first byte of the following instruction.

bit — Direct Addressed bit in Internal Data RAM or Special Function Register.

Mnemonic		Description	Byte	Oscillator Period
ARITHMETIC OPERATIONS				
ADD	A,Rn	Add register to Accumulator	1	12
ADD	A,direct	Add direct byte to Accumulator	2	12
ADD	A,@Ri	Add indirect RAM to Accumulator	1	12
ADD	A,#data	Add immediate data to Accumulator	2	12
ADDC	A,Rn	Add register to Accumulator with Carry	1	12
ADDC	A,direct	Add direct byte to Accumulator with Carry	2	12
ADDC	A,@Ri	Add indirect RAM to Accumulator with Carry	1	12
ADDC	A,#data	Add immediate data to Acc with Carry	2	12
SUBB	A,Rn	Subtract Register from Acc with borrow	1	12
SUBB	A,direct	Subtract direct byte from Acc with borrow	2	12
SUBB	A,@Ri	Subtract indirect RAM from ACC with borrow	1	12
SUBB	A,#data	Subtract immediate data from Acc with borrow	2	12
INC	A	Increment Accumulator	1	12
INC	Rn	Increment register	1	12
INC	direct	Increment direct byte	2	12
INC	@Ri	Increment direct RAM	1	12
DEC	A	Decrement Accumulator	1	12
DEC	Rn	Decrement Register	1	12
DEC	direct	Decrement direct byte	2	12
DEC	@Ri	Decrement indirect RAM	1	12

Table 10. 8051 Instruction Set Summary (Continued)

Mnemonic		Description	Byte	Oscillator Period
ARITHMETIC OPERATIONS (Continued)				
INC	DPTR	Increment Data Pointer	1	24
MUL	AB	Multiply A & B	1	48
DIV	AB	Divide A by B	1	48
DA	A	Decimal Adjust Accumulator	1	12
LOGICAL OPERATIONS				
ANL	A,Rn	AND Register to Accumulator	1	12
ANL	A,direct	AND direct byte to Accumulator	2	12
ANL	A,@Ri	AND indirect RAM to Accumulator	1	12
ANL	A,#data	AND immediate data to Accumulator	2	12
ANL	direct,A	AND Accumulator to direct byte	2	12
ANL	direct,#data	AND immediate data to direct byte	3	24
ORL	A,Rn	OR register to Accumulator	1	12
ORL	A,direct	OR direct byte to Accumulator	2	12
ORL	A,@Ri	OR indirect RAM to Accumulator	1	12
ORL	A,#data	OR immediate data to Accumulator	2	12
ORL	direct,A	OR Accumulator to direct byte	2	12
ORL	direct,#data	OR immediate data to direct byte	3	24
XRL	A,Rn	Exclusive-OR register to Accumulator	1	12
XRL	A,direct	Exclusive-OR direct byte to Accumulator	2	12
XRL	A,@Ri	Exclusive-OR indirect RAM to Accumulator	1	12
XRL	A,#data	Exclusive-OR immediate data to Accumulator	2	12
XRL	direct,A	Exclusive-OR Accumulator to direct byte	2	12
XRL	direct,#data	Exclusive-OR immediate data to direct byte	3	24
CLR	A	Clear Accumulator	1	12
CPL	A	Complement Accumulator	1	12

Mnemonic		Description	Byte	Oscillator Period
LOGICAL OPERATIONS (Continued)				
RL	A	Rotate Accumulator Left	1	12
RLC	A	Rotate Accumulator Left through the Carry	1	12
RR	A	Rotate Accumulator Right	1	12
RRC	A	Rotate Accumulator Right through the Carry	1	12
SWAP	A	Swap nibbles within the Accumulator	1	12
DATA TRANSFER				
MOV	A,Rn	Move register to Accumulator	1	12
MOV	A,direct	Move direct byte to Accumulator	2	12
MOV	A,@Ri	Move indirect RAM to Accumulator	1	12
MOV	A,#data	Move immediate data to Accumulator	2	12
MOV	Rn,A	Move Accumulator to register	1	12
MOV	Rn,direct	Move direct byte to register	2	24
MOV	Rn,#data	Move immediate data to register	2	12
MOV	direct,A	Move Accumulator to direct byte	2	12
MOV	direct,Rn	Move register to direct byte	2	24
MOV	direct,direct	Move direct byte to direct	3	24
MOV	direct,@Ri	Move indirect RAM to direct byte	2	24
MOV	direct,#data	Move immediate data to direct byte	3	24
MOV	@Ri,A	Move Accumulator to indirect RAM	1	12

Table 10. 8051 Instruction Set Summary (Continued)

Mnemonic		Description	Byte	Oscillator Period
DATA TRANSFER (Continued)				
MOV	@Ri,direct	Move direct byte to indirect RAM	2	24
MOV	@Ri, #data	Move immediate data to indirect RAM	2	12
MOV	DPTR, #data16	Load Data Pointer with a 16-bit constant	3	24
MOVC	A,@A+DPTR	Move Code byte relative to DPTR to Acc	1	24
MOVC	A,@A+PC	Move Code byte relative to PC to Acc	1	24
MOVX	A,@Ri	Move External RAM (8-bit addr) to Acc	1	24
MOVX	A,@DPTR	Move External RAM (16-bit addr) to Acc	1	24
MOVX	@Ri,A	Move Acc to External RAM (8-bit addr)	1	24
MOVX	@DPTR,A	Move Acc to External RAM (16-bit addr)	1	24
PUSH	direct	Push direct byte onto stack	2	24
POP	direct	Pop direct byte from stack	2	24
XCH	A,Rn	Exchange register with Accumulator	1	12
XCH	A,direct	Exchange direct byte with Accumulator	2	12
XCH	A,@Ri	Exchange indirect RAM with Accumulator	1	12
XCHD	A,@Ri	Exchange low-order Digit indirect RAM with Acc	1	12
BOOLEAN VARIABLE MANIPULATION				
CLR	C	Clear Carry	1	12
CLR	bit	Clear direct bit	2	12
SETB	C	Set Carry	1	12
SETB	bit	Set direct bit	2	12
CPL	C	Complement Carry	1	12
CPL	bit	Complement direct bit	2	12
ANL	C,bit	AND direct bit to CARRY	2	24
ANL	C,/bit	AND complement of direct bit to Carry	2	24
ORL	C,bit	OR direct bit to Carry	2	24
ORL	C,/bit	OR complement of direct bit to Carry	2	24
MOV	C,bit	Move direct bit to Carry	2	12
MOV	bit,C	Move Carry to direct bit	2	24
JC	rel	Jump if Carry is set	2	24
JNC	rel	Jump if Carry not set	2	24
JB	bit,rel	Jump if direct Bit is set	3	24
JNB	bit,rel	Jump if direct Bit is Not set	3	24
JBC	bit,rel	Jump if direct Bit is set & clear bit	3	24
PROGRAM BRANCHING				
ACALL	addr11	Absolute Subroutine Call	2	24
LCALL	addr16	Long Subroutine Call	3	24
RET		Return from Subroutine	1	24
RETI		Return from interrupt	1	24
AJMP	addr11	Absolute Jump	2	24
LJMP	addr16	Long Jump	3	24
SJMP	rel	Short Jump (relative addr)	2	24

Table 10. 8051 Instruction Set Summary (Continued)

Mnemonic		Description	Byte	Oscillator Period
PROGRAM BRANCHING (Continued)				
JMP	@A + DPTR	Jump indirect relative to the DPTR	1	24
JZ	rel	Jump if Accumulator is Zero	2	24
JNZ	rel	Jump if Accumulator is Not Zero	2	24
CJNE	A,direct,rel	Compare direct byte to Acc and Jump if Not Equal	3	24
CJNE	A, #data,rel	Compare immediate to Acc and Jump if Not Equal	3	24
CJNE	Rn, #data,rel	Compare immediate to register and Jump if Not Equal	3	24
CJNE	@Ri, #data,rel	Compare immediate to indirect and Jump if Not Equal	3	24
DJNZ	Rn,rel	Decrement register and Jump if Not Zero	2	24
DJNZ	direct,rel	Decrement direct byte and Jump if Not Zero	3	24
NOP		No Operation	1	12

HM6264BI Series

8,192-word × 8-bit High Speed CMOS Static RAM

HITACHI

ADE-203-492A (Z)
Rev. 1.0
Sep. 5, 1996

Description

The Hitachi HM6264BI is 64k-bit static RAM organized 8-kword × 8-bit. It realizes higher performance and low power consumption by 1.5 µm CMOS process technology. The device, packaged in 450 mil SOP (foot print pitch width), 600 mil plastic DIP, is available for high density mounting.

Features

- High speed
  - — Fast access time: 100/120 ns (max)
- Low power
  - — Standby: 10 µW (typ)
  - — Operation: 15 mW (typ) (f = 1 MHz)
- Single 5 V supply
- Completely static memory
  - — No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
  - — Three state output
- Directly TTL compatible
  - — All inputs and outputs
- Battery backup operation capability
- Operating temperature range
  - — –40°C to +85°C

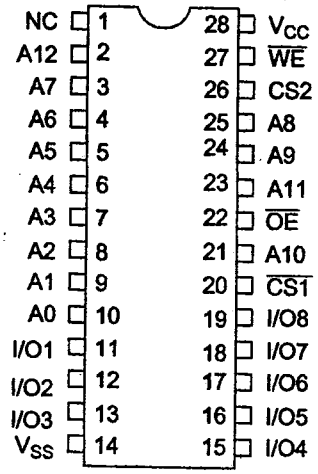
Ordering Information

Type No.	Access time	Package
HM6264BLPI-10	100 ns	600-mil, 28-pin plastic DIP (DP-28)
HM6264BLPI-12	120 ns	
HM6264BLFPI-10T	100 ns	450-mil, 28-pin plastic SOP(FP-28DA)
HM6264BLFPI-12T	120 ns	

HM6264BI Series

Pin Arrangement

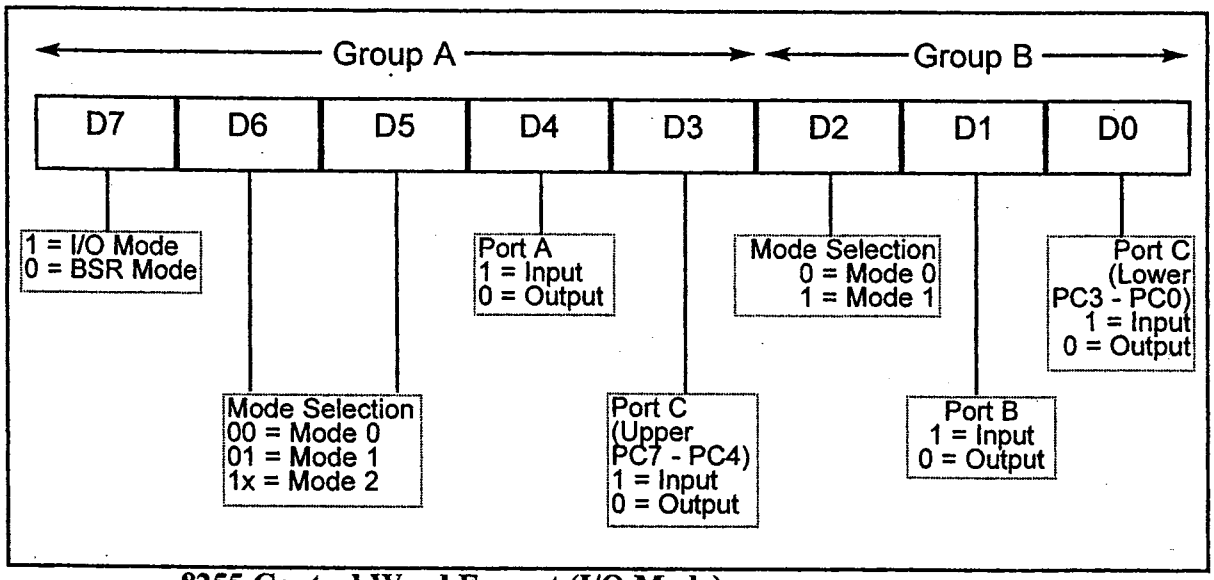
HM6264BLPI/BLFPI Series



(Top view)

Pin Description

Pin name	Function
A0 to A12	Address input
I/O1 to I/O8	Data input/output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
NC	No connection
V_{cc}	Power supply
V_{ss}	Ground



8255 Control Word Format (I/O Mode)

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