UNIVERSITI SAINS MALAYSIA

Peperiksaan Semester Pertama

Sidang Akademik 2004/2005

Oktober 2004

# EEE 241 – ELEKTRONIK ANALOG I

Masa : 3 Jam

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**ARAHAN KEPADA CALON:-**

Sila pastikan kertas peperiksaan ini mengandungi **TIGA BELAS (13)** muka surat beserta **(Lampiran 3 muka surat)** bercetak dan **ENAM (6)** soalan sebelum anda memulakan peperiksaan ini.

Jawab **LIMA (5)** soalan.

Agihan markah diberikan di sut sebelah kanan soalan berkenaan.

Semua soalan hendaklah dijawab di dalam Bahasa Malaysia.

...2/-

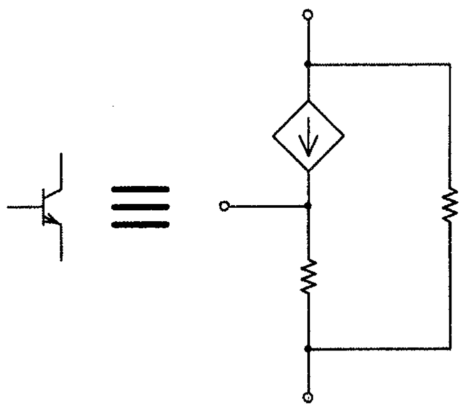
1. (a) Senaraikan **lima** ciri penguat BJT tapak-sepunya.
*State **five** main characteristic of a BJT common-base amplifier.*

(15%)

(b) **Rajah 1(a)** menunjukkan model isyarat kecil T bagi satu BJT. Lukiskan semula model ini dan labelkan semua unsurnya.

***Figure 1(a)** shows a small-signal T model for a BJT. Redraw the model and label all the elements.*

(10%)



**Rajah 1(a)**
***Figure 1(a)***

(c) Bagi penguat BJT tapak-sepunya dalam **Rajah 1(b)**;
*For the common-base BJT amplifier in **Figure 1(b)**;*

$R_B = 100\,\text{k}\Omega,\ R_C = 10\,\text{k}\Omega,\ R_E = 10\,\text{k}\Omega,\ R_s = R_L = 1\,\text{k}\Omega,\ V_{CC} = V_{EE} = 10\,\text{V}$.

Transistor Q mempunyai parameter-parameter berikut;
*The transistor Q has the following parameters;*

$V_{BE(\text{ON})} = 0.7\,\text{V},\ \beta = 100,\ V_A = \infty,\ V_T = 25\,\text{mV}$

[i] Lakukan analisis dc bagi mendapatkan nilai-nilai $V_B$, $V_C$ dan $V_E$.

*Perform a dc analysis to obtain the values of* $V_B$, $V_C$ *and* $V_E$.

(25%)

[ii] Dengan menggunakan model T bagi transistor Q, lukis dan labelkan litar setara bagi penguat tersebut. Anda boleh mengabaikan kesan-kesan $r_o$ dan semua kapasitans.

*Draw and label the equivalent circuit for the amplifier using T model for the transistor Q. You may neglect the effects of* $r_o$ *and all capacitances.*

(15%)

[iii] Cari gandaan arus isyarat kecil $A_i = i_o / i_i$ dan gandaan voltan isyarat kecil $A_v = v_o / v_s$.

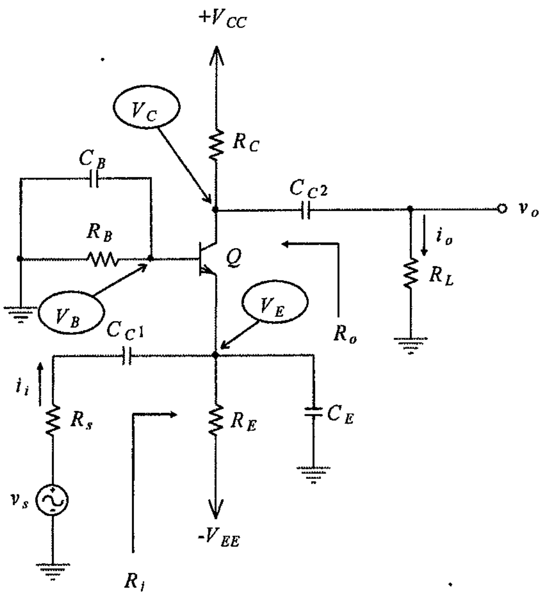
*Find the small-signal current gain* $A_i = i_o / i_i$ *and small-signal voltage* $A_v = v_o / v_s$.

(25%)

[iv] Cari rintangan masukan $R_i$ dan rintangan keluaran $R_o$.

*Determine the input resistance* $R_i$ *and output resistance* $R_o$.

(10%)




**Rajah 1(b)**
***Figure 1(b)***

2. **Rajah 2(a)** menunjukkan penguat salir-sepunya atau "*source-follower*". $Q_1$, $Q_2$ dan $Q_3$ dalam adalah MOSFET daripada jenis yang sama.

***Figure 2(a)*** *shows a common-drain amplifier or source-follower. $Q_1$, $Q_2$ and $Q_3$ are identical MOSFETs.*

(a) Lakukan analisis isyarat kecil ke atas litar penguat ini bagi membuktikan bahawa;

*Perform a small-signal analysis on this amplifier circuit to show that;*

[i] ungkapan bagi gandaan voltan $A_v \equiv v_o / v_i$ ialah;

*the expression for voltage gain $A_v \equiv v_o / v_i$ is;*

$$A_v \approx \frac{1}{1+\chi}$$

[ii] ungkapan bagi rintangan keluaran $R_o$ ialah;

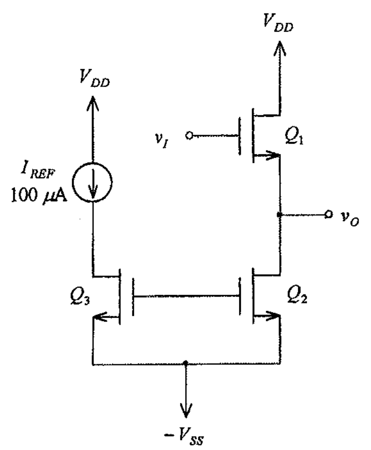
*the expression for output resistance $R_o$ is;*

$$R_o \approx \frac{1}{g_{m1}(1+\chi)}$$

di mana;

*where;*

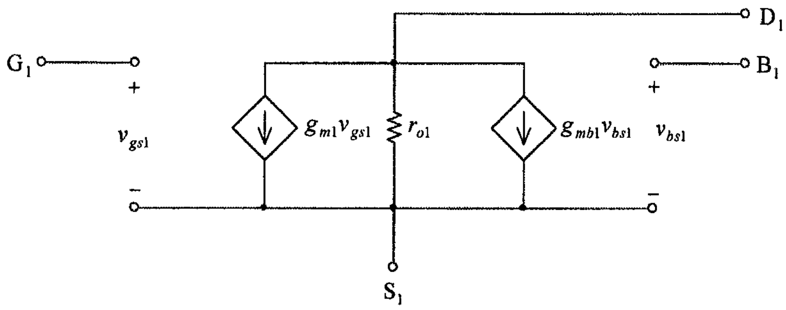
$$\chi = \frac{g_{mb1}}{g_{m1}}$$




**Rajah 2(a)**
***Figure 2(a)***

Anda boleh menggunakan model isyarat kecil seperti yang ditunjukkan dalam **Rajah 2(b)** bagi MOSFET.

*You may use the small-signal model shown in **Figure 2(b)** for the MOSFET.*




**Rajah 2(b)**
***Figure 2(b)***

(60%)

(b) $Q_1$, $Q_2$ dan $Q_3$ masing-masing mempunyai parameter-parameter berikut;
*Each of $Q_1$, $Q_2$ and $Q_3$ has the following parameters;*

$V_{t0} = 1\,\text{V}$, $W = 70\,\mu\text{m}$, $L = 5\,\mu\text{m}$, $\mu_n C_{ox} = 80\,\mu\text{A/V}^2$, $V_A = 90\,\text{V}$,
$\gamma = 0.7\,\text{V}^{1/2}$, $2\phi_f = 0.6\,\text{V}$,

Bagi julat isyarat masukan 3 V dan julat voltan salir-badan $V_{SB}$ dari 1 V hingga 4 V, cari julat;

*For an input signal range of 3 V and source-body voltage $V_{SB}$ of 1 V to 4 V, find the range of;*

[i] $A_v$;
[ii] $R_o$;

Di mana yang berkenaan, anda boleh gunakan jadual persamaan-persamaan MOSFET yang diberikan dalam Lampiran;

*Where applicable, you may use the table of MOSFET equations provided in the Appendix.*

(40%)

...6/-

3. Penguat dua peringkat dalam **Rajah 3** adalah gabungan secara "*cascode*" penguat-penguat sumber-sepunya dan get-sepunya. $Q_1$ dan $Q_2$ adalah NMOS daripada jenis yang sama dan masing-masing mempunyai parameter-parameter berikut;

*The two-stage amplifier in **Figure 3** is in a cascode connection of a common-source and a common-gate amplifiers. Each of the identical NMOS $Q_1$ and $Q_2$ has the following parameters;*

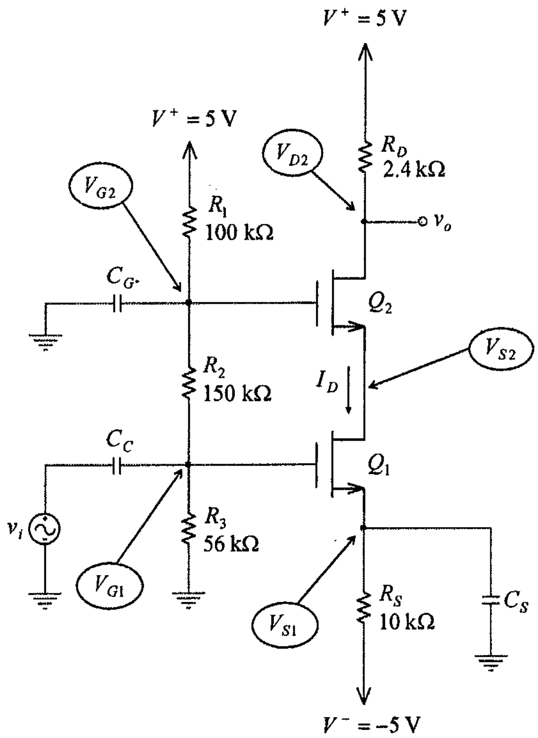
$$V_t = 1.2\text{ V}; \ \frac{1}{2}k_n'\left(\frac{W}{L}\right) = 0.8\text{ mA/V}^2; \ \lambda = 0.$$

(a) Lukiskan litar setara a.t. bagi penguat.
*Draw the dc equivalent circuit of the amplifier.*

(15%)

(b) Kira nilai-nilai a.t. bagi $V_{G1}$; $V_{G2}$; $I_D$; $V_{S1}$; $V_{S2}$ dan $V_{D2}$.
*Calculate dc values of $V_{G1}$; $V_{G2}$; $I_D$; $V_{S1}$; $V_{S2}$ and $V_{D2}$.*

(40%)




**Rajah 3**
***Figure 3***

(c) Dengan mengandaikan semua kapasitor berlitar pintas pada frekuensi isyarat tertentu, lukiskan litar setara a.t. bagi penguat.

*Assuming that all capacitors are short circuited at certain signal frequency, draw the ac equivalent circuit of the amplifier.*

(15%)

(d) Dengan menggunakan model "*hybrid-π*" bagi $Q_1$ dan $Q_2$, lukiskan litar setara isyarat kecil bagi penguat dan cari gandaan voltan keseluruhan.

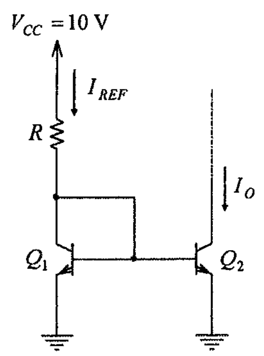
*Using hybrid-π model for $Q_1$ and $Q_2$, draw small-signal equivalent circuit for the amplifier and calculate its overall voltage gain.*

(30%)

4. (a) **Rajah 4(a)** menunjukkan satu sumber arus malar yang asas. $Q_1$ dan $Q_2$ adalah BJT sepadan dan masing-masing mempunyai $V_{BE} = 0.7\text{ V}$ pada nilai arus pemungut 1 mA. Dengan mengandaikan nilai $\beta$ yang teramat tinggi dan $V_T = 25\text{ mV}$, rekabentuk litar untuk mendapatkan arus keluaran $I_O = 10\ \mu\text{A}$.

***Figure 4(a)*** *shows a basic constant current source. $Q_1$ and $Q_2$ are matched BJT and each has a $V_{BE} = 0.7\text{ V}$ at a collector current of 1 mA. Assuming that the value of $\beta$ is very high and that $V_T = 25\text{ mV}$, design the circuit to obtain an output current $I_O = 10\ \mu A$.*

(10%)




**Rajah 4(a)**
***Figure 4(a)***

(b) Jelaskan masalah yang dihadapi untuk membina sumber arus asas seperti dalam **Rajah 4(a)** di atas litar bersepadu dan jelaskan bagaimana masalah ini dapat di atasi dengan penambahan satu perintang pada litar tersebut.

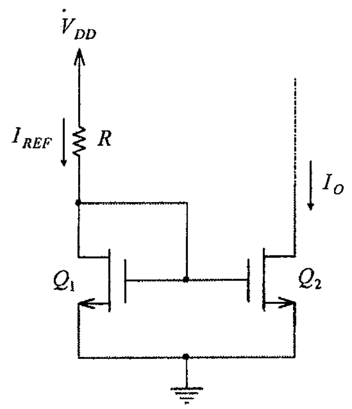
*Explain the problem encountered in implementing the basic current source in **Figure 4(a)** on integrated circuit and decribe how this problem may be overcome by adding another resistor to the circuit.*

(30%)

(c) Buktikan bahawa sekiranya transistor-transistor $Q_1$ dan $Q_2$ bagi sumber arus dalam **Rajah 4(b)** adalah sepadan, kaitan di antara arus keluaran $I_O$ dengan arus rujukan $I_{REF}$ ditentukan oleh geometri transistor sahaja. Anda boleh mengandaikan arus get adalah sifar.

*Show that if $Q_1$ and $Q_2$ in the current source circuit of **Figure 4(b)** are matched transistors, the relationship between the output current $I_O$ and the reference current $I_{REF}$ is solely determined by the geometry of the transistors. You may assume that the gate current is zero.*

(30%)




**Rajah 4(b)**
***Figure 4(b)***

(d) **Rajah 4(c)** menunjukkan dua unit sumber arus asas disambung secara kaskod bagi meninggikan nilai rintangan keluaran $R_O$.

***Figure 4(c)*** *shows two units of basic current sources connected in cascode to increase its output resistance* $R_O$.

[i] Lukiskan litar setara ac bagi sumber arus tersebut.
*Draw the ac equivalent circuit for the current source.*

[ii] Lukiskan litar isyarat kecil dengan menggunakan model "*hybrid-π*" bagi transistor.
*Draw the small-signal equivalent circuit using a "hybrid-π" model for the transistors.*

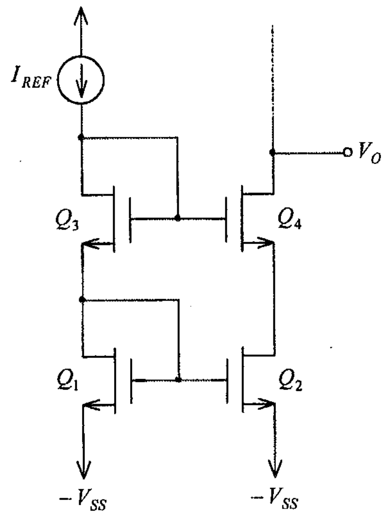
[iii] Lakukan analisis ac ke atas sumber arus kaskod ini untuk mendapatkan satu ungkapan hampiran bagi rintangan keluarannya dalam sebutan $r_{o2}$, $g_{m4}$ dan $r_{o4}$.

*Perform an ac analysis on the cascode current source to obtain an approximate expression for its output resistance in terms of* $r_{o2}$, $g_{m4}$ *and* $r_{o4}$.

Abaikan kesan badan dan andaikan bahawa rintangan bagi transistor-transistor sambungan diod adalah rendah dan boleh diabaikan

*Neglect body effect and assume that the resistances of diode-connected transistors are very low and may be neglected.*

(30%)




**Rajah 4(c)**
***Figure 4(c)***

5. Transistor dalam penguat tapak-sepunya dalam **Rajah 5**, mempunyai arus pincang 1 mA, $\beta$ = 100, $C_\mu$ = 0.8 pF dan $f_T$ = 600 MHz;

*The transistor in the common-base amplifier in Figure 5 has a bias current 1 mA, $\beta$ = 100, $C_\mu$ = 0.8 pF and $f_T$ = 600 MHz;*

(a) Anggarkan gandaan voltan jalur tengah $v_o/v_s$;

*Estimate the midband gain $v_o/v_s$;*

(20%)

(b) Gunakan kaedah pemalar-masa litar-pintas bagi menganggarkan frekuensi 3-dB bawah, $f_L$;

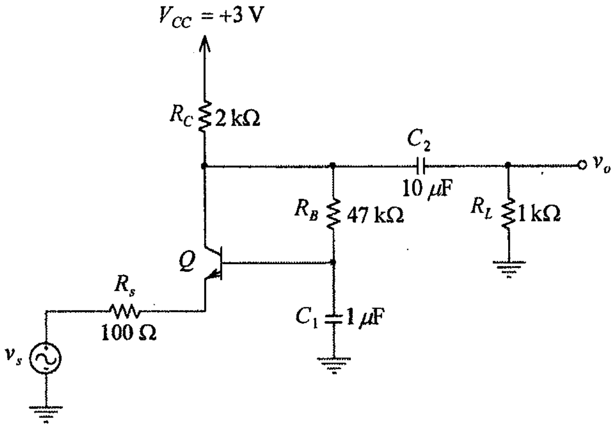
*Use the short-circuit time-constant method to estimate the lower 3-dB frequency $f_L$;*

(50%)

(c) Cari kutub-kutub frekuensi tinggi dan anggarkan frekuensi 3-dB atas, $f_H$;

*Find the high-frequency poles, and estimate the upper 3-db frequency, $f_H$;*

(30%)




**Rajah 5**
***Figure 5***

6. (a) Jelaskan bagaimana titik "quiescent" bagi penguat isyarat besar dalam **Rajah 6** dapat ditentukan melalui pemilihan nilai $R_1$ dan $R_2$.

*Explain how the quiescent point of the large-signal amplifier shown in **Figure 6** may be determined through a proper selection of $R_1$ and $R_2$.*

(40%)

(b) Transistor $Q_N$ dan $Q_P$ dalam **Rajah 6** adalah sepadan dan masing-masing mempunyai arus tepu $I_S = 1.482 \times 10^{-15}$ A . $Q_1$ pula mempunyai arus tepu $I_{S1} = 6.668 \times 10^{-15}$ A. Nilai arus pemungut "*quiescent*" bagi $Q_N$ ialah $I_Q = 10$ mA. Sumber isyarat $v_I$ membekalkan voltan isyarat sinus dengan amplitud 10 V.

*$Q_N$ and $Q_P$ in **Figure 6** are matched transistors and each has a saturation current $I_S = 1.482 \times 10^{-15}$ A. $Q_1$ has a saturation current $I_{S1} = 6.668 \times 10^{-15}$ A. The quiescent collector current of $Q_N$ is 10 mA. The signal source $v_I$ provides a sinusoidal voltage of amplitude 10 V.*

**Table 4.3** RELATIONSHIPS BETWEEN THE SMALL-SIGNAL MODEL PARAMETERS OF THE BJT

Model Parameters in Terms of DC Bias Currents:

$$g_m = \frac{I_C}{V_T} \qquad r_e = \frac{V_T}{I_E} = \alpha\left(\frac{V_T}{I_C}\right)$$

$$r_\pi = \frac{V_T}{I_B} = \beta\left(\frac{V_T}{I_C}\right) \qquad r_o = \frac{V_A}{I_C}$$

In terms of $g_m$:

$$r_e = \frac{\alpha}{g_m} \qquad r_\pi = \frac{\beta}{g_m}$$

In terms of $r_e$:

$$g_m = \frac{\alpha}{r_e} \qquad r_\pi = (\beta + 1)r_e \qquad g_m + \frac{1}{r_\pi} = \frac{1}{r_e}$$

Relationships between $\alpha$ and $\beta$:

$$\beta = \frac{\alpha}{1 - \alpha} \qquad \alpha = \frac{\beta}{\beta + 1} \qquad \beta + 1 = \frac{1}{1 - \alpha}$$

## Table 5.4 SUMMARY OF IMPORTANT MOSFET EQUATIONS

### Current-Voltage Relationships

■ For NMOS Devices:

- *Triode region* ($v_{GS} \geq V_t$, $v_{DS} \leq v_{GS} - V_t$)

$$i_D = k'_n \left(\frac{W}{L}\right)\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2} v_{DS}^2\right]$$

For small $v_{DS}$: $r_{DS} \equiv \dfrac{v_{DS}}{i_D} = \left[k'_n \left(\dfrac{W}{L}\right)(v_{GS} - V_t)\right]^{-1}$

- *Saturation region* ($v_{GS} \geq V_t$, $v_{DS} \geq v_{GS} - V_t$)

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L}\right)(v_{GS} - V_t)^2 (1 + \lambda v_{DS})$$

- $k'_n = \mu_n C_{ox}$ ~~(see Table 5.1)~~

$V_t = V_{t0} + \gamma [\sqrt{2\phi_f + |V_{SB}|} - \sqrt{2\phi_f}]$

$\gamma = \sqrt{2qN_A\varepsilon_s}/C_{ox}$, $q = 1.6 \times 10^{-19}$ coulomb, $\varepsilon_s = 1.04 \times 10^{-12}$ F/cm

$\lambda = 1/V_A$, $V_A \propto L$

■ For PMOS Devices: $V_t$, $\gamma$, $\lambda$ and $V_A$ are negative

- For triode region, $v_{GS} \leq V_t$ and $v_{DS} \geq v_{GS} - V_t$
- For saturation region, $v_{GS} \leq V_t$ and $v_{DS} \leq v_{GS} - V_t$

■ For Depletion Devices (refer to Fig. 5.23):

- $n$ channel: $V_t$ is negative
- $p$ channel: $V_t$ is positive
- $I_{DSS} = \dfrac{1}{2} k' \left(\dfrac{W}{L}\right) V_t^2$