UNIVERSITI SAINS MALAYSIA

First Semester Examination
2015/2016 Academic Session

December 2015 / January 2016

EEE 520 – Embedded Microprocessor Systems

Duration : 3 hours

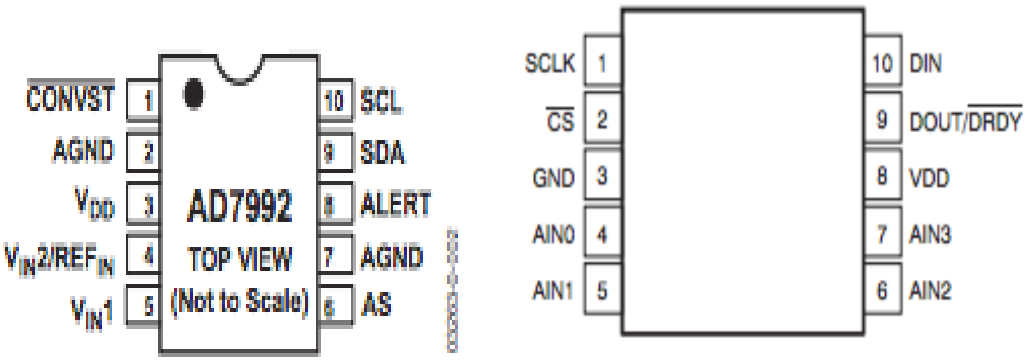
Please check that this examination paper consists of **SEVEN (7)** pages printed material before you begin the examination.

Instructions: This question paper consists **SIX (6)** questions. Answer **FIVE (5)** questions. All questions carry the same marks.

1. (a) Figure 1(a) shows electronic devices to convert analog signal to digital signal in embedded system design. Answer the following questions :

(i) Explain about communication protocol for the devices.

(ii) Give advantage and disadvantage of the communication protocol for each device.



(a) (b)

Figure 1(a)

(40 marks)

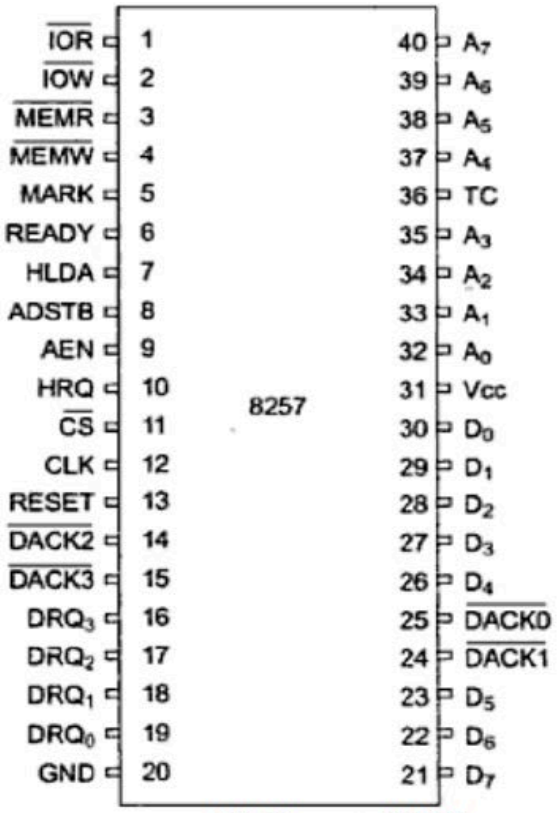
(b) Read the following statements :

Most of the car drivers used a reverse radar or a reverse camera to detect the road situation behind the vehicle when it is engaged in reverse gear. As a matter of fact, the pedestrians can virtually know if the vehicle is backing up or not only by seeing the permanent bright reverse lamps. And as there is not much change with the reverse lamp to be seen, therefore their warning function for pedestrians seems to be still insufficient eventually.

Propose an embedded system to improve the existing reverse lamp so that pedestrians can get sufficient information of the event.

(60 marks)

2. (a)



Pin Diagram of 8257

Figure 2(a)

Figure 2(a) shows DMA controller. DACK0 – DACK3 are DMA acknowledge and DRQ0- DRQ3 are DMA request. Answer the following questions:

(i) Explain the operating sequence of the DMA controller.

(ii) Propose a data path circuit with the DMA controller.

(20 marks)

(b) Figure 2(b) shows the AT25010 and table 1 shows the pin configuration. It provides serial electrically erasable read only memory (EEPROM). The AT25010A is enabled through the Chip Select pin (CS) and accessed via a three-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). All programming cycles are completely self-timed, and no separate erase cycle is required before write. Hardware data protection is provided via the WP pin to protect against inadvertent write attempts. The HOLD pin may be used to suspend any serial communication without resetting the serial sequence. Based on the information:

Propose a data path for the communication between one master and four slaves of AT25010.

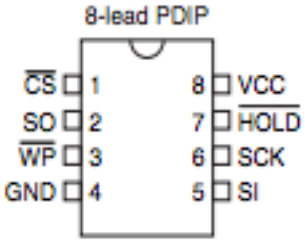


Table 1

Pin Name	Function
$\overline{CS}$	Chip Select
SCK	Serial Data Clock
SI	Serial Data Input
SO	Serial Data Output
GND	Ground
VCC	Power Supply
$\overline{WP}$	Write Protect
$\overline{HOLD}$	Suspends Serial Input

Figure 2(b)

(40 marks)

(c) Consider a controller for traffic at the intersection of a main highway and a country road. The following specifications must be considered.

(a) the traffic signal for the main highway gets highest priority because cars are continuously present on the main highway. Thus, the main highway signal remains green by default.

(b) Occasionally cars from the country road arrive at the traffic signal. The traffic signal for the country road must turn green only long enough to let the cars on the country road go.

(c) As soon as there are no cars on the country road, the country road traffic signal turns yellow and then red and the traffic signal on the main highway turns green again.

(d) There is a sensor to detect cars waiting on the country road. The sensor sends a signal X as input to the controller. X = 1 if there are no cars on the country road; otherwise X = 0.

Answer the following questions:

(i) Draw a state diagram to design the traffic light controller.
(ii) Based on the state diagram write Verilog code to implement the traffic light controller.

(40 marks)

3. (a) There are two types of activation level for interrupting the CPU. Describe briefly both of the activation levels. Assign 2 peripheral which suitable for each of the activation level of interrupt in CPU. Justify you selection.

(40 marks)

(b)

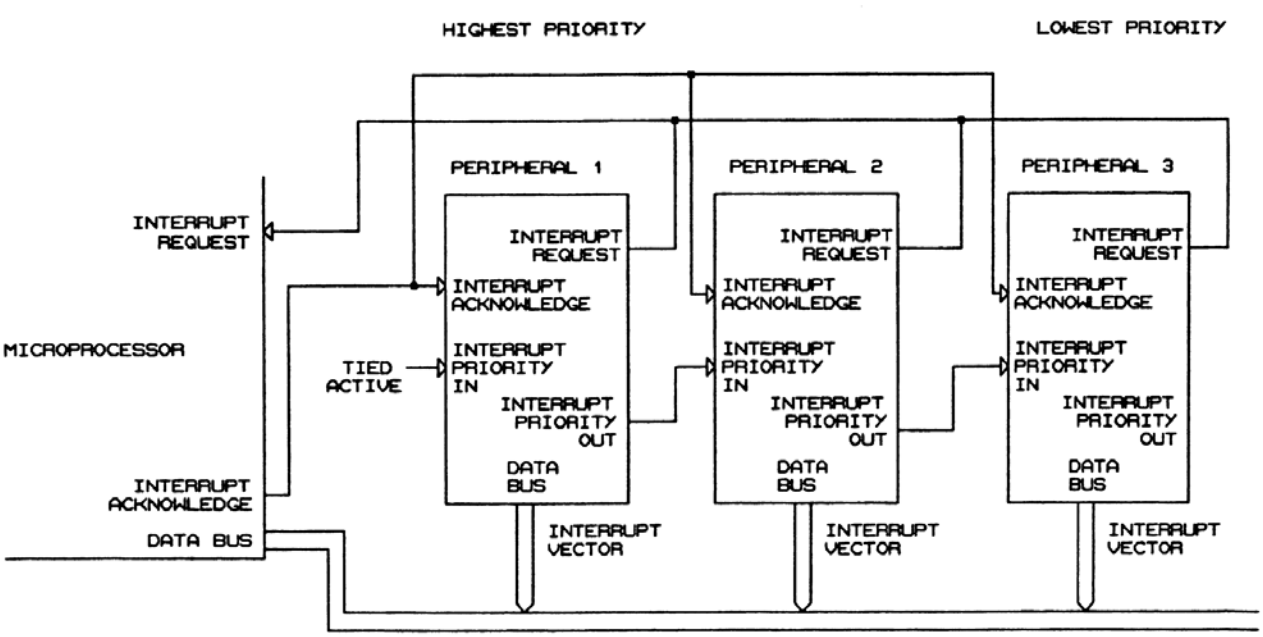


Figure 3(b)

Figure 3(b) above is a block diagram for daisy-chained system of interrupt in embedded system. Describe briefly how the system operates. Assign 3 suitable peripheral as in above Figure 3(b) and explain.

(60 marks)

4. (a) There are several tools which could be used to debug an embedded system. Logic analyzer or digital oscilloscope can be used as a debug tools. Explain how both of the tools to identify the error in embedded system.

(50 marks)

(b) Circular trace buffer is software tools to debug an embedded system. Describe briefly the operation of the tools and list down advantages and disadvantages of the tools.

(50 marks)

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5. (a) Many embedded systems target real-time applications. What characterizes a real-time system? Give an example of embedded real-time systems.

(20 marks)

(b) Real-time operating systems play an important role in the design of real-time systems. How do real-time operating systems differ from general purpose operating systems and what are the features you might expect to be provided by a real-time operating system kernel?

(20 marks)

(c) What are modeling and computation in relation to embedded processor system design and the 10 levels of hardware modeling? Provide relevant examples.

(60 marks)

6. (a) What are the differences between “process” and “threads” in relation to a RTOS embedded system application? Provide relevant diagrams.

(20 marks)

(b) Provide suitable descriptions for the following types of multitasking :

(i) Co-operative Multitasking

(ii) Preemptive Multitasking

(iii) Non-preemptive Multitasking

(20 marks)

(c) What are the importance of shared memory and the utilisation of priority inversion and priority inheritance? Provide sufficient explanation.

(30 marks)

(d) Three processes with process IDs – P1, P2 and P3 with estimated completion time 10, 5, 7 milliseconds and priorities 1, 3, 2 (0 – highest priority, 3 – lowest priority) respectively enters the ready queue together. A new process P4 with estimated completion time 6 ms and priority 0 enters the ‘Ready’ queue after 5 ms of start execution of P1. Assume all the processes contain only CPU operation and no I/O operations are involved. Determine the timing representation for all the processes, i.e. the average turn-around-time.

(30 marks)

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