UNIVERSITI SAINS MALAYSIA

First Semester Examination
2015/2016 Academic Session

December 2015 & January 2016

EEE 554/4 – Digital Integrated Circuit Design

Duration : 3 hours

Please check that this examination paper consists of **FIVE (5)** pages printed material and **ONE (1)** page of Appendix before you begin the examination.

Instructions: This question paper consists **SIX (6)** questions. Answer **FIVE (5)** questions. All questions carry the same marks.

1. (a) Design a digital circuit based on following specification using Verilog HDL. You have to use the concept of connection of instances for the top level module, where the top level module only consists of the instances of low level module. As for the low level module, you may use any type of description. However, you are not allowed to use the arithmetic operator (*). You need to develop also the test bench to verify the designed circuit. No need to test all combinations.

The circuit has two inputs (A and B) and each of it is in the range of 0 to 7. An output OUT is based on following conditions:-
If A is an even number and B is an odd number, OUT = A * 2;
If A is an odd number and B is an even number, OUT = B * 2;
If both are even numbers, OUT = A + B;
If both are odd numbers, OUT = (A + B)*2;

(80 marks)

(b) Find a test pattern that can detect *s-a-1* at *net u* of the following circuit

```
module circuit1(f, a, b, c, d);
  output f;
  input a, b, c, d;

  and (p, a, b);
  not (r, c);
  and (u, r, d);
  or (v, p, c);
  not (t, p);
  or (w, t, u);
  and (f, v, w);

endmodule
```

(20 marks)

2. Design a digital circuit for a sequence detector based on following specification. Develop the block diagram (consists of datapath and control units) and the ASMD chart.

The inputs are as follows :-

(i) An input IN (IN is an unsigned integer in the range of 0 to 3).

(ii) A 4-digit number SEQ0, SEQ1, SEQ2, SEQ3 (each of it is an unsigned integer in the range of 0 to 3)

(iii) A 1-bit CLR that will clear the output signal OUT

(iv) A 1-bit START that will start the operation

(iv) A 1-bit RESET (asynchronous, active low) that will reset the circuit

(v) A 1-bit CLK as the clock

The output OUT is a 1-bit signal that will be asserted in the next clock cycle when the input IN for four consecutive clock cycles are equal to SEQ0, SEQ1, SEQ2 and SEQ3, respectively. The output signal OUT should remain high until the CLR input is asserted. Assume that the input IN is available at every clock cycle as long as the START signal is asserted. Kindly refer to Appendix A for an example of the simulation results.

(100 marks)

3. Write Verilog codes for the designed circuit in Question 2.

(100 marks)

4. (a) There are significant changes in the standard cell libraries as the technology progress beyond deep submicron regime. In your own words, explain the evolution of these standard libraries taking into account the contents of the library itself.

(30 marks)

(b) You are given a task to assist a new intern with a macro placement. With an example, show the intern how you would place the macros. Make sure that your macro placement will not suffer from routing congestion.

(30 marks)

(c) It is known that Clock Tree Synthesis is necessary for placement. However there are some negative effects due to CTS, especially when it comes to routing. Describe what the problems that associated with CTS are and how you might solve them.

(40 marks)

5. (a) Before you start on your back-end design, it is necessary to plan your design first. Why do you think this is the case? What is the important planning that you need to include in the design planning?

(50 marks]

(b) Using Figure 5(b) as an example, illustrate the placement flow considering the floorplanning and the power planning. Label the I/O, core, power and ground grid accordingly on the figures.

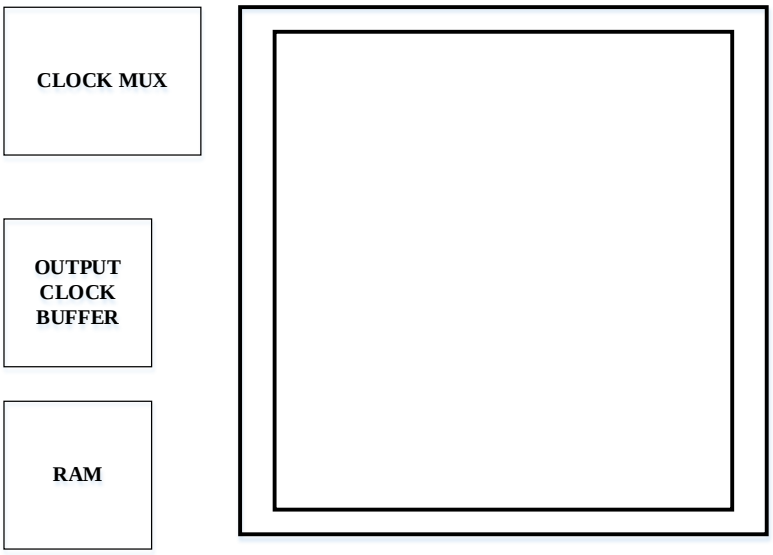

Figure 5(b)

(50 marks)

6. (a) A back-end designer is given a design where the ICG cells have been inserted. However he/she found out that there is a clock gating violation where the ICG cells are placed too far away from the flip-flop. Show how you help this designer solve this problem without changing the number of existing flip-flops.

(30 marks)

(b) During floorplanning stage, it has been decided that some region needs to be shut down. A back-end designer has been informed that this can be done through placement of switch cells. Assist this designer in carrying out his task by choosing the best method available.

(40 marks)

(c) You are given a task to carry out the final routing for a design. You have to keep in mind that you need to make sure that your design is DRC clean. First of all what do you understand by DRC and what are the violations that might occur during detailed routing?. Show how you would solve these violations.

(30 marks)

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