UNIVERSITI SAINS MALAYSIA

First Semester Examination
Academic Session of 2006/2007

October/November 2006

EBB 526/3 – Electronic Packaging

Time : 3 hours

Please ensure that this paper consists of EIGHT printed pages before you proceed with the examination.

This paper contains SEVEN questions.

Answer FIVE questions. If a candidate answer more than five questions, only the first five answered will be examined and awarded marks.

Answer to any question must start on a new page.

All questions must be answered in English.

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1. Two of the key processes involved during the front of line assembly are the first level interconnect and the encapsulation. The questions are:

[a] There are 3 main types of the first level interconnects used i.e., Wirebonding, Flip chip and Tab interconnect bonding. Describe (using flow diagram to help if needed) to show ONLY 2 of the 3 types of interconnect assembly flow and show the different issues and challenges that you would expect for the module.

(40 marks)

[b] Encapsulation is typically the next package assembly step required to provide physical protection during handling, shipment and application. Describe the four different encapsulation processes that are typically used for the electronic packaging. Next, identify the issues and challenges that you may expect for ONLY 2 of the 4 different encapsulation processes.

(30 marks)

[c] Define Moore's Law and briefly discuss the impact of Moore's Law to semiconductor packaging.

(30 marks)

2. [a] Now, imagine you are the Director of the package development group for a multi-million dollars silicon chip corporation. You were told there are new Products A and B that require new packaging. Now, identify the best packaging technology that you would recommend for the assembly of the products. Please also explain why you would select the particular package for the different products.

(i) Product A:

I. Die size of 3x3 mm^2 and 3 mils thick

II. Organic substrate size of 5x5 mm^2 and 0.5mm thick

III. Total I/O = 1000

IV. High frequency application = 10 Gigahertz

V. Require second level interconnect using ball attach

(ii) Product B:

I. Die size of 10x10mm and 30 mils thick

II. Organic substrate size of 27 x 27mm^2 and 0.8mm thick

III. Total I/O = 300

IV. Low frequency application <200 MegaHertz

V. Requiring second level interconnect using ball attach

(40 marks)

[b] In real life, electronic components are subjected to electrical, thermal and mechanical stresses. The solder interconnect and wire-bond interconnect must be able to withstand all the stresses during its entire life span. If not properly designed, the solder interconnect may fail due to creep, fatigue or solder joint brittle fracture. Describe what is the conditions for causing fatigue failure and solder creep failure in solder interconnect.

(40 marks)

[c] Discuss similarity and difference of electroless and electrolytic nickel plating.

(20 marks)

3. [a] With aid of sketches, describe the thermal mechanical defects which normally occur in substrate material, and briefly explain the causes of the defects.

(30 marks)

[b] Briefly explain the differences between subtractive patterning and semi-additive patterning.

(30 marks)

[c] Label the construction of organic flip chip substrate shown in Figure 1. Briefly explain (using Flow diagram) the manufacturing process of the substrate.

(40 marks)

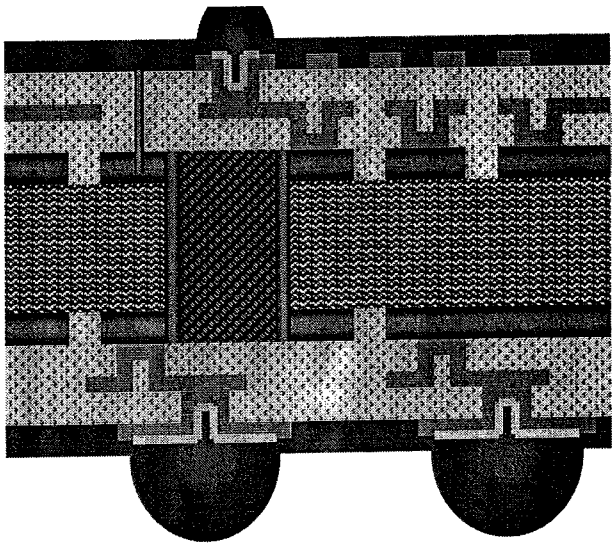

Figure 1: Organic flip chip substrate construction

4. [a] List five (5) types of package that you know (provide with full names).

(10 marks)

[b] Briefly explain 3 packaging classification and give example for each classification.

(45 marks)

[c] Reflow process is one of the important process step in flip chip interconnect packaging technology:

(i) What is the purpose of flip chip wafer reflow process?

(ii) Explain the reflow process method.

(iii) Briefly discuss the issues and challenges in reflow process.

(45 marks)

5. Consider the chip package with heat sink shown in the Figure 3 below. The thermal resistance of the heat sink is obtained from a vendor catalog and is specified as 1.0 K/W. The silicon die is 1cm x 1cm and is 1 mm thick. The overall package size is 2 cm x 2 cm. The package is 5mm thick and the mold material has a thermal conductivity of 0.8 W/mK. The package dissipates 2 W. The thermal interface material is 0.2 mm thick and has a thermal conductivity of 1.5 W/mK. The air gap between the package and printed board is expected to be 0.1 mm thick.

The board has a construction similar to that in Figure 2. Thermal conduction through the leads is assumed to be negligible. Ambient air temperature is 45°C. Compute the value of the die temperature, if the thermal resistance from PWB to the air is known to equal 10 K/W.

(100 marks)

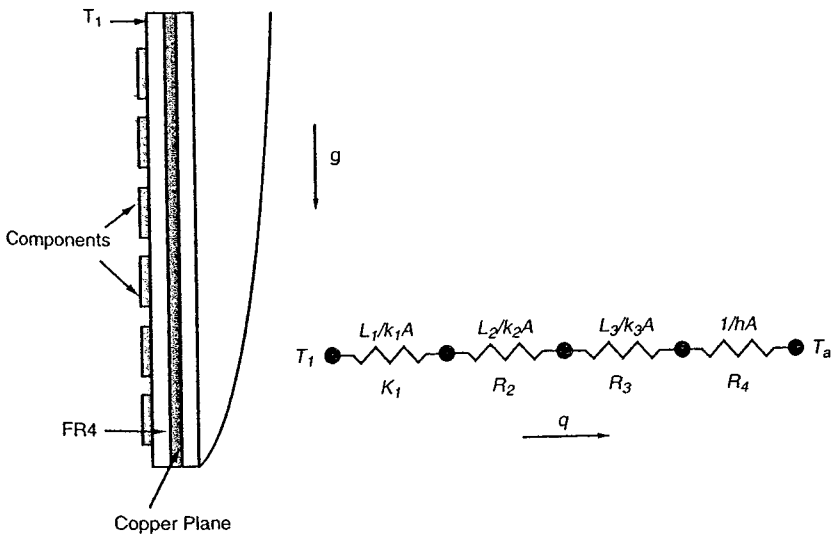

Figure 2

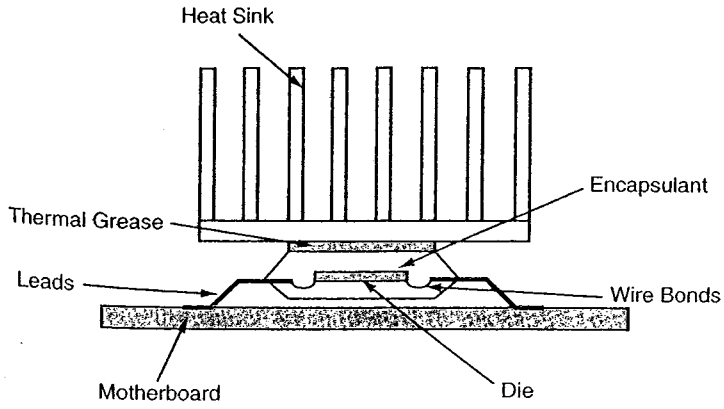

Figure 3

6. [a] What is thermal interface materials (TIM) and its roles? Describe three types of TIM materials and their advantages.

(40 marks)

[b] What is electronic packaging? Briefly describe the functions of electronic packaging in electronic industry.

(15 marks)

[c] What is capillary underfill (CUF), no-flow underfill (NUF) and mould underfill (MUF)? Discuss the effect of filler loading on three (3) properties of underfill.

(45 marks)

7. [a] (i) Draw a curve for a typical product reliability failure pattern.

(10 marks)

(ii) Name the axis correctly.

(5 marks)

(iii) What is the famous name for this curve?

(5 marks)

(iv) Split into 3 sections of failure pattern and name all three sections correctly.

(15 marks)

(v) Describe each of the 3 sections you mentioned in (c).

(15 marks)

[b] (i) With respect to the Differential Scanning Calometry (DSC), gives definitions to the following:

I. Calorimetry

(5 marks)

II. Differential

(5 marks)

III. Scanning

(5 marks)

IV. Exothermic reaction

(5 marks)

V. Endothermic reaction

(5 marks)

(ii) With the aid of diagrams, explains the differences between dilatant, plastic and pseudoplastics fluids.

(25 marks)

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