UNIVERSITI SAINS MALAYSIA

Peperiksaan Semester Kedua
Sidang Akademik 2005/2006

April/Mei 2006

EEE 130 – ELEKTRONIK DIGIT I

Masa : 3 Jam

ARAHAN KEPADA CALON:-

Sila pastikan kertas peperiksaan ini mengandungi **LAPAN BELAS** muka surat termasuk **TIGA** muka surat **Lampiran** bercetak sebelum anda memulakan peperiksaan ini.

Jawab **LIMA** soalan.

Semua soalan hendaklah dijawab dalam Bahasa Malaysia.

...2/-

1. (a) You are required to design a simple automobile warning buzzer. The criterion for the activation of the warning buzzer is as follows:

Anda dikehendaki untuk merekabentuk satu penggera kecemasan kenderaan mudah. Kriteria bagi penggera kecemasan itu berbunyi adalah seperti berikut:

The buzzer activates if the headlights are on and the driver's door is opened, or if the key is in the ignition and the driver's door is opened.

Penggera akan dibunyikan jika lampu dihidupkan dan pintu pemandu dibuka, atau jika kunci dihidupkan dan pintu pemandu dibuka.

(i) Prepare a complete truth table for the burglar alarm system.
Sediakan satu jadual kebenaran yang lengkap untuk sistem penggera kecurian.

(ii) Construct a K-map for the burglar alarm system, complete with groups.
Bina satu peta-K bagi sistem penggera kecurian tersebut, lengkap dengan kumpulan-kumpulannya.

(iii) Write the Boolean equation for the system.
Tulis persamaan Boolean bagi sistem tersebut.

(iv) Draw the system's logic circuit.
Lukis litar logik bagi sistem. (15%)

(b) Using the partial data sheets for a 74HC00A and 74LS00 provided in Appendices A-1 and A-2, determine the following:

Menggunakan helaian data berasingan bagi 74HC00A dan 74LS00 yang disediakan dalam Lampiran A-1 dan A-2, tentukan yang berikut:

...3/-

(i) Maximum LOW level output voltage for a 74HC00A
Voltan keluaran maksimum logik RENDAH bagi satu 74HC00A

(ii) Maximum propagation delay for a 74HC00A
Masa lengah pengoperasian maksimum bagi satu 74HC00A

(iii) Power dissipation at maximum supply voltage and 50% duty cycle for a 74LS00
Kuasa dilesapkan pada voltan bekalan maksimum dan 50% kitar tugas bagi satu 74LS00

(iv) Minimum HIGH level output voltage for a 74LS00
Voltan keluaran minimum logik TINGGI bagi satu 74LS00

(v) Maximum propagation delay for a 74LS00
Masa lengah pengoperasian maksimum bagi satu 74LS00

(5%)

2. (a) Draw the logic circuit of a 4-bit binary number comparator which outputs HIGH if $A_0=B_0$, $A_1=B_1$, $A_2=B_2$, and $A_3=B_3$.

Lukis litar logik bagi satu pembanding nombor perduaan 4-bit di mana keluarannya TINGGI jika $A_0=B_0$, $A_1=B_1$, $A_2=B_2$, dan $A_3=B_3$. (6%)

(b) Determine the voltage level of the output voltage signal of a 74HCT4051 analog multiplexer in Figure 1 when the binary count reaches 110_2.

Tentukan paras voltan bagi isyarat voltan keluaran sebuah pemultipleks analog 74HCT4051 dalam Rajah 1 apabila kiraan perduaan mencapai 110_2.

(1%)

...4/-

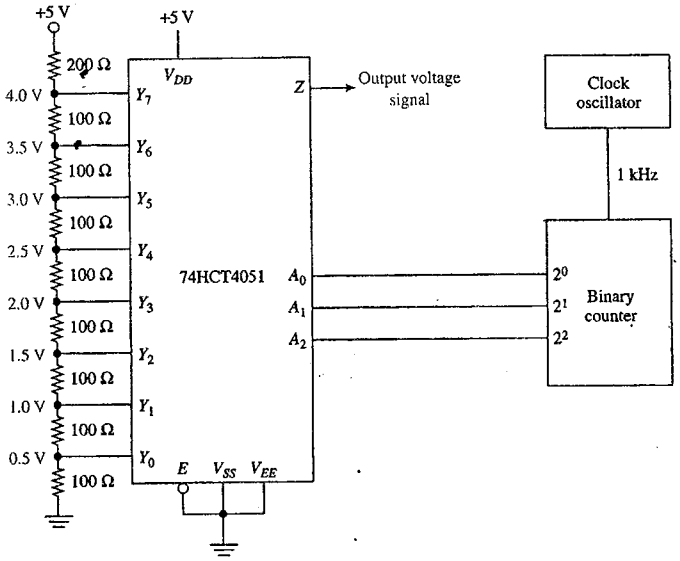


Figure 1
Rajah 1

(c) What are the output levels at $\overline{0}, \overline{1}, \overline{2}$ and $\overline{3}$ of the 74139 demultiplexer in Figure 2 when the circuit is displaying the number 3_{10} in the Least Significant Digit (LSD) of the 7-segment display?

Apakah paras-paras keluaran pada $\overline{0}, \overline{1}, \overline{2}$ dan $\overline{3}$ bagi demultipleks 74139 dalam Rajah 2 apabila litar tersebut memaparkan nombor 3_{10} dalam LSD pada sebuah pemapar 7-temberang garis?

(2%)

...5/-

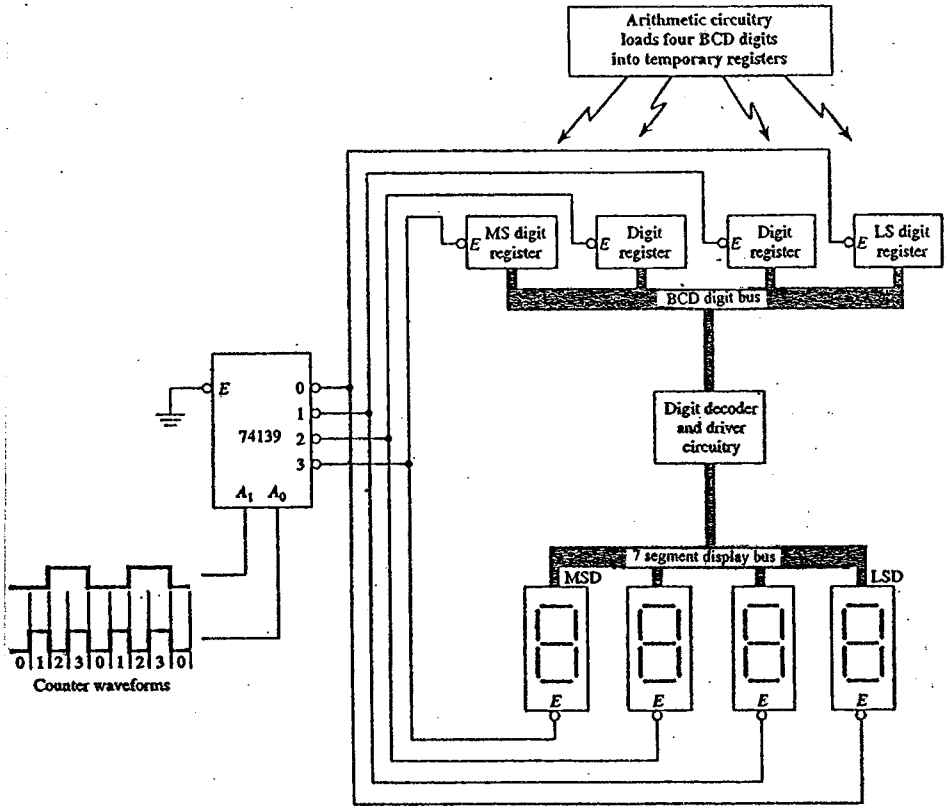


Figure 2
Rajah 2

(d) There is a malfunction in a digital system that contains several multiplexer and demultiplexer ICs. A reading was taken at each pin with a logic probe, and the results were recorded in Table 1. By referring to the IC pin configuration given in Appendix B, comment on each IC, indicating whether or not there is a malfunction. If there is, indicate on which pin and briefly explain what the problem is.

Terdapat satu kerosakan pada sebuah sistem digit yang mengandungi beberapa litar bersepadu pemultipleks dan demultipleks. Satu bacaan telah diambil pada setiap pin menggunakan prob logik, dan keputusannya direkodkan dalam Jadual 1. Dengan merujuk kepada konfigurasi pin litar bersepadu yang diberikan dalam Lampiran B, berikan ulasan bagi setiap litar bersepadu, tunjukkan samada ia berfungsi atau rosak. Jika terdapat kerosakan, nyatakan pin tersebut dan terangkan secara ringkas tentang permasalahannya. (4%)

...6/-

74150		74151		74139		74154	
Pin	Level	Pin	Level	Pin	Level	Pin	Level
1	0	1	1	1	0	1	1
2	1	2	0	2	1	1	1
3	1	3	0	3	0	3	1
4	0	4	1	4	0	4	1
5	1	5	1	5	1	5	1
6	0	6	0	6	1	6	1
7	1	7	0	7	1	7	1
8	1	8	0	8	0	8	1
9	0	9	0	9	0	9	1
10	0	10	0	10	0	10	1
11	0	11	0	11	1	11	1
12	0	12	0	12	0	12	0
13	1	13	1	13	1	13	1
14	1	14	0	14	0	14	1
15	1	15	0	15	1	15	1
16	0	16	1	16	1	16	1
17	1					17	1
18	0					18	1
19	1					19	0
20	1					20	0
21	1					21	0
22	0					22	1
23	1					23	1
24	1					24	1

Table 1: IC logic states at troubleshooting

(e) Sketch the output waveform of the 74138 in Figure 3a. The input waveforms to the 74138 are given in Figure 3b.

Lakarkan gelombang keluaran bagi 74138 dalam Rajah 3a. Gelombang masukan bagi 74138 diberikan dalam Rajah 3b.

(7%)

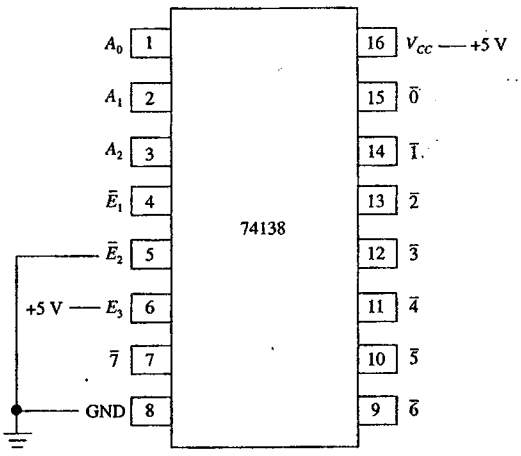


Figure 3a
Rajah 3a

...7/-

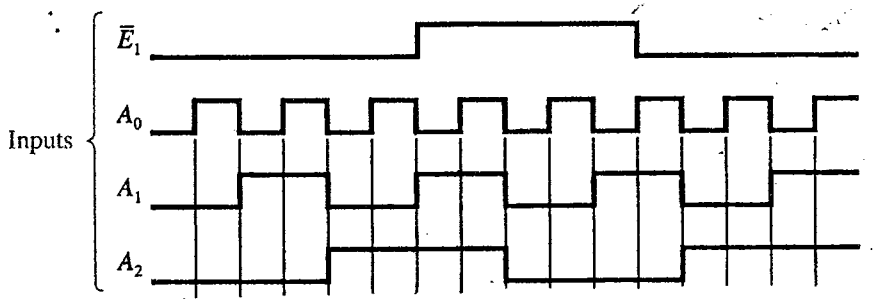


Figure 3b
Rajah 3b

3. (a) What hex number will be read by port 1 of the 8051 microcontroller in Figure 4 if the fluid level is high in the following chemical tanks?

Apakah nombor per-enambelasan yang akan dibaca oleh pin 1 pengawalmikro 8051 dalam Rajah 4 jika paras larutan adalah tinggi dalam tangki-tangki kimia berikut?

(5%)

(i) Tank 1
Tangki 1

(ii) Tank 6
Tangki 6

(iii) Tanks 2 and 7
Tangki 2 dan 7

(iv) All tanks
Kesemua tangki

(v) No tanks
Tanpa tangki

...8/-

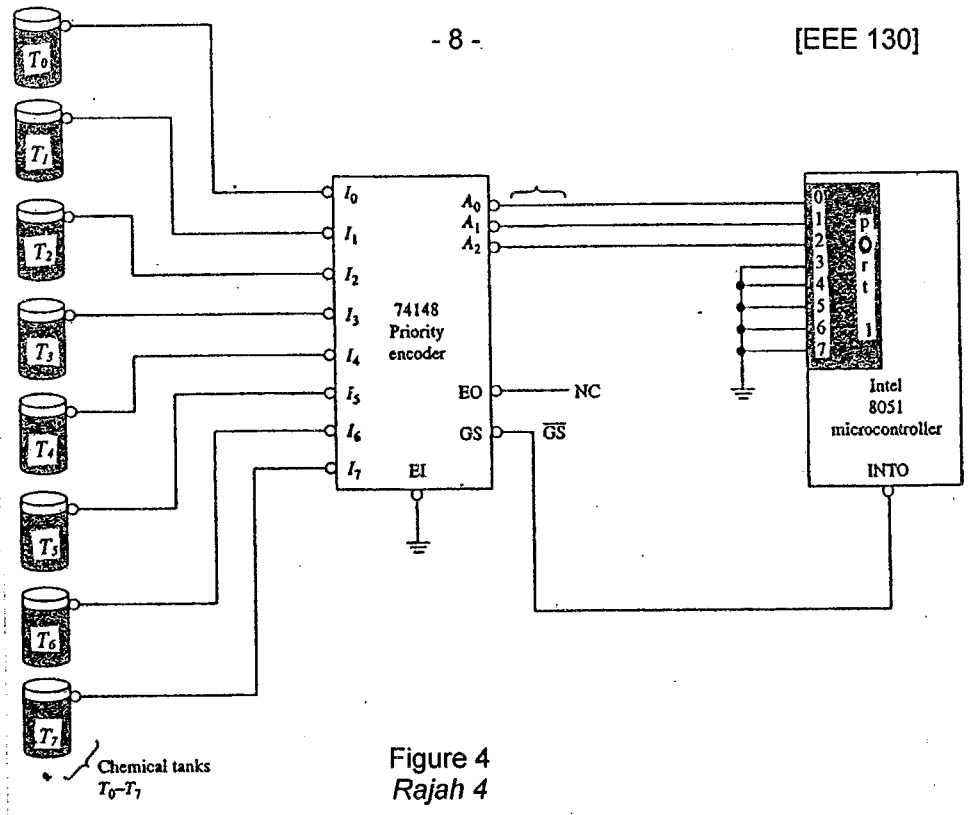


Figure 4
Rajah 4

(b) How is the microcontroller in Figure 4 notified of a high fluid level at one of the chemical tanks?

Bagaimanakah pengawalmikro dalam Rajah 4 mengenalpasti paras larutan tinggi pada salah satu daripada tangki-tangki kimia tersebut?

(1%)

(c) The 74147 shown in Figure 5a is set-up for encoding just three of its inputs (7, 8 and 9). Using the function table from Figure 5b, sketch the outputs at $\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$ and $\overline{A}_3$ as the $\overline{I}_7$, $\overline{I}_8$, and $\overline{I}_9$ inputs are switching as shown in Figure 5c.

74147 yang ditunjukkan dalam Rajah 5a telah disetkan untuk tujuan pengekodan hanya 3 daripada masukan-masukannya (7, 8 dan 9). Menggunakan jadual fungsi daripada Rajah 5b, lakarkan keluaran-keluaran pada $\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$ dan $\overline{A}_3$ jika masukan $\overline{I}_7$, $\overline{I}_8$, dan $\overline{I}_9$ adalah pensuisan seperti dalam Rajah 5c.

(4%)

...9/-

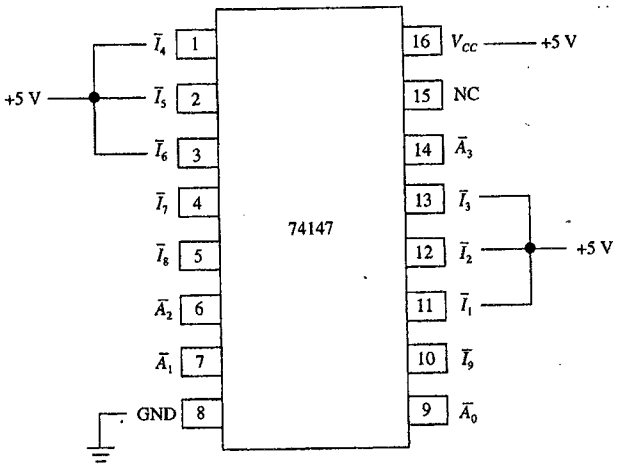


Figure 5a
Rajah 5a

Input									Output			
$\bar{I}_1$	$\bar{I}_2$	$\bar{I}_3$	$\bar{I}_4$	$\bar{I}_5$	$\bar{I}_6$	$\bar{I}_7$	$\bar{I}_8$	$\bar{I}_9$	$\bar{A}_3$	$\bar{A}_2$	$\bar{A}_1$	$\bar{A}_0$
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

Figure 5b
Rajah 5b

...10/-

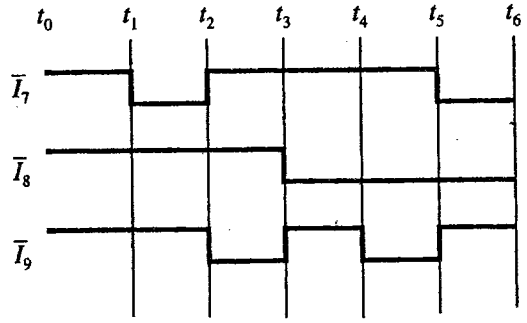


Figure 5c
Rajah 5c

(d) The connections shown in Figure 6 are made to the 74151 8-line multiplexer. Determine *Y* and $\overline{Y}$.

Sambungan seperti Rajah 6 telah dibuat kepada pemultipleks 8-talian 74151. Tentukan Y dan $\overline{Y}$.

(10%)

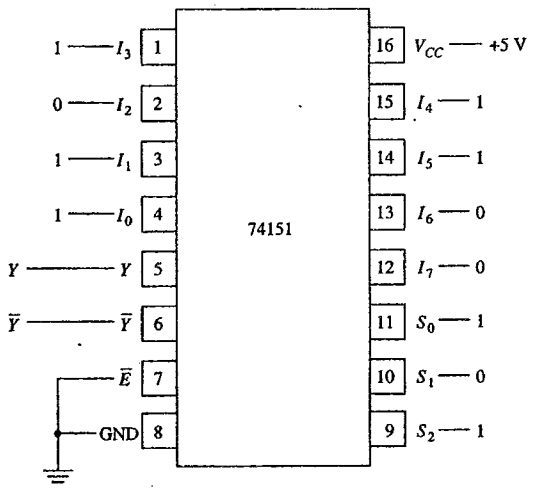


Figure 6
Rajah 6

...11/-

4. (a) Determine the MOD number of the counter in Figure 7. Also determine the frequency at the D output.

Tentukan nombor mod bagi pembilang yang ditunjukkan dalam Rajah 7. Apakah frekuensi pada keluaran D.

(5%)

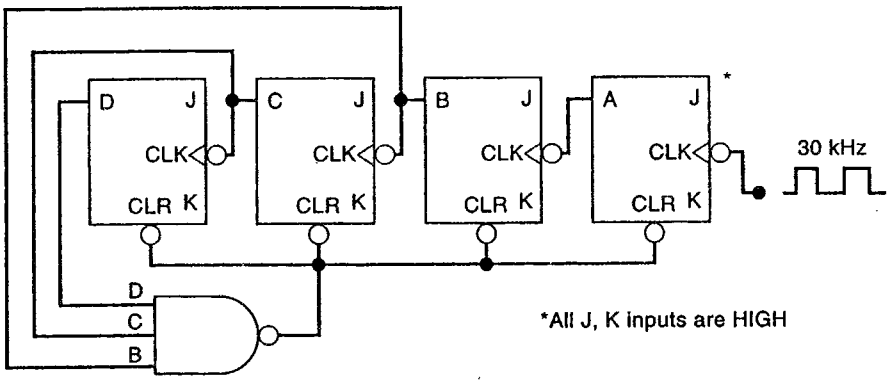


Figure 7
Rajah 7

(b) Determine the sequence of 8 bits Johnson counter. State the application of Johnson counter.

Tentukan jujukan bagi pembilang segerak Johnson 8 bit. Nyatakan kegunaan pembilang Johnson.

(5%)

...12/-

(c) Stepper motor is controlled by 4 coils, coil 1, coil 2, coil 3 and coil 4 as shown in Figure 8. Coil 1 and coil 2 must always be in opposite states, that is when coil 1 is energized, coil 2 is not and vice versa. Likewise, coil 3 and 4 must always be in opposite states. The current amplifiers are needed because the flip-flop output cannot supply the amount of current that the coils require. Stepper motor can rotate either in clockwise or counter clockwise depends on direction input D. If D =0 is for clockwise rotation and D=1 is for counter clockwise rotation, design a circuit to drive the stepper motor using JK flip-flop. Include the state diagram, excitation table, Karnaugh map and block diagram.

Stepper motor dikawal oleh 4 gegelung, gegelung 1, gegelung 2, gegelung 3 dan gegelung 4 seperti yang ditunjukkan dalam Rajah 8. Gegelung 1 dan 2 mesti dalam keadaan berbeza yang mana apabila gegelung 1 diaruhkan, gegelung 2 tidak diaruhkan dan sebaliknya. Begitu juga dengan gegelung 3 dan 4. Stepper motor boleh bergerak samada mengikut arah jam atau melawan arah jam bergantung kepada masukan D yang diberikan. Penguat arus diperlukan kerana arus daripada flip-flop tidak mencukupi untuk memicu gegelung tersebut. Dengan menganggap jika D=0 untuk pusingan mengikut arah jam dan D =1 untuk pusingan melawan arah jam, rekabentuk satu litar dengan menggunakan flip-flop J-K untuk memicu motor tersebut. Gambarajah keadaan, jadual rangsangan, peta Karnaugh dan gambarajah litar perlu diberikan.

(10%)

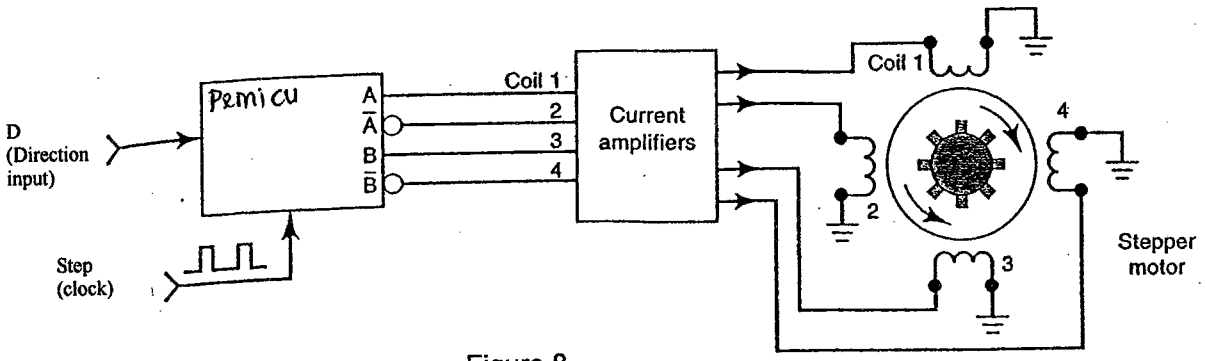


Figure 8
Rajah 8

...13/-

5. (a) Design a counter to produce a sequence as shown in Figure 9.

Rekabentuk pembilang yang menghasilkan jujukan seperti dalam Rajah 9.

(5%)

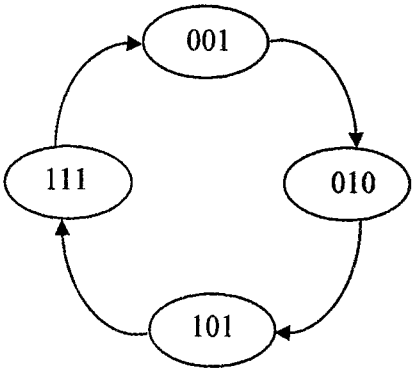


Figure 9
Rajah 9

(b) Determine the Q waveform if the signals in Figure 10 are applied to the inputs of the JK flip-flop.

Dapatkan bentuk gelombang Q apabila isyarat dalam Rajah 10 diberikan kepada masukan flip-flop JK .

(5%)

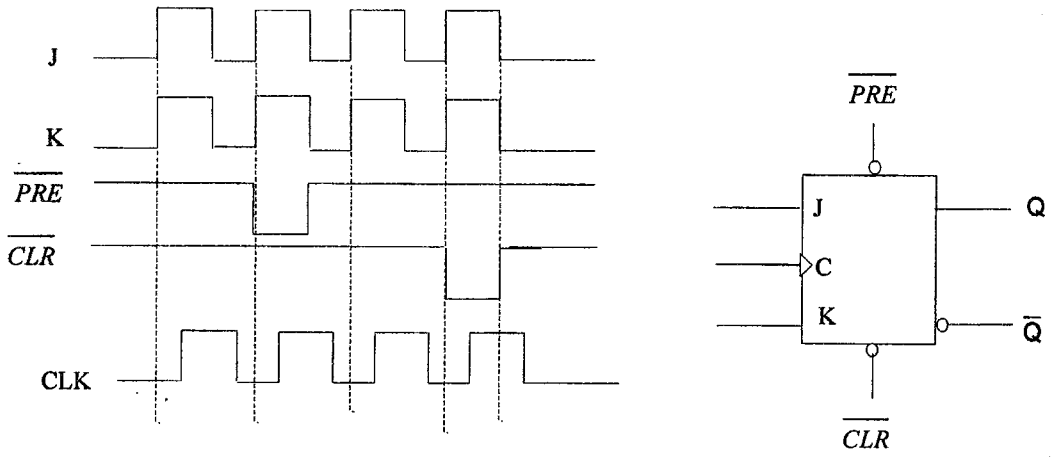


Figure 10
Rajah 10

...14/-

(c) Define four states to model a serial binary adder as a Moore network. Based on the states construct a state diagram and state table.

Nyatakan empat keadaan untuk memodelkan penambah binari sesiri sebagai rangkaian Moore. Daripada keadaan tersebut, bina gambarajah keadaan dan jadual keadaan.

(10%)

6. (a) Determine the states of shift register shown in Figure 11 for the given Right/Left signal. Assume that Q0=1, Q1=0, Q2=0 and Q3=1. Input at serial input pin is logic 0.

Tentukan keadaan bagi daftar anjak dalam Rajah 11 bagi isyarat Right/Left yang diberikan. Andaikan ~Q0=1, Q1=0, Q2=0 dan Q3=1. Masukan pada pin masukan sesiri adalah logik 0.

(5%)

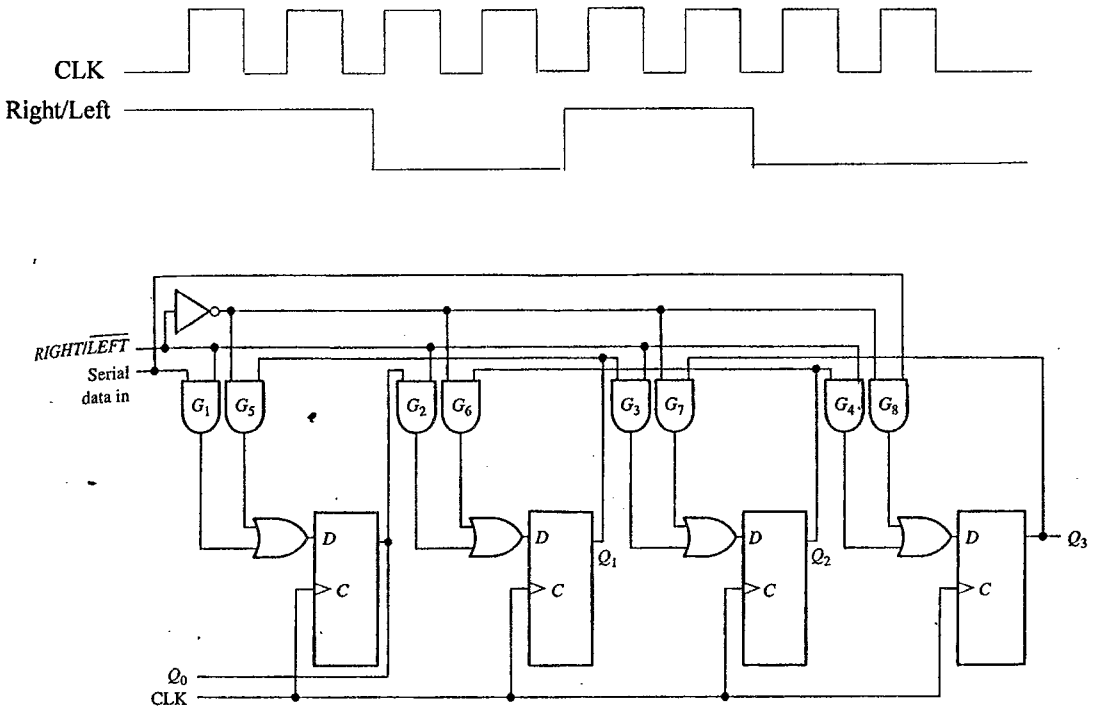


Figure 11
Rajah 11

...15/-

(b) Determine the Q and $\overline{Q}$ output, for the SR flip flop as shown in Figure 12.

Tentukan keluaran pada Q dan $\overline{Q}$ bagi flip flop SR seperti yang ditunjukkan dalam Rajah 12.

(5%)

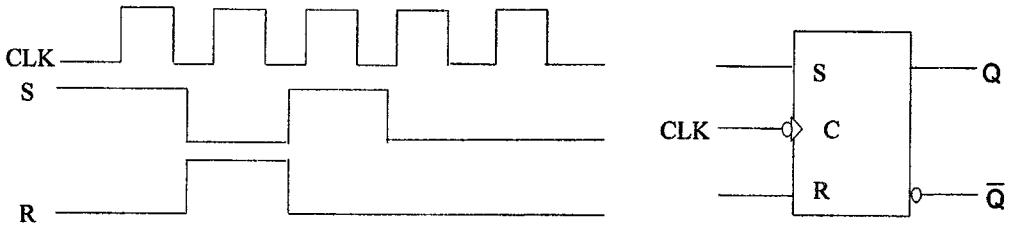


Figure 12
Rajah 12

(c) For the asynchronous sequential network in Figure 13 construct the excitation table, transition table, state table, flow table and flow diagram.

Untuk rangkaian jujukan tak segerak seperti yang ditunjukkan dalam Rajah 13, bina jadual rangsangan, jadual peralihan, jadual keadaan, jadual alir dan rajah alir.

(10%)

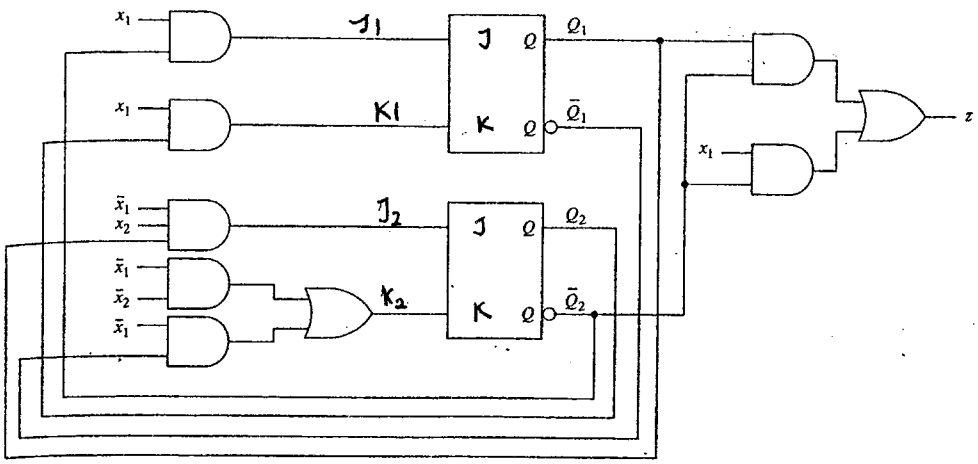


Figure 13
Rajah 13

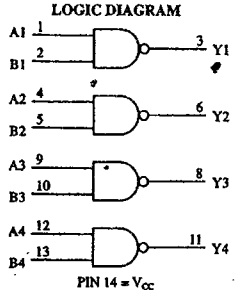
oooOooo

Quad 2-Input NAND Gate High-Performance Silicon–Gate CMOS

The MC54/74HC00A is identical in pinout to the LS00. The device inputs are compatible with Standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

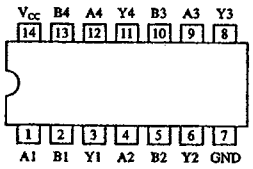
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7A Requirements
- Chip Complexity: 32 FETs or 8 Equivalent Gates

LOGIC DIAGRAM



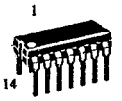
PIN 14 = V_{CC}
PIN 7 = GND

Pinout: 14–Load Packages (Top View)



MC54/74HC00A

J SUFFIX
CERAMIC PACKAGE
CASE 632-08



N SUFFIX
PLASTIC PACKAGE
CASE 646-06

D SUFFIX
SOIC PACKAGE
CASE 751A-03

DT SUFFIX
TSSOP PACKAGE
CASE 948G-01

ORDERING INFORMATION

MC54HCXXAJ	Ceramic
MC74HCXXAN	Plastic
MC74HCXXAD	SOIC
MC74HCXXADT	TSSOP

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
	TSSOP Package†	450	
T_{stg}	Storage Temperature	−65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		°C
	Plastic DIP, SOIC or TSSOP Package	260	
	Ceramic DIP	300	

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: – 10 mW/°C from 65° to 125° C
Ceramic DIP: – 10 mW/°C from 100° to 125° C
SOIC Package: – 7 mW/°C from 65° to 125° C
TSSOP Package: – 6.1 mW/°C from 65° to 125° C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		−55	+125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0 V	0	1000	ns
		V_{CC} = 4.5 V	0	500	
		V_{CC} = 6.0 V	0	400	

DC CHARACTERISTICS (Voltages Referenced to GND) MC54/74HC00A

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit −55 to 25°C	≤85°C	≤125°C	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out} = 0.1V or V_{CC} − 0.1V $\lvert I_{out}\rvert \le 20\mu A$	2.0	1.50	1.50	1.50	V
			3.0	2.10	2.10	2.10	
			4.5	3.15	3.15	3.15	
			6.0	4.20	4.20	4.20	
V_{IL}	Maximum Low-Level Input Voltage	V_{out} = 0.1V or V_{CC} − 0.1V $\lvert I_{out}\rvert \le 20\mu A$	2.0	0.50	0.50	0.50	V
			3.0	0.90	0.90	0.90	
			4.5	1.35	1.35	1.35	
			6.0	1.80	1.80	1.80	
V_{OH}	Minimum High-Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\lvert I_{out}\rvert \le 20\mu A$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V_{in} = V_{IH} or V_{IL} $\lvert I_{out}\rvert \le 2.4mA$	3.0	2.48	2.34	2.20	
		$\lvert I_{out}\rvert \le 4.0mA$	4.5	3.98	3.84	3.70	
		$\lvert I_{out}\rvert \le 5.2mA$	6.0	5.48	5.34	5.20	
V_{OL}	Maximum Low-Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\lvert I_{out}\rvert \le 20\mu A$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V_{in} = V_{IH} or V_{IL} $\lvert I_{out}\rvert \le 2.4mA$	3.0	0.26	0.33	0.40	
		$\lvert I_{out}\rvert \le 4.0mA$	4.5	0.26	0.33	0.40	
		$\lvert I_{out}\rvert \le 5.2mA$	6.0	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0μA	6.0	1.0	10	40	μA

AC CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit −55 to 25°C	≤85°C	≤125°C	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y	2.0	75	95	110	ns
		3.0	30	40	55	
		4.5	15	19	22	
		6.0	13	16	19	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	16	19	
C_{in}	Maximum Input Capacitance		10	10	10	pF

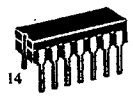
C_{PD}	Power Dissipation Capacitance (Per Buffer)	Typical @ 25°C, V_{CC} = 5.0 V, V_{EE} = 0 V	pF
		22	

QUAD 2-INPUT NAND GATE

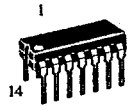
• ESD > 3500 Volts

SN54/74LS00

QUAD 2-INPUT NAND GATE
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08

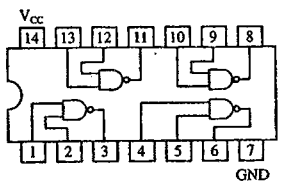


N SUFFIX
PLASTIC
CASE 646-06

D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC



SN54/74LS00

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Ouput HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.5		V	
V_{OL}	Ouput LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, I_N = 0.4 V
I_{OS}	Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX
I_{CC}	Power Supply Current Total, Output HIGH				1.6	mA	V_{CC} = MAX
	Total, Output LOW				4.4		

NOTE 1: Not more than one output should be shorted at a time, nor for more than 1 second.

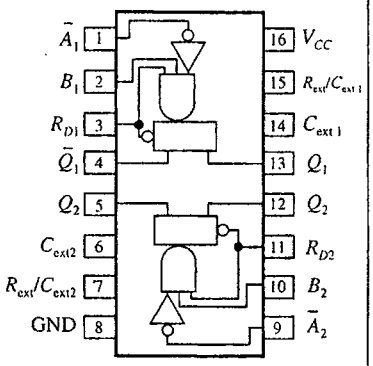
AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
t_{PLH}	Turn-Off Delay, Input to Output		9.0	15	ns	V_{CC} = 5.0 V; C_L = 15 pF
t_{PHL}	Turn-On Delay, Input to Output		10	15	ns	

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

74123



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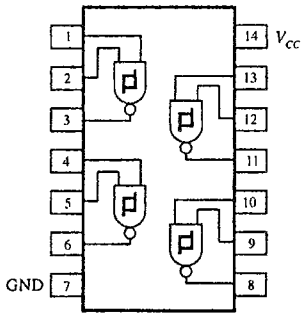

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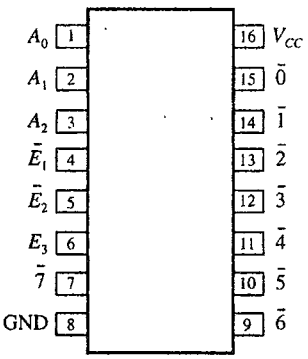

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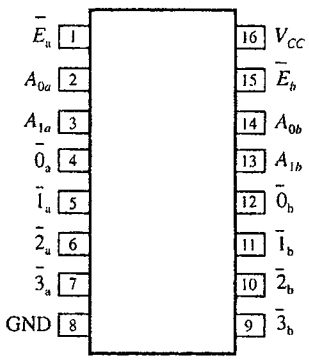

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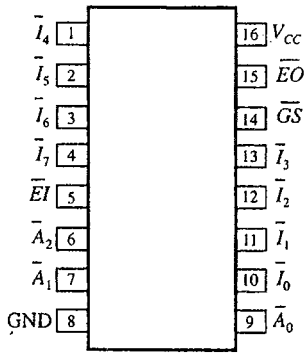

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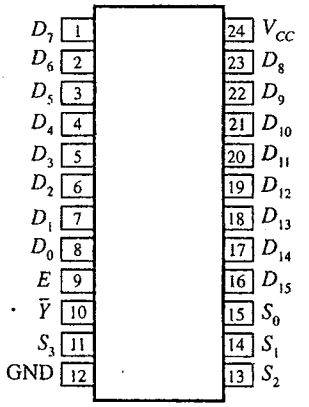

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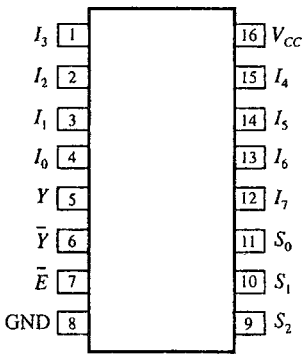

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