A DISCRETE DISTRIBUTED POWER AMPLIFIER FOR VHF TO UHF

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A DISCRETE DISTRIBUTED POWER AMPLIFIER FOR VHF TO UHF

by

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[1] Tan Teik Siew, Mohd Fadzil bin Ain and Syed Idris Syed Hassan. (2005). 100MHz-500MHz, 1 watt distributed power amplifier with discrete MOSFET devices. Asia-Pacific Conference On Applied Electromagnetic Proceedings, Johor Bahru, Johor, Malaysia.

[2] Tan Teik Siew, Mohd Fadzil bin Ain and Syed Idris Syed Hassan. (2006). 100MHz-650MHz, 1 Watt Distributed Power Amplifier with Discrete MOSFET devices. TENCON2006, Hong Kong.

[3] Tan Teik Siew, Mohd Fadzil bin Ain and Syed Idris Syed Hassan. (2006). Large signal design of distributed power amplifier with discrete RF MOSFET devices. International RF and Microwave Conference Proceedings, Putrajaya, Malaysia.

PENGUAT KUASA TERAGIH DISKRET UNTUK VHF KE UHF

ABSTRAK

Penguat kuasa yang mempunyai lebar-jalur yang lebar adalah komponen utama dalam teknologi Radio Tertakrif Perisian. Namun demikian, penguat kuasa jalurlebar lazim mempunyai lebarjalur yang kurang kerana dihadkan oleh hasil gandaan-lebarjalur transistor. Untuk mengatasi masalah hasil gandaan-lebarjalur, penguat teragih sering digunakan dengan menggabungkan keluaran dari beberapa elemen gandaan aktif secara penambahan. Bagaimanapun, penguat teragih lazim mempunyai kuasa dan kecekapan yang kurang disebabkan oleh pembalikan gelombang dari salur. Untuk mendapatkan kecekapan dan kuasa bagi penggunaan jalur lebar, penguat kuasa teragih tirus telah direkabentuk, secara teorinya penguat ini menumpukan semua kuasa kepada beban keluaran. Penguatkuasa teragih tirus menggunakan peranti diskret frekuensi radio MOSFET RD01MUS1 dari Mitsubishi telah difabrikasi dan memberikan kuasa keluaran 1 Watt dengan gandaan 13 dB dan kecekapan tambahan kuasa sebanyak 25 % bagi julat 100 MHz ke 600 MHz. Lebarjalur yang lebih lebar (500 MHz) untuk penguat kuasa teragih tirus adalah amat baik berbanding penguat kuasa jalurlebar lazim yang mempunyai lebarjalur hanya 180 MHz.

A DISCRETE DISTRIBUTED POWER AMPLIFIER FOR VHF TO UHF

ABSTRACT

Wide bandwidth power amplifiers are key components in Software-Defined Radio technology. However, the conventional broadband power amplifier has poor bandwidth that limited by the transistor's gain-bandwidth product. To overcome the conventional gain-bandwidth tradeoff, distributed amplifier topology is often used by combining the outputs from several active gain elements in an additive fashion. However, the conventional distributed amplifier has poor power and efficiency due to the drain line reverse wave. To obtain efficiency and power with wideband application, a tapered distributed power amplifier has been developed, where in theoretically it forces all the power to deliver to the output load. A tapered distributed power amplifier using discrete RF MOSFET devices, RD01MUS1 from Mitsubishi was fabricated and achieved 1 Watt output power with 13 dB associated gain with 25 % of power added efficiency (PAE) over 100 MHz to 600 MHz. This relatively wide bandwidth (500 MHz) performance for tapered distributed power amplifier is better than conventional broadband power amplifier with bandwidth of only 180 MHz.

CHAPTER 1
INTRODUCTION

1.0 Background

In today's environment, two-way radio is usually designed for a single frequency band. In the U.S, the rural police and urban police operate at different radio frequencies, for example 150 MHz and 450 MHz respectively. In an emergency situation, the two departments cannot communicate effectively. Software Defined Radio (SDR) technology (Burns, P., 2002) promises to alleviate this problem. The SDR technology enables seamless communication for different modulation format and multiple frequency bands. It enables customers to improve the coverage and seamless mobility among different users.

In order to realize the SDR technology, wideband power amplifies are one of the most critical building blocks on the transmitter for two-way radio. Over the last decade, a demand has been continually increasing for high power amplifier over a very wideband operating frequencies. The distributed power amplifier is known to be a good candidate for broadband power amplifier design.

1.1 Objective

The main objectives of this thesis are listed here:

- A detail methodology for the design of conventional broadband power amplifier.
- Detailed analysis of the design of a wideband distributed power amplifier using tapered drain line impedance technique.

- Board fabrication and measurement of these two types of power amplifier using Mitsubishi RF MOSFET, RD01MUS1 and compared their performance in terms of bandwidth and efficiency.

1.2 Thesis Outline

Chapter 2 is the literature review. It describes previous related work by other researchers. Included is a review of work on the conventional broadband amplifiers that have relevance to our research.

Chapter 3 discusses the methodology for conventional broadband power amplifier and tapered distributed power amplifier design, as well as briefly explains the measurement setup used to measure the performance of power amplifier.

Chapter 4 explains the bandwidth limitation of the conventional power amplifier and demonstrates a design and fabrication of broadband conventional power amplifier.

Chapter 5 contains the principle of distributed amplifier design for small signal application followed by the method to enhance the output power and efficiency performance for large signal application using tapered drain line impedance technique. It also explains in detail the design and fabrication of such distributed power amplifier.

Lastly, Chapter 6 presents the conclusions and future works from this thesis.

CHAPTER 2
LITERATURE REVIEW

2.0 Introduction

Power amplifiers (PA) are essential in any communication transmitter, as they are used to amplify a signal to the desired power level for delivery to a load. While the absolute power necessary is highly application dependent, the concept, as illustrated in Figure 2.1, is always the same: a PA must deliver enough power so that the signal, after path loss, can still be detected by a receiver. For satellite applications, this may require thousands of watts, while for an indoor personal area network (PAN), it may be as small as several miliwatts.

In this chapter, the power amplifier theory is described. The first section is about operation classes of amplifiers. The second describes the typical characteristic for a power amplifier, such as output power, gain, efficiency, linearity and stability. The last section examines conventional amplifier topologies in literature and evaluates their performance in terms of the bandwidth, output power and efficiencies they can achieve. This will provide sufficient motivation to explore alternate topologies to obtain high power over broad bandwidth with high efficiency.

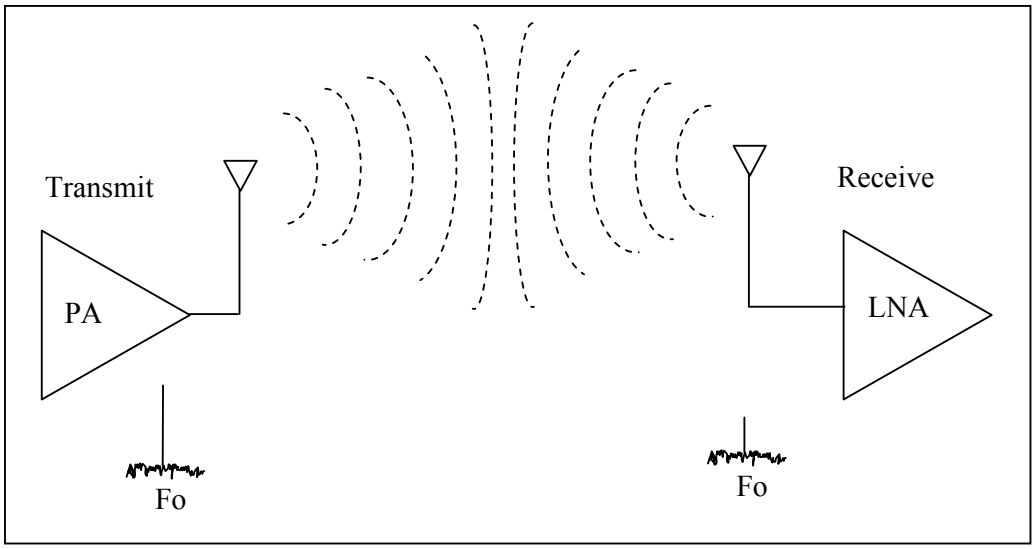

Figure 2.1: Conceptual drawing of generic wireless communication system.

2.1 Generic Power Amplifier

Figure 2.2 illustrates a generic power amplifier at RF frequencies. While the active device shown is an NMOS transistor, it can be replaced by any active device capable of power amplification, such as a vacuum tube or BJT transistor without loss of generality. The drain of the transistor is connected to the supply voltage V_{DD} through an inductor and to the output node V_{out} through a DC blocking capacitor, C_{block} and a matching/filtering network. The inductor, usually of large value and referred to as a radio-frequency choke (RFC) enables the drain of the transistor to be biased at V_{DD} (since an ideal inductor has zero DC impedance), while allowing the drain to swing from 0 V to $2V_{DD}$ at RF frequencies for a 50 % duty cycle. C_{block} isolates the DC level of the drain (V_{DD}) from that of the output node, which is usually 0 V. Z_L models the load impedance.

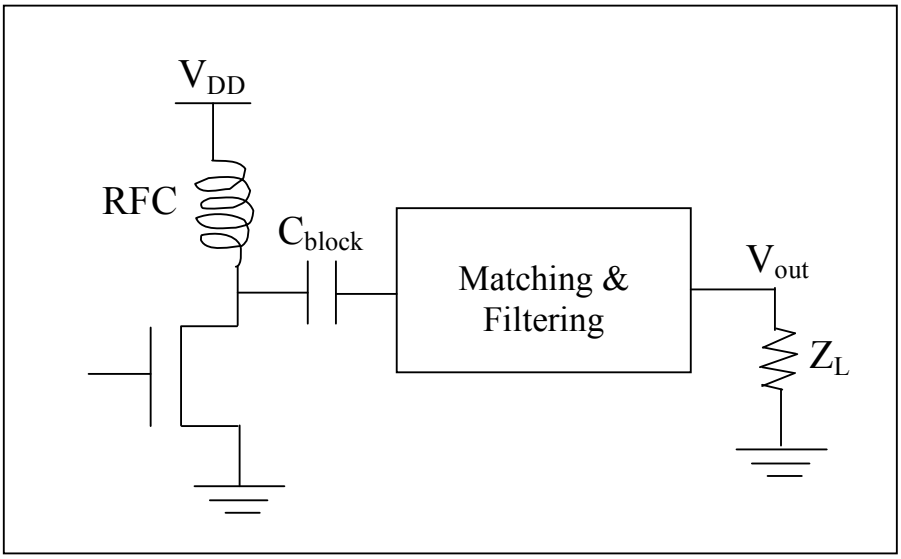

Figure 2.2: Diagram of a generic power amplifier.

2.2 Class of Amplifiers

Choosing a bias point of an RF PA can determine the level of performance ultimately possible with that PA. In certain applications, it maybe desirable to have the transistor conducting for only a certain portion of the input signal. The portion of the input RF signal for which there is an output current determines the class of operation of a PA. The comparison of PA bias approaches evaluate the trade-off for: Output power, efficiency, linearity or other parameters for different applications (Razavi, B., 1998).

In order to operate a transistor for a certain class, the gate and drain DC voltages have to be biased carefully to the certain operation point (quiescent point or q-point). The reason is that the choice of q-point greatly influences linearity, power handling and efficiency (Doudorov, G., 2003). Figure 2.3 shows the typical classes based on the transistor transfer characteristics.

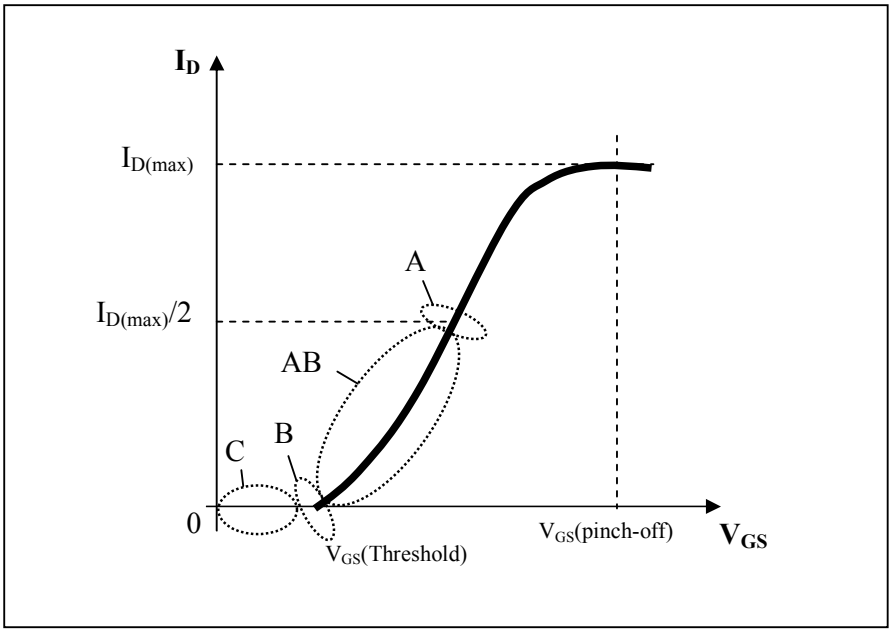

Figure 2.3: Classes of power amplifiers (Doudorov, G., 2003).

2.2.1 Class A

Class A is the simplest power amplifier type in terms of design and construction. Class A amplifier is biased in the center of the load line as shown in Figure 2.4 such that the variations in input signal occur within the limits of cutoff and saturation to allow for maximum voltage and current swing. Hence, it has a conduction angle of 360 degree and provides the maximum linearity in comparison to any other class of operation. However, the problem with Class A amplifiers is their very poor efficiency because the transistor conducting current at all times which translates to higher power loss. Theoretically, the maximum efficiency achievable from a Class A power amplifier is only 50 % and the actual efficiency is typically much less (Gonzalez, G., 1984).

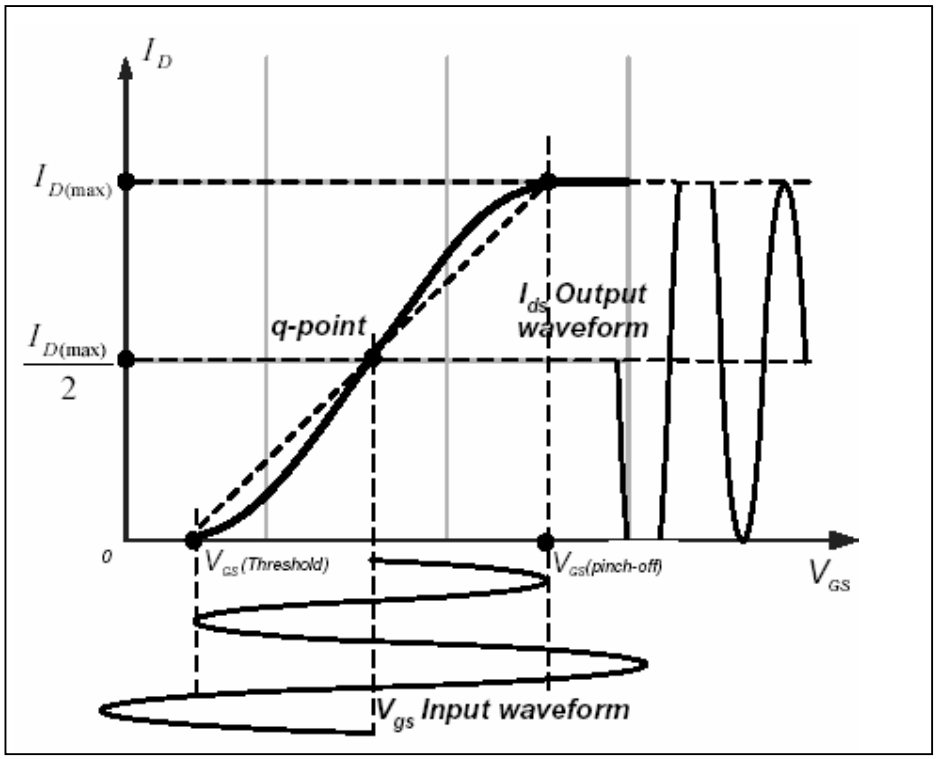

Figure 2.4: Class A transfer characteristic (Doudorov, G., 2003).

2.2.2 Class B

For a class B amplifier, the transistor is biased at its threshold voltage as depicted in Figure 2.5. Hence, there is a current flowing at the output of the transistor only when there is a signal at the input. Moreover, the transistor would conduct current only when the input signal level is greater than the threshold voltage. This occurs for the positive half cycle of the input signal and remains turned off during the negative half cycle. Hence, the conduction angle for Class B operation is 180 degree. By doing this, theoretically it can achieve maximum power efficiency of about 78 %. Although this architecture greatly improves the efficiency, it is normally used in applications with less stringent linearity requirements (Hella, M.M, et al., 2002).

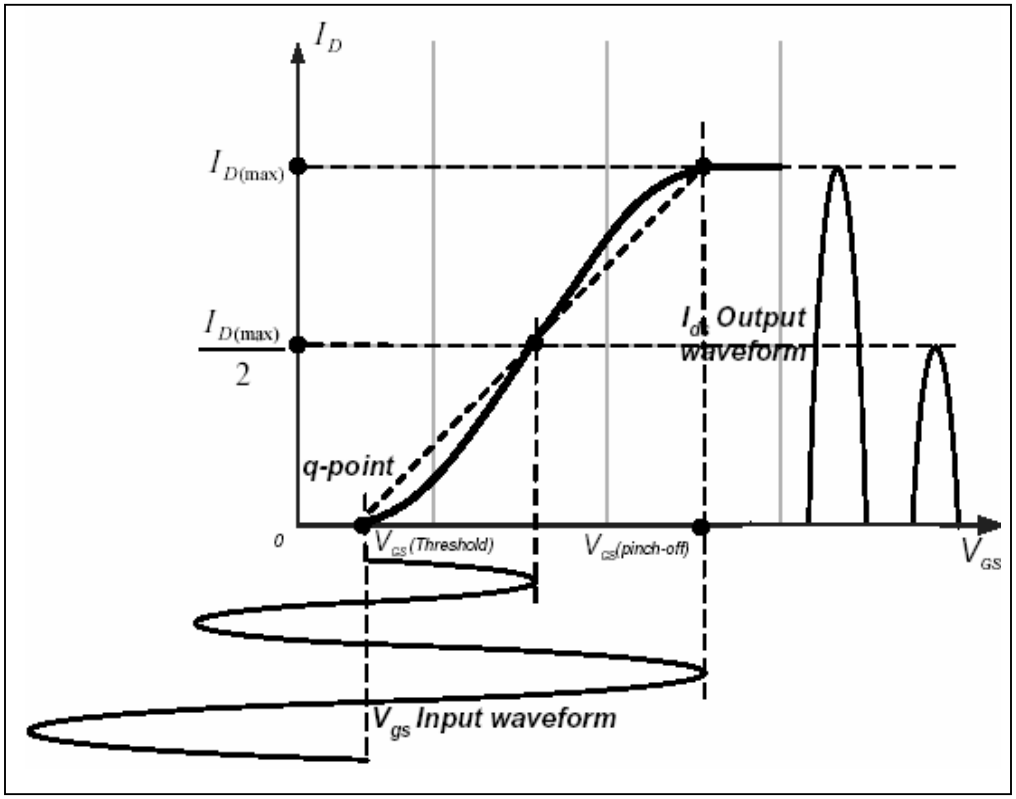

Figure 2.5: Class B transfer characteristic (Doudorov, G., 2003).

2.2.3 Class AB

Class A and Class B power amplifiers have conduction angles of 360 degree and 180 degree, respectively. As the name imply, Class AB amplifiers have a conduction angle between 180 degree and 360 degree, and therefore have properties intermediate between Class A and Class B, including efficiency ranging between 50 % and 78 %. Many find the Class AB amplifier to be a good compromise between the linearity and efficiency (Hella, M.M, et al., 2002).

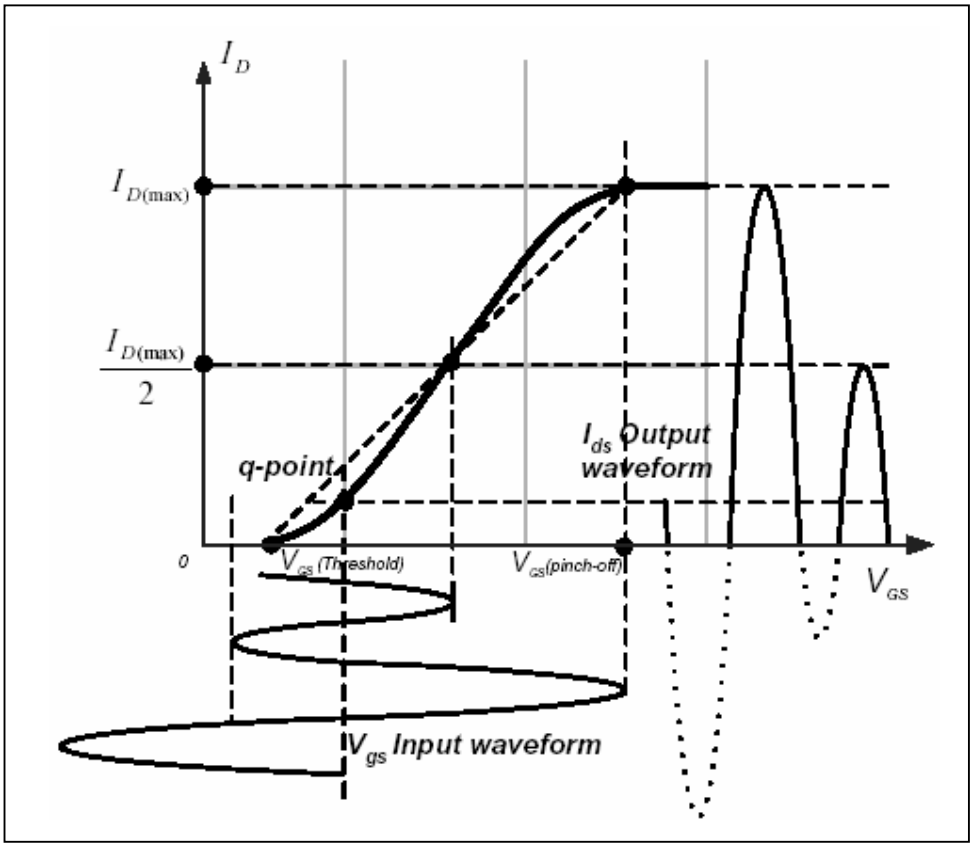

Figure 2.6: Class AB transfer characteristic (Doudorov, G., 2003).

2.2.4 Class C

Class C amplifiers are almost similar to the class B amplifiers with the device biased deep into the cut-off region, so that the conduction angle for a sinusoidal waveform is less than 180 degree. Higher efficiencies are obtained by lowering the conduction angle, up to a theoretical limit of 100 % with 0 degree conduction angle, which means that no signal is applied and this condition is of no interest. However, Class C amplifiers have poor linearity compared to the previous amplifier classes (Hella, M.M, et al., 2002).

Table 2.1 brings together comparisons for different classes of PA.

Table 2.1: Classes of operation PA.

Class	Conduction angle, degree	Max efficiency, %
A	360	50
B	180	78
AB	180-360	50-78
C	0-180	Approaches to 100

2.2.5 Other High Efficiency Classes

There are other high efficiency classes of operation such as Class D, E and F. These classes of operation are more suited for application using constant envelope modulation technique with linearity being a less stringent requirement. Class D, E and F are switched mode power amplifiers, where the device is operated as a switch. These classes use a resonator at the output to obtain the fundamental power and are of no significance in broadband amplifiers. In addition, their description can be found in (Hella, M.M., et al., 2002).

2.3 Characteristics of Power Amplifier

The most important parameters when designing power amplifiers are listed below:

- Power (dBm or Watts)
- Efficiency (%)
- Gain (dB)
- Stability

These parameters are discussed deeply in (Maas, S.A., 2003) and (Bowick, C., 1982).

2.3.1 Power

There are two concepts of power for RF/microwave circuits: available and dissipated power. Available power is the maximum power, which is accessible from a source. The maximum available power is obtained from the source if the input impedance of the device equals the conjugate of the source impedance ($Z_{in}=Z_s^*$). Therefore, maximum available power as a function of frequency can be expressed as:

$$P_{av}(\omega) = \frac{1}{8}\frac{|V_S(\omega)|^2}{\mathrm{Re}\{Z_S(\omega)\}} \tag{2.1}$$

where $V_s(\omega)$ is a peak value of a sinusoidal voltage applied on input and $\mathrm{Re}\{Zs(\omega)\}$ is the real part of the source impedance.

The dissipated or transferred power is the power dissipated in a load. It can be expressed as:

$$P_d(\omega) = \frac{1}{2}\frac{|V_L(\omega)|^2}{\mathrm{Re}\{Z_L(\omega)\}} \tag{2.2}$$

where $V_L(\omega)$ is a peak value of a sinusoidal output voltage and $\mathrm{Re}\{Z_L(\omega)\}$ is the real part of the load impedance.

2.3.2 Gain

There are different definitions of the gain. The most useful is transducer gain, which is the ratio between the power delivered to the load and the power available from the source. The transducer gain can be expressed by:

$$G = \frac{P_L}{P_S} \tag{2.3}$$

where P_S is the RF drive power and P_L is the output RF power.

2.3.3 1 dB Compression Point

Non-linear response appears in a power amplifier when the output is driven to a point closer to saturation. As the input level approaches this saturation point, the amplifier gain falls off, or compresses. The output 1 dB compression point ($P_{out,1dB}$) can be expressed as the output level at which the gain compresses by 1 dB from its linear value. Figure 2.7 shows the relationship between the input and output power of a typical power amplifier.

$P_{in,1dB}$ at 1 dB compression point is related to corresponding output power, $P_{out,1dB}$ by

$$P_{in,1dB}(dBm) = P_{out,1dB}(dBm) + G_{1dB}(dB) \tag{2.4}$$

where G_{1dB} is the gain at the compression point.

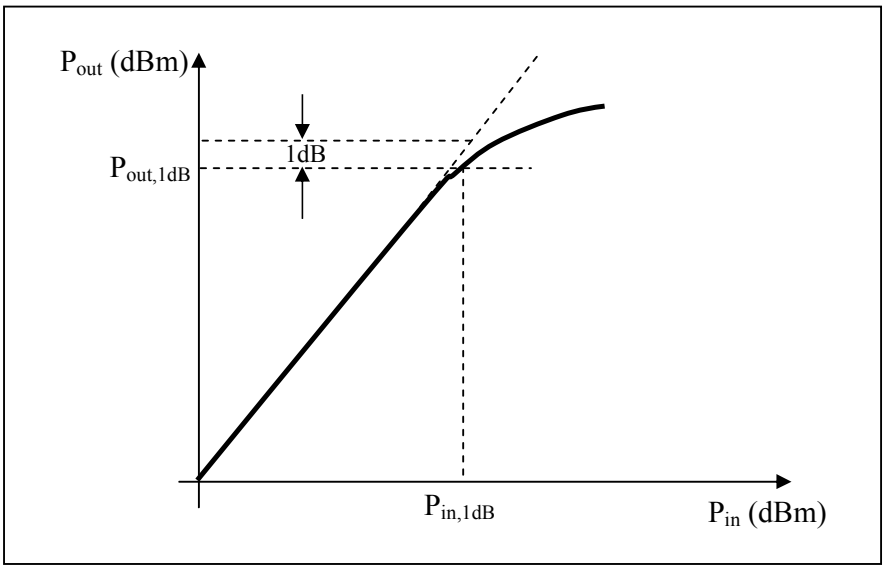

Figure 2.7: 1 dB compression point. .

2.3.4 Efficiency

The operational efficiency of the amplifier can be estimated by the output efficiency (drain efficiency):

$$\eta = \frac{P_{out}}{P_{dc}} \tag{2.5}$$

where P_{out} is the fundamental output power and P_{dc} is the DC power consumption.

In addition, one of the frequently used parameters is Power Added Efficiency (PAE), which takes the power of the input signal, P_{in} into account, expressed by:

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} \tag{2.6}$$

2.3.5 Stability

The power amplifier must be stable under all operating frequencies and all possible load termination. In other words, we have to design the power amplifier to reach "unconditional" stability, which means that no matter what the amplifier load is, it does not exhibit spurious oscillations even drive levels and supply voltages outside their nominal values. The main reason behind unstable behavior of the transistor is a reverse feedback from output to input. There are several factors to estimate stability for Class A, AB amplifiers. The Rollett factor (K) is based on the two-port S-parameters matrix expressed as (Bowick, C., 1982).

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12} \cdot S_{21}|} \tag{2.7}$$

where

$|\Delta| = |S_{11} \cdot S_{22} - S_{12} \cdot S_{21}|$,

S_{11} = Input reflection coefficient,

S_{12} = Reverse transmission coefficient,

S_{21} = Forward transmission coefficient,

S_{22} = Output reflection coefficient.

If K is greater than 1, then the transistor will be unconditionally stable for any combination of source and load impedance. If, on the other hand, K is less than 1, the transistor is potentially unstable and will most likely oscillate with certain combinations of source and load impedance. Several approaches can be considered to solve the instability:

1. Avoid the instability region when matching,
2. Reduce low frequency gain by adding a series resistor and capacitor, or knowing as RC feedback between output and input of the transistor,
3. Reduce the input and output impedance by resistive damping.

2.4 Wideband Amplifier

The most popular and well-establish circuit techniques employed in the design of broadband amplifiers that are realized in hybrid and monolithic technologies are:

- Reactively matched amplifier
- Lossy matched amplifier
- Resistive feedback amplifier
- Distributed amplifier

2.4.1 Reactively Matched Amplifier

The reactively matched amplifier shown in Figure 2.8 uses purely reactive matching networks at the input and output of the transistor, either lumped inductors and capacitors or transmission lines can be used. Since the matching networks are lossless, the reactively matched amplifier can be designed for optimum gain and output power. However, because of the transistor inherent instability and gain roll-off, wideband design is difficult.

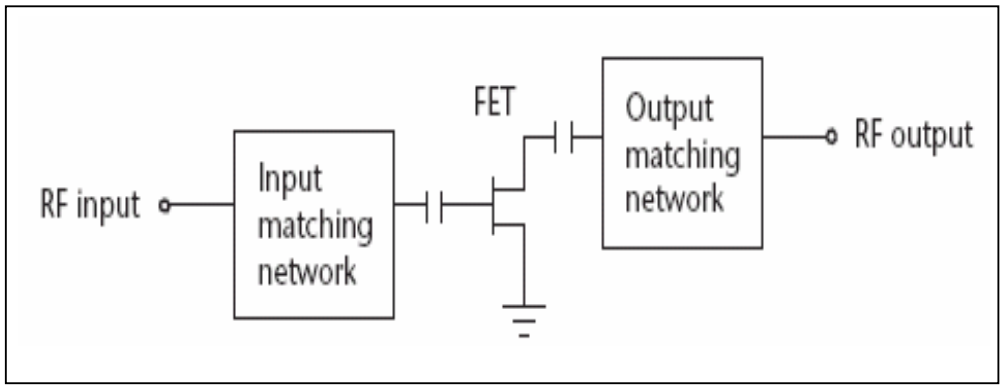

Figure 2.8: Reactively matched amplifier.

(Tserng, H.Q., et al., 1981) reported the reactively matched 2 GHz to 18 GHz power amplifier employing GaAs MESFET devices. The amplifier was designed using wideband impedance transformers realized in MMIC, and it achieved average power added efficiency in the range of 8 % to 15 % with and output power of 23 dBm.

(Palmer, C.D., et al., 1984) demonstrated the reactively matched MMIC multioctave power amplifier operating over the frequency range of 6 GHz to 18 GHz. The amplifier achieved an output power of 27 dBm with an average power added efficiency of 19 %.

2.4.2 Lossy Matched Amplifier

The lossy matched amplifier shown in Figure 2.9 uses resistors within its matching networks to enable flat gain to be achieved over a broad bandwidth. This is achieved by introducing high attenuation at low frequencies and low attenuation at high frequencies, while maintaining a good input and output match over the desired

bandwidth. The disadvantages of this approach, compared to the previous one, are that it has a lower gain and lower output power especially at low frequency.

(Zhu, X., et al., 2000) reported the lossy matched power amplifier employing GaAs MESFET devices. The amplifier was designed in MMIC with 0.5 um gate length, and it achieved >20 % of power added efficiency with output power of 1 to 1.4 watt across the 2-6.7 GHz frequency band. The main deficiency of this amplifier was that the output power start to degrade or attenuated at frequency lower than 2 GHz.

(Honjo, K., et al.,1981) in Japan obtained an 8.6 dB gain over the 3-dB bandwidth from 800 kHz to 9.5 GHz. The amplifier had an output power at 1 dB gain compression of 12 dBm over the 2 MHz to 9 GHz. Again, this output power was seems to be low at low frequency.

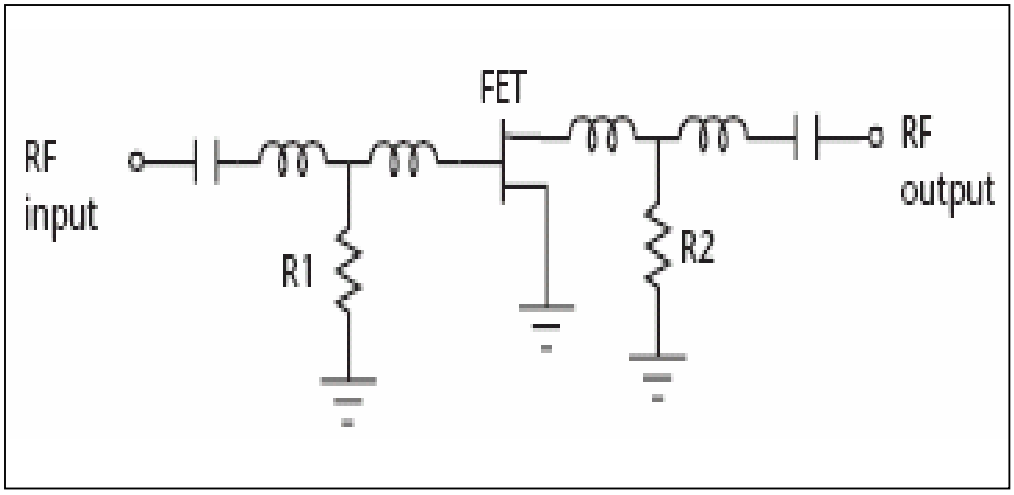

Figure 2.9: Lossy matched amplifier.

2.4.3 Feedback Amplifier

The feedback amplifier consists of three elements (i.e., resistor, R_{fb}, inductor, L_{fb} and capacitor C_{fb}) as shown in Figure 10. The value of the feedback resistor R_{fb} controls the gain and bandwidth of the amplifier. The feedback inductance L_{fb} reduces the effectiveness of the negative feedback with increasing frequency. The dc block capacitor C_{fb} is used to isolate the gate from the drain supply. The main disadvantage is the erosion of the output power over the lower end of the frequency band due to losses associated with the feedback resistor. The feedback amplifier can be very sensitive to frequency when implemented in hybrid technology; hence, its implementation dominates in MMIC technology.

(Niclas, K.B., et al., 1980) reported the feedback 350 MHz to 14 GHz power amplifier employing GaAs MESFET devices. The amplifier was designed using both negative and positive feedback realized in MMIC, and it achieved minimum gain of 4 dB with output power of 14 dBm.

(Terzian, P.A., et al., 1982) demonstrated the 1 GHz to 7 GHz monolithic negative feedback amplifier using lumped elements. The small signal gain was only 6 dB and output power at 1 dB compression was average of 10 dBm. These two reported data with low output power was due to the loss of the feedback resistor.

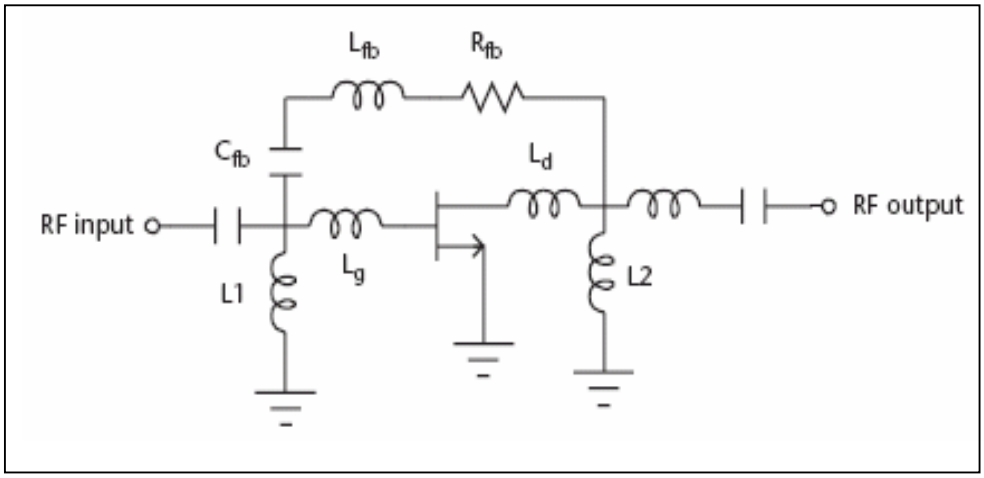

Figure 2.10: Feedback amplifier.

2.4.4 Distributed Amplifier

Distributed or traveling wave concept has been well researched and established; hence it is immensely popular in the design of amplifier, operating across multi-octave bandwidths. Distributed amplifiers shown in Figure 2.11 obtain high bandwidth by absorbing the transistor input capacitance, C_{gs} and output capacitance, C_{ds} into the input gate and output drain transmission lines, respectively. This type of amplifier eases the difficulties associated with broadband matching of the FET input and output impedances. More details of the concept of distributed amplifier will be discussed in Chapter 4.

The major disadvantages of the amplifier are its relatively poor output power and therefore low power added efficiency performance. Several techniques have been explored in the past few decades to improve the output power and efficiency.

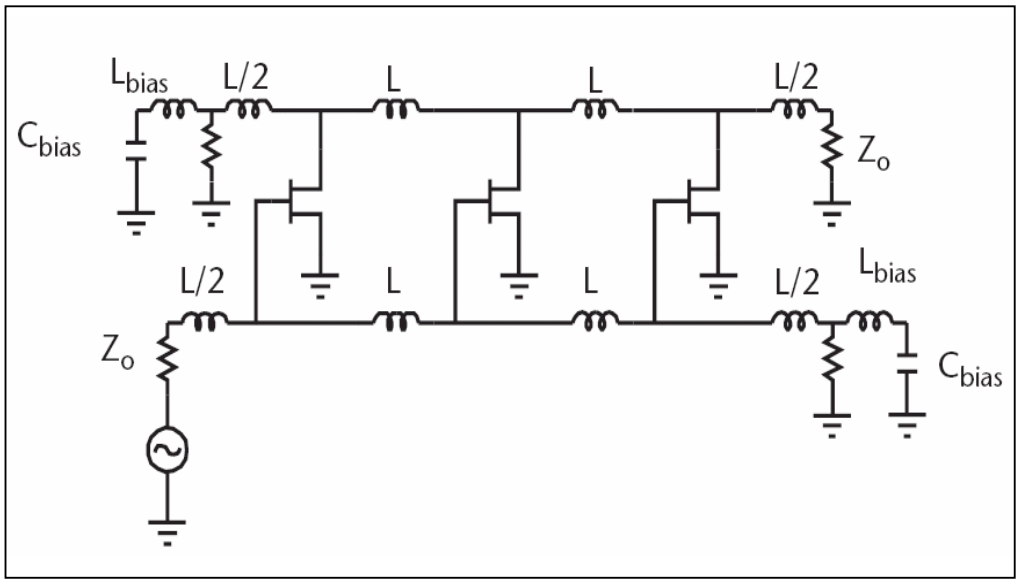

Figure 2.11: Distributed amplifier.

(Paoloni, C., et al. 1994) describe an innovative topology of a distributed amplifier based on input and output broadband Lange couplers. This topology establishes a remarkable improvement of the output power, power added efficiency and small signal gain. The performance of a 2-18 GHz conventional distributed amplifier is presented with power added efficiency in the range of 8 % to 15 %. The newly configured amplifier design achieves power added efficiency in the range of 13 % to 19 %, which is a significant improvement when compared with the conventional distributed amplifier.

(Shapiro, E.S., et al., 1998) described a novel distributed power amplifier topology, which employs power-combining techniques. Using the same traditional input line distributed techniques to achieve high bandwidth, this research has explored a delay line and corporate combining output topology which improves the distributed amplifier's efficiency at large signal by eliminating of the backward

waves. This amplifier designed to operate over the frequency range of 1 GHz to 9 GHz, achieves an efficiency of 25 % across the entire bandwidth. The conventional distributed amplifier, however, achieves 5 % to 10 % across the same bandwidth.

In recent year, (Fraysse, J.P., et al., 2000) has demonstrated a novel power distributed amplifier using the HBT cascode cell. More than 2 W have been measured in the 2-8 GHz frequency range with an associated gain of 9 dB and power added efficiency higher than 20 %.

In the following year, (Green, B.M., et al., 2001) has explored to employ cascode AlGaN/GaN high electron-mobility transistor for broadband high power amplifier in MMIC. Using a non-uniform distributed amplifier (NDA), a saturated output power of 3-6 W over a dc-8 GHz bandwidth with an associated power added efficiency of 13 % to 3 % was achieved.

CHAPTER 3
METHODOLOGY AND MEASUREMENT SETUP

3.0 Introduction

In this chapter, basic design procedure of a broadband power amplifier is described. Two types of power amplifiers are designed in this research; conventional broadband power amplifier and tapered distributed power amplifier. Both power amplifiers have their own design methodology and will be described individually. Besides, this chapter also presents the measurement setup used to measure the performance of the power amplifier.

3.1 Design Methodology in Conventional Broadband Power Amplifier

Figure 3.1 presents the summary of the design steps to be followed for a conventional broadband power amplifier. The design starts with determining the requirements and device selection. Power amplification in RF frequencies can be accomplished by using any one of many different devices; BJT, MOSFET, GaAs MESFET, HBT, etc. In this thesis, the PA is designed using MOSFET technology. After the device is chosen, DC analysis will be performed to obtain device I-V curves, which are used to determine the optimum bias points for the certain class of operation. The next step will be to determine the stability of the amplifier as well as maximum available gain, simultaneous source and load impedance using S-parameter simulation. Load and source pull simulation will be conducted to determine the optimum input and output impedance for maximum output power. Then, the input and output matching networks are designed to transform 50 Ω load to the optimum source and load impedance, respectively. Then, the overall performance of the PA design is tested via simulation tools. Finally, the circuit is fabricated on the

printed circuit board (PCB) and the performance is measured. The detail of the design of conventional broadband power amplifier is described in Chapter 4.

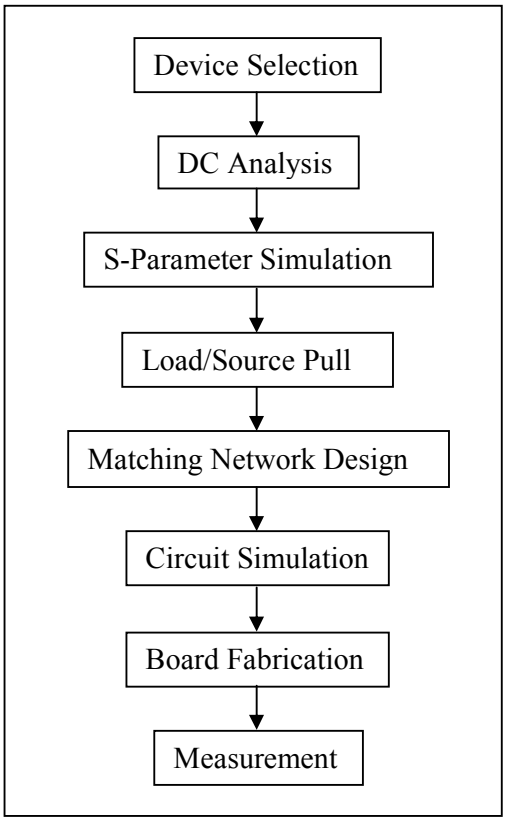

Figure 3.1: Design steps for conventional broadband power amplifier.

3.2 Design Methodology in Tapered Distributed Power Amplifier

The design steps for the tapered distributed power amplifier is slightly different compared with conventional power amplifier design. Figure 3.2 presents the summary of the design steps for tapered distributed power amplifier design.

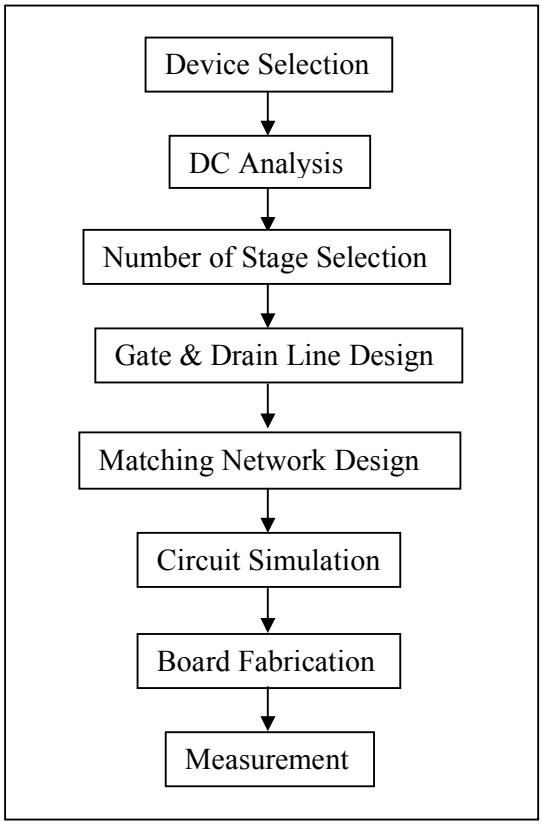

Figure 3.2: Design steps for tapered distributed power amplifier.

The first two steps, device selection and DC analysis, are similar steps as conventional broadband power amplifier. The next step is to select number of stages. Theoretically, an ideal distributed amplifier has no limits on the number of sections that can be connected together. The larger the number of sections selected, the higher the gain of the amplifier can be achieved. In reality, however, practically considerations limit the maximum number of sections. In this thesis, three stages or sections are used. After the number of stage is chosen, the gate and drain line of the distributed amplifier can be designed. The intrinsic parameters of the selected device, such as gate to source capacitance, C_{gs}, drain to source capacitance, C_{ds} and drain to gate capacitance, C_{dg}, will be employed to design the gate and drain line of the