COMPARISON OF FRONT - AND BACK - JUNCTIONS MONOCRYSTALLINE SILICON SOLAR CELL

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COMPARISON BETWEEN FRONT- AND BACK-JUNCTION MONOCRYSTALLINE SILICON SOLARCELL

by

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LIST OF ABBREVIATION

.

AFM	Atomic force microscopy.
ALE	Atomic layer epitaxy.
CdTe	Cadmium telluride.
CH_3CHOOH	Acetic acid.
CFP	Conventional Furnace Processing.
CVD	Chemical vapour deposition.
CZ	Czochralski silicon.
EDS	Energy dispersion spectroscopy.
EWT	Emitter wrap through
FF	Fill Factor.
FZ	Float zone
GaS	Gallium Arsenide.
I-V	Current voltage.
InP	Indium Phosphate.
LPE	Liquid phase epitaxy.
MOVPE	Metal organic vapour phase epitaxy.
MBE	Molecular beam epitaxy.
MWT	Metal wrap through.
O_2	Oxygen.
PSG	Phosphosilicate glass.
r.m.s	Root mean square.
RTP	Rapid thermal processing.
SEM	Scanning electron microscope.
SiO_2	Silicon dioxide.
SOD	Spin-on-dopant.
SOG	Spin-on-glass.
SLAR	Single layer antireflection.
I_{SC}	Short circuit current.
V_{OC}	Open circuit current
FF	Fill factor.
P_m	Maximum power

V_m	Maximum voltage
I_m	Maximum current
J_{SC}	Short circuit current density.

LIST OF SYMBOLS

Symbol	Unit	Name or Description
ε	F/cm	Semiconductor permittivity
η	%	Efficiency
τ	μs	Carrier lifetime
C	2.9979×10^{8} m/s	Velocity of light in the vacuum.
h	6.624×10^{-34} J.s	Planks constant
K_B	8.62×10^{-5}eV /K	Bolzmanns Constant
Q	1.602×10^{-19} C	Electron charge
N_C	3×10^{19} cm^3	Effective density of state in cond. band
N_V	1×10^{19} cm^{-3}	Effective density of state in valance band
n_i	1×10^{10} cm^{-3}	Intrinsic carrier concentration
μ_n	≤ 0.135 $m^2V^{-1}S^{-1}$	Electron mobility
μ_p	≤ 0.048 $m^2V^{-1}S^{-1}$	Hole mobility
D_n	$0.02586\ \mu_n$	Diffusion coefficient of electron
D_p	$0.02586\ \mu_p$	Diffusion coefficient of holes
E_g	1.124eV	Energy gap
G	cm s^{-1}	Minority carrier generation rate

PERBANDINGAN SIMPANGAN DEPAN DAN BELAKANG

MONOHABLURAN SEL SURIA SILIKON

ABSTRAK

Tesis ini menjalankan fabrikasi, pencirian dan pengoptimuman sel-sel suria persimpangan depan dan belakang. Sebagai sebahagian usaha kami iaitu strategi pengurangan kos, satu teknologi mudah pemprosesan relau konvensional (CFP) dan pemprosesan terma yang pesat (RTP) telah dibandingkan. Satu monohabluran wafer silikon dengan keluasan 19.64cm^2 dan keluasan aktif yang efektif 12.6cm^2 mempunyai kerintangan (0.75 1.25) Ωcm digunakan bagi mencari nilai optimum pemancar untuk kedua-dua bahagian hadapan dan belakang persimpangan sel suria. Sel persimpangan depan telah menggunakan CFP untuk peresapannya. Ia menunjukkan purata FF 69% dengan arus litar pintas Jsc= 35.0mA / cm^2 dan satu voltan litar buka yang cemerlang 0.640V, ia juga mempunyai kecekapan η = 15.6±1% (100mW/cm^2, 25^{0}C). Kami juga membangunkan satu sel persimpangan belakang yang direka di mana serasi dengan satu julat yang lebih luas untuk kualiti bahan silikon. Untuk persimpangan belakang sel suria secara lebih khususnya, kecekapannya adalah sangat bergantung pada bahan kualiti, nisbah ketebalan alat untuk panjang resapan pembawa minoriti dan permukaan-permukaan yang telah dipasifkan secara tinggi. Persimpangan belakang sel suria menunjukkan kecekapan 19.3±1 % dengan FF 72%, voltan litar buka V_{OC} 0.67V dan satu arus litar pintas 40.0mA/cm^2. Kami mendapati yang pembentukan pengeluar untuk sel persimpangan belakang memerlukan masa yang lebih panjang dengan menggunakan CFP, yang mana mungkin tidak ada serasi untuk pengurangan kos. Sel suria berefisyen tinggi memerlukan permukaan bertekstur untuk mengurangkan pantulan dan untuk

meningkatkan cahaya terperangkap. Sodium Hidroxide (NaOH) dan potassium hydroxide (KOH) selalu digunakan tetapi bahan-bahan ini adalah toksik dan tercemar. Ion K^+ dan Na mencearkan lapisan pasif SiO_2 yang didepositkan pada permukaan sel suria selepas proses pengteksturan. Dalam pengkajian ini, bahan alternatif yang mengandungi tetrametil ammonium hidrokside ($(CH_3)_4NOH$, TMAH telah digunakan. Pengkajian ini menunjukkan pengaruh beberapa parameter (konsentrasi,suhu dan masa) bagi proses pengtekturan. Daripada ujikaji menunjukan 3% TMAH konsentrasi pada 45 minit dan 90^0C memberikan kondisi terbaik bagi sel suria berefisyen tinggi. Sel suria dipasifkan dengan baik melalui penambahan lapisan SiO_2. Suhu deposit bagi lapisan pasif ialah 850^oC, ia adalah untuk menjaga jangka hayat pengangkut terkecil. Lapisan pasif ini mengurangkan kelajuan pengkombinasian semula permukaan bagi pengangkut terkecil.

COMPARISON OF FRONT AND BACK JUNCTION MONOCRYSTALLINE SILICON SOLAR CELL

ABSTRACT

This thesis undertakes fabrication, characterization and optimization of front and back junction solar cells. As part of our effort on cost reduction strategy, a simple technologies of conventional furnace processing (CFP) and rapid thermal processing (RTP) has been compared. A monocrystalline silicon wafer with an area of 19.64cm^2 and effective active area of 12.6cm^2 resistivity of (0.75-1.25) Ωcm was used to find an optimal emitter for both front and back junction solar cells. The front junction cell utilizes CFP for its diffusion. It shows an average FF of 69 % with short-circuit current density J_{sc}= 35.0mA/cm^2 and an excellent open circuit voltage of 0.640V with an efficiency of η = 15.6 %. We also developed a back junction cell whose design is compatible with a wider range of silicon material qualities. For back junction solar cell more specifically, its efficiency strongly depends on material quality, the ratio of device thickness to minority carrier diffusion length and highly passivated surfaces. The back junction solar cell demonstrated an efficiency of 19.3 % with FF 72 %, open circuit voltage V_{OC} of 0.67V and a short-circuit current density of 40.0mA/cm^2. We found that emitter formation for back junction cell requires a very long time by using CFP, which might not be compatible with cost reduction. High –efficiency silicon solar cells requires texturing of the front surface to reduce reflectance and to improve light trapping. Sodium hydroxide (NaOH) and potassium hydroxide (KOH) are commonly used, but these solutions are toxic and pollutant. The K^+ and Na ions contaminate the passivation layer SiO_2 deposited on the surface of the cell after texturing. In this study an alternative solution containing

tetramethyl ammonium hydroxide ($(CH_3)_4$ NOH), TMAH) was used .This research show the influence of different parameters (concentration, temperature and time) for the texturing processes. We found that 3 % TMAH concentration at 45 min and 90 ^{0}C gave an optimized condition for high efficient solar cells. The solar cells were excellently passivated by the growth of SiO_2 layers. The deposition temperature of the passivation layer was kept at 850 ^{0}C, in order to maintain high lifetime of minority carriers. This passivation layer reduces surface recombination velocity of the minority carriers.

COMPARISON OF FRONT AND BACK JUNCTION MONOCRYSTALLINE SILICON SOLAR CELL

ABSTRACT

This research thesis was undertaken to fabricate, characterize and optimize the front and back junction solar cells. As part of an effort towards cost reduction, simple technologies of conventional furnace processing (CFP) and rapid thermal processing (RTP) were compared. A monocrystalline silicon wafer with an area of 19.64cm^2 and resistivity of (0.75-1.25) Ωcm was used to find an optimal emitter for both the front and back junction solar cells. The front junction cell utilized CFP for diffusion. It showed an average FF of 69 % with short-circuit current density J_{sc}= 35.0mA/cm^2 and a good open circuit voltage of 0.640V, with an efficiency of η = 15.5±1 % (100mW/cm^2, 25^{0}C).We also developed a back junction cell, the design of which was compatible with a wide range of silicon quality materials. For back junction solar cell specifically, its efficiency strongly depended on material quality, ratio of device thickness to minority carrier diffusion length and highly passivated surfaces. The back junction solar cell demonstrated an efficiency of 19.3±1 % with FF 72 %, open circuit voltage V_{OC} of 0.67V and a short-circuit current density of 40.0mA/cm^2. We found that by using CFP, emitter formation for back junction cell required a long time, which might not be compatible with the cost reduction strategy. High –efficiency silicon solar cells require a textured front surface to reduce reflectance and to improve light trapping. Sodium hydroxide (NaOH) and potassium hydroxide (KOH) are commonly used, but these solutions are toxic pollutants. The K^+ and Na^+ ions contaminate the passivation layer of SiO_2 deposited on the surface of the cell after texturing. In this study an alternative solution containing tetramethyl

ammonium hydroxide ($(CH_3)_4$ NOH), TMAH) was used .This research shows the influence of different parameters (concentration, temperature and time) on the texturing processes. We found that 3 % TMAH concentration at 45 min and 90 ^{0}C were the optimal conditions for highly efficient solar cells. The solar cells were well passivated by the growth of SiO_2 layers. The deposition temperature of the passivation layer was kept at 850 ^{0}C, to maintain high lifetime of minority carriers. This passivation layer reduced surface recombination velocity of the minority carriers.

CHAPTER ONE

INTRODUCTION

1.1 Motivation

Becquerel discovered the direct conversion of solar energy to electricity by the photovoltaic effect in 1839 [1].Showing that an electric field may arise between two electrodes attached to a liquid or solid system when illuminated. By using light of appropriate intensity and wavelength, it turns out that almost any condensed matter can be used to generate electricity of some efficiency in this way. Moreover, the first silicon solar cell was developed as early as 1954 by Bell laboratories [2], showing efficiency under solar radiation of as high as 6%. For a long time succeeding this event, the main use of solar cells was for power supply in space applications, with increased interest for small scale consumer products.

The photovoltaic industry produced 2.54 GW of solar cells in 2006 [3]. About 89.9% of these cells were made from monocrystalline and multicrystalline wafers, 7.4% from thin films (a-Si, CdTe, Cis) and 2.6% from silicon ribbons. Various research groups all over the world have been working on more advanced solar cell concepts and have successfully reached efficiencies of well above 20% [4-6].

There is a drastic increase in energy demands worldwide, which seems to be unavoidable in the near feature. In studies conducted in USA, it was found that electricity generation from fossil fuel accounted for as much as 34% of CO_2 , 37% of NO_x and 62% of SO_2 emissions from controlled sources [7]. Hence, for a merited

development of a sustainable economy in third world countries, the utilization of renewable energy resources was regarded to be of great importance. Environmental awareness has traditionally motivated the research into renewable energy sources.

Solar cell converts sunlight directly to electrical power without any pollution, exhaust, noise or moving parts. There could still be great environmental impacts if solar cells effectively reduce the amount of fossil fuel used in developing countries, which is predicted to be responsible for the majority of global CO_2 emission in the future.

The photovoltaic market has two main objectives. The first is to make the production of electricity as cheap as possible and the other is to maximize the performance of the solar energy system to be at moderate level of cost. The cost of solar energy system can be roughly divided into the following categories as shown in the Fig. 1.1 below;

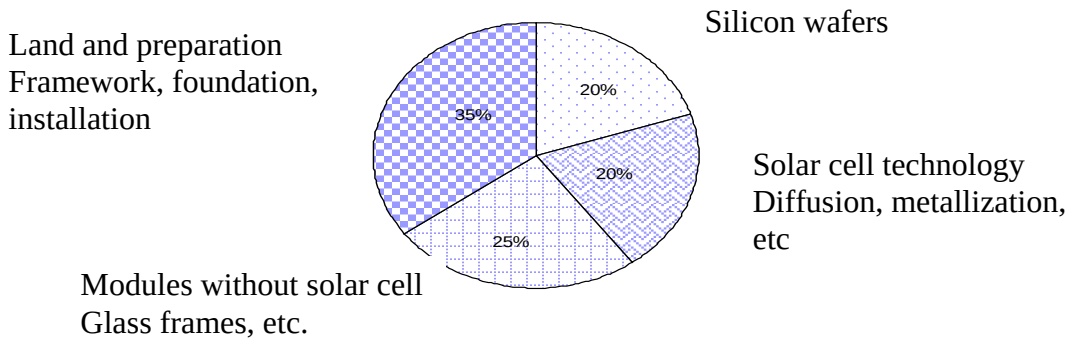

Figure 1.1: The cost breakdown of a solar array.

As shown in Fig1.1, about one fifth of the total cost of photovoltaic module is attributed to the silicon substrate [8]. The cost of the silicon wafers takes 20%, solar cell technology (diffusion, metallization etc) 20% while land and land preparation

(framework foundations, installation) 35%, and finally modules without solar cells account for 25%.

1.2 The Challenges

In the effort to bring PV one-step closer to being cost-effective with improved efficiency, researchers tried to develop different cell designs, having low thermal budgeting. Solar cell design includes cells with the junctions located either at the front or at the rear, with conventional furnaces processing (CFP) and rapid thermal processing (RTP) used to provide the required thermal input.

Rapid thermal processing is a promising method for the fabrication of crystalline silicon solar cell. It utilizes banks of tungsten lamp to quickly heat the semiconductor wafers. RTP drastically reduces the time required for solar cell fabrication when compared to CFP. For example, phosphorus emitter diffusion by CFP may require 30 minutes to 1 hour, whereas this is reduced to a few seconds to one minute when RTP is used.

In the microelectronics industry, RTP is well established. It is commonly used for the fabrication of high –quality layers. For example for the growth of ultra thin gates oxides, as well as the activation anneal of ion-implants are usually performed by RTP. Within the area of crystalline silicon solar cell, RTP so far has been used for the diffusion of P emitter [9 -12], for the growth of surface passivation oxides [13,14] and tunnel oxides [15,16] for the alloying of Al layer for back surface formation (BSF) and for firing of Ag front contacts [17-20]. However, RTP is relatively expensive and only single wafer RTP machines are available which can hardly meet the throughput of CFP batch furnace, despites its short time processing conditions.

1.3 Research Objectives

Researchers are trying to enhance the competitiveness of photovoltaic production with other forms of energy. The cost of industrial module is at present around Euro/W_P 2.15 .The aims of this research therefore, are:

- To reduced material cost; this can be achieved by a cell with its junction located at the rear of the wafer. This cell requires thin wafers which could subsequently, result to significant reduction in to the use of silicon.
- To improve the efficiency by lowering reflectance from the surface of the cell, texturing with tetramethyl ammonium hydroxide (TMAH) and antireflection coating that serves as passivating layer.

In order to reduce the cost of production of solar cell using low thermal input, we make comparisons between front junction cell and back-junction cell employing, both conventional furnace processing (CFP) and rapid thermal processing (RTP).

1.4 Organization of Thesis

The thesis starts with a brief history of photovoltaic in general and its significance to environmental protection when compared to other forms of energy like nuclear power.

Chapter 2 presents a comprehensive literature review of different types of solar cells, ranging from silicon and other materials with their fabrication procedures. The limitations of front junction cell over rear junction are also emphasized.

Chapter 3 provides a detailed explanation of the physics of the solar cell. The theories of phosphorus diffusion, oxidation, antireflection coating are discussed. In

Chapter 4, a presentation of the various equipments used in fabrication and characterization of our solar cell is made. The experimental procedures used to optimize the device are also explained.

Chapter 5 contains a comprehensive explanation and analyses of various results obtained from chapter four. The effects of diffusion conditions on front and rear junction cells are treated.

Chapter 6: This chapter contains a summary of results obtained from our study. Logical conclusions are drawn from the comparison between front and rear junction cells. Suggestions for future work in the same area are given as well.

CHAPTER TWO

LITERATURE REVIEW

2.1 Introduction

The previous chapter gave a brief history of the photovoltaic industry and its challenges. It also contains the aim and objectives of the research study intended to be performed. This chapter focuses on the evolution of the solar cell and the different types of cell. A great emphasis is laid on the limitations of front junction cell and the advantages of back junction cell.

2.2 Limitation of the Conventional Solar Cell

The conventional (front-contact) silicon solar cell has a structure in which a large p-n junction is formed over the entire substrate on the illuminated side of the cell. This conventional design has the virtue of simplicity, in that no patterning is required for the emitter (typically the p-type layer in a p-n junction cell), since it covers the entire front surface. However, simultaneous and conflicting requirements are imposed on the front surface and the emitter layer in this type of arrangement. On one hand, the emitter diffusion should be shallow and have low dopant concentration ($<1\times10^{19}$ cm^{-2}), to reduce recombination which occurs with higher dopant concentrations.

On the other hand, such a shallow, lightly-doped emitter will have a high sheet resistance (current flows laterally through the top layer of a conventional cell, and in between any contact grid lines and sheet resistance is inversely proportional to the doped layer thickness) generally greater than 100 ohms/square, which will

necessitate that the grid contact line be closely spaced to avoid excessive ohmic power losses. Figs. 2.1 and 2.2 show a cross sectional and front view schematic representation of a front junction solar cell respectively.

Closely spaced contact lines in a conventional front-contact cell means reduced power from the cell due to shadowing of the underlying silicon by the contact material. One important limitation arises at high input intensity because large amount of current must be conducted from the front surface of the device, through a metal grid contact to wires or leads that connect the device to an external circuit. Power loss owing to series resistance increases as the square of the current, thus increasing as the intensity increases.

The metal grid cannot be made arbitrarily large without reducing the photo-generated current, since the grid blocks the light from entering the cell. Owing to numerous constraints on the grid design, which are necessary for both minimizing series resistance and maximizing the amount of light that enters the device, other aspects of the cell design (such as junction optimization) cannot be simultaneously optimized [21].

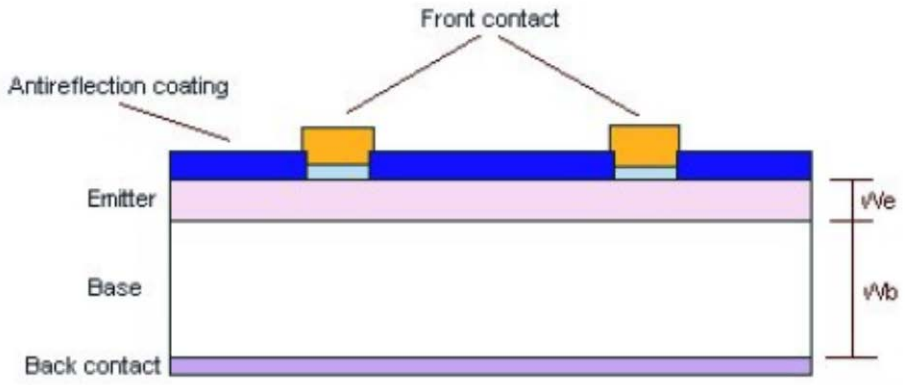

Figure 2.1: Schematic representation of front junction solar cell. (W_e is width of the emitter; W_b is the width base of the solar cell).

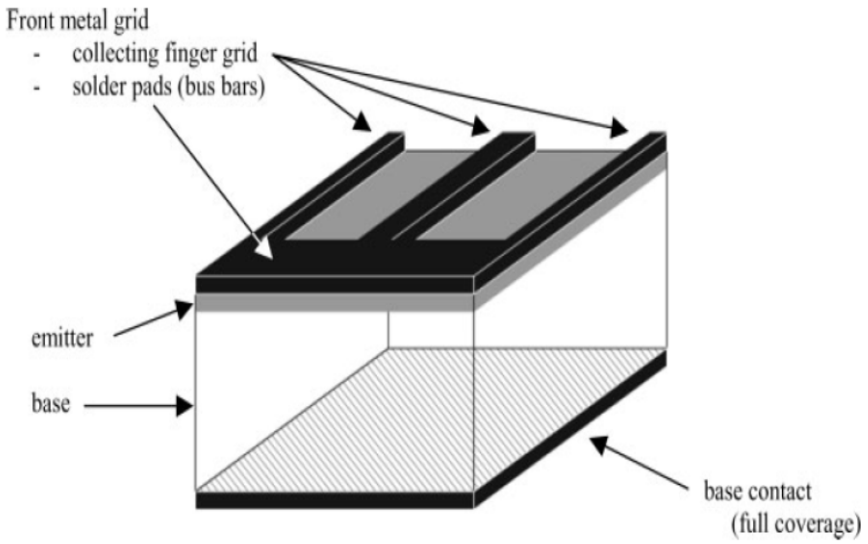

Figure 2.2: Schematic representation of a conventional solar cell.

Additionally, if the dopant concentration is low, the contact dopant layer interface will rectify (like a Schottky diode) rather than ohmic contact formation, with corresponding power loss associated with the turn-over voltage of the diode. However, the higher the dopant concentration, the greater the recombination of electrons and holes in the emitter layer, which is deleterious and typically occurs greatest near the surface, where incoming light shines.

For a conventional cell structure, a balance must be sought between the following features: desirability for a heavily -doped surface to promote ohmic contact formation, reduced shadowing, desirability for a lightly-doped surface, reduced carrier recombination and effective surface passivation. Constrains due to texturing and shadowing also constitute a problem; the alternative approach to these of which is to place the p-n junction on the (non-illuminated side) cell [22].

2.3 Advantages of Back-junction cell over Front -junction

1. The requirements for texturing and passivating the front surface are separated from the requirements for forming the p-n junction and for contacting the emitter and the base. This means the p-n junction can be deep and the emitter can be heavily doped without extreme consequences.
2. Back-contact cells have higher conversion efficiency due to reduced or eliminated contact obscuration losses.
3. Assembly of back-contact cells into electrical circuit is easier and therefore cheaper, because both polarities are on the same surface. Because of the significant cost savings compared to the present photovoltaic module, assembly can be achieved with back-contact cells by encapsulating the photovoltaic module and the solar cell electrical circuit in a single step.
4. Back-contact solar cells are better aesthetics through more uniform appearance. Aesthetics is important for some applications, such as building-integrated photovoltaic systems and photovoltaic sunroofs for automobiles.

2.4 Types of Back Contact Solar Cells

Back-contact solar cell is an alternative to the conventional solar cell. It simply refers to a cell design where all the interconnection circuitry is located behind the cell. Back-contact solar cells are generally categorized into the three main classes. These are:

2.4.1 Metallization wrap-through

Its concept is most closely linked to the conventional cell structure. The emitter is located near the front surface, but part of the metallization grid in the front is moved from the front to the back surface. Figure 2.3 shows a schematic representation of metallization wrap-through cell. This is depicted as the busbar moving from one

surface to another. The remaining front surface grid is connected to the interconnection pads on the surface by extending it through a number of openings in the wafer [23].

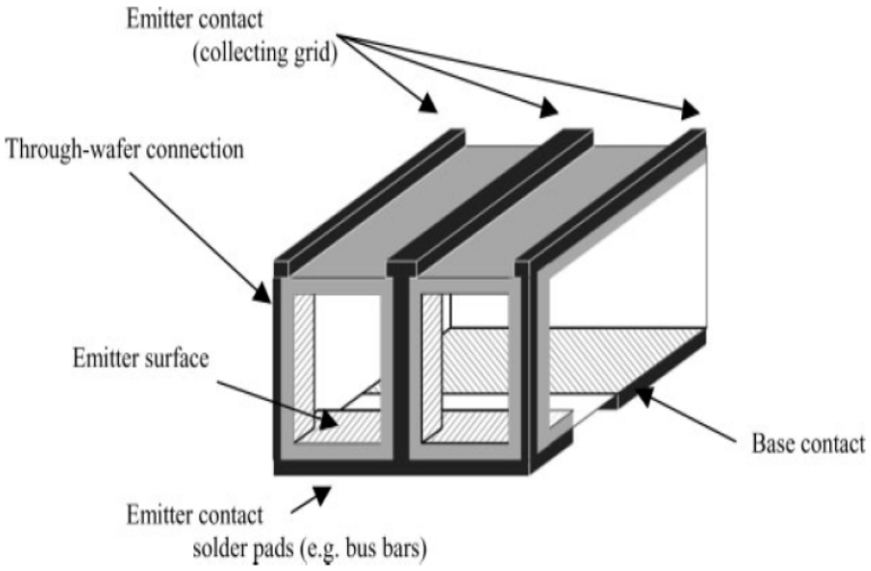

Figure 2.3: Schematic representation of a metallization wrap-through solar cell (**MWT**).

2.4.2 Emitter wrap-through

Its concept is similar to that of front junction cell but its surface is void of any metallization. The emitter is still located near the front surface; all the contacts are on the rear surface. In Fig 2.4, an embodiment of this structure is shown [24]. The current-collection between the active emitter near the front surface and the emitter contact on the rear surface is provided by extending doped conductive channels in the silicon wafer. Such conductive channels can be produced by drilling holes into the silicon substrate with a laser and subsequently forming the emitter inside the hole as well as forming the emitter on the front and the rear surface.

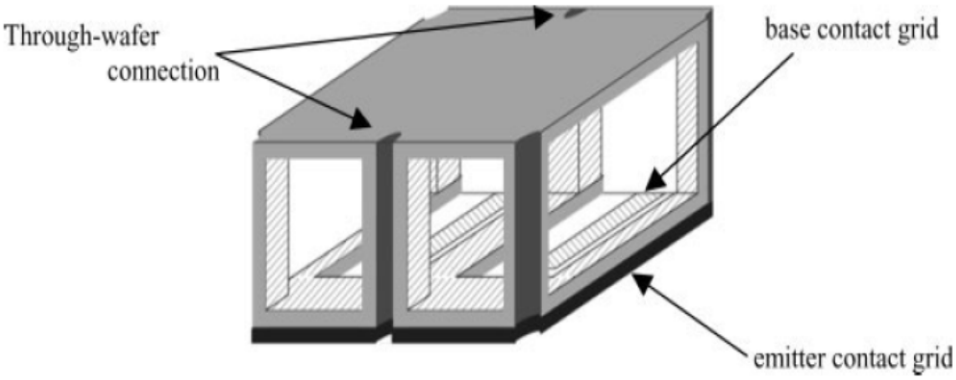

Figure 2.4: Schematic representation of an emitter wrap through solar cell (**EWT**).

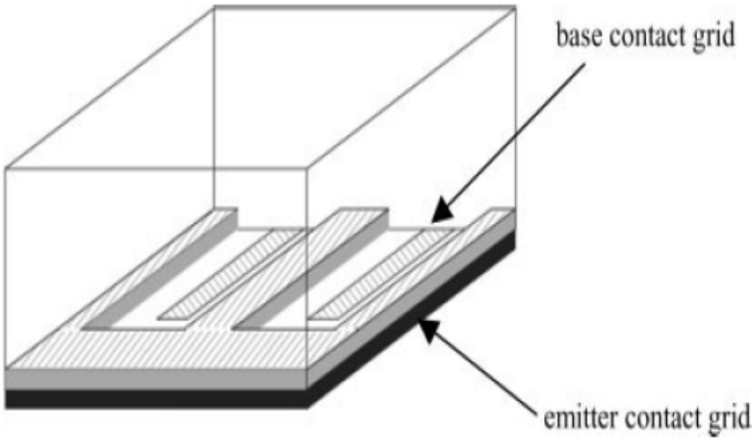

Figure 2.5: Schematic representation of a back junction solar cell.

2.4.3 Back-junction cell

The emitter is no longer located near the front surface, but put together with all contact on the rear surface. Since most of the light is absorbed and most of the carriers are photo-generated near the front surface, back- junction cells require very high quality material, so that carriers have sufficient time to diffuse from the front to the rear surface with the collection junctions on the rear surface. The schematic presentation of back junction solar cell is shown in Fig. 2.5.

2.5 Bifacial Solar Cells

In this type of cell, instead of very wide interdigitated fingers, an interdigitated finger grid is deposited with a similar layout but very narrow. This cell can be illuminated from both sides. Such a cell is capable of collecting diffused light from the back surface, thus increasing total efficiency. One variant of this cell consist of a cell with an n^+ layer on its back surface. This gives a structure similar to a transistor. The highest efficiency reported was 21.4 %, if the cell is illuminated on the non-metalized side. It also has an efficiency of 20.2 % when illuminated on the surface containing the grid. The lower efficiency was due to shadowing. This was the first bifacial cell with efficiency on both sides >20%. This high and very consistent values both show that the two sided surface passivation is very effective and that the carrier life time in the base must be very high [25- 26].

2.6 Buried Contact Solar Cell

This structure was first suggested in 1985 [27]. The significance of this cell is from the buried contact using laser technology; grooves of approximately 20μm wide and up to 100μm deep are cut in Si wafers textures according to the principle of random pyramids, to hold the grid fingers. The etching process which follows, removes the silicon destroyed by this process.

These grooves provide two advantages. First, shadowing is reduced significantly when compared with the normal grid structure of the commercial solar cell. Values of only 3 % surface shadowing are obtained. Secondly, the grooves can be filled with contact material. The technology of metallization consists of electrode deposited nickel contact, which is reinforced after sintering with copper.

Since this technique does not require photomask process or high vacuum evaporation technologies and is thus significantly more economical, it is predestined for use in large scale volume production. The double stage emitter is used for the emitter structure, where by the highly doped n^{++} film is restricted to the grooves. The p^{+} backfield permits higher efficiencies.

A further advantage of this cell is the textured back surface, which increase the confinement of light and thus the total efficiency. With this type of cell (large area), average efficiencies of 18 % has been achieved in production [28]. With specific techniques such as an improved antireflection coating and local back surface field, efficiencies of up to 21 % have been achieved in the laboratory [29].

2.7 Thin Film Solar Cells

A great effort has been in research and development in the field of thin film solar and other materials, with cell thickness of few micrometers. Thin film solar cell is expected to provide cost reductions and energy savings in cell manufacture.

All known semiconductor compounds [III-V or IV materials] are direct semiconductors, such that the absorption of light occurs within a crystal thickness of a few micrometers. For application in terrestrial solar technology however, these cells must have efficiency of the same magnitude as those of crystalline silicon and also high stability.

2.7.1 Amorphous silicon solar cells

An amorphous material (glass is a typical example) differ from a crystalline structure primarily because the strict periodicity of the lattice is not present. In particular, the absorption of light occurs directly. Amorphous silicon [a-Si] – is a compound of

silicon and hydrogen and has a band gap of approximately 1.7eV but varies between certain limits due to its hydrogen content.

In 1977, Carson [30], [31] produced the fist solar cell in RCA laboratory, with a very low efficiency of 2 %. The current production method for a-Si solar cells involves depositing the individual layers in a higher frequency glow discharge reactor. Silane (SiH_4) in a mixture with hydrogen is split into hydrogen and silicon. The required doping for the manufacture of solar cells is achieved by addition of dibromine B_2H_6 or phosphine (PH_3). In case of evaporation unto glass, the electrical contact is made using a conductive oxide film (TOC). Indium-Tin-Oxide (ITO) is often used for this purpose.

The critical problem of a-Si solar cells is their stability. The efficiency drop is degraded. The degradation acts primarily on the fill factor and the short circuit current, whereas the open circuit voltage remains constant. The degradation can be reversed only by exposing the cells to a temperature of approximately 160 ^{0}C.

2.7.2 Gallium-Arsenide (GaAS) solar cell

GaAs is also a very interesting material for photovoltaic applications. The energy gap for this semiconductor is 1.42 eV, with an effective adaptation to solar radiation. Further advantages are:

- GaAs is also a direct semiconductor and therefore up to 90 % of sunlight is absorbed in a film thickness of 2 µm.
- The temperature dependency of efficiency in a GaAs solar cell is only one –third of silicon due to higher energy gap.

Furthermore, this binary semiconductor can be transformed into a ternary semiconductor by the addition of elements from group (III or V) of the periodic table. This means that the semiconductor with lager bang gap can be produced, which can then act as window layer, or with smaller band gaps for tandem solar cell.

In addition, GaAs solar cells have a much lower sensitivity to cosmic radiation than Si solar cells. The GaAs solar cell is a cell with a p-n junction. There are currently three manufacturing process:

- Liquid phase epitaxy (LPE).
- Metal organic vapour phase epitaxy (MOVPE).
- Molecular beam epitaxy (MBE) carried out in an ultra high vacuum; therefore used almost exclusively in research and development laboratories.

In the first process a molten mass of Ga is almost saturated with As in a graphite crucible at a temperature of approximately 850 ^{0}C and dopants such as zinc and aluminium are added. For processing Ga it is placed with the crucible open at the bottom over an n-doped GaAs substrate.

First, a very small quantity of the n-GaAs is dissolved from the surface and secondly, during contact with the molten mass, zinc diffuses into the GaAs substrate thus doping a small part of the substrate to a p-material (creation of p-n junction). Thirdly, within the dissolved layer near the surface, some 85 % of Ga is exchanged for Al ($Al_{0.85}$ $Ga_{0.15}$ As), thus creating a semiconductor with a band gap of approximately 1.9eV. Using this elegant method –in which all necessary layers are created in a single step –an efficiency of 22 % was achieved (AM 1.5) [32].

To further improve efficiency, n^{+}-GaAs is required on the back surface. Both epitaxy processes mentioned permit the creation of any chosen layer sequence and

the dopant level. The technique of (MOVPE) was used to produce the highest efficiency of 25 % under AM1.5 [33].

Two problems prevent increased use of GaAs. One is the very high price of the GaAs cell, if the cell has to be built on its substrate. The second is a problem of acceptability, since Ga and As are toxic substances.

2.7.3 Cadmium-Telluride solar cells

Cadmium-Telluride has band gap of 1.45eV and like GaAs, it is an optimal semiconductor for conversion of sunlight. The first work dates back to the 1960s and early 1970s when an efficiency of 6 % was achieved [34-35]. Work was then put on hold until the 1980s, when it was taken up again by numerous laboratories around the world with different technologies. As well as the classical CVD and high evaporation techniques, other techniques were successfully developed such as; electrolytic deposition, chemical spraying as well as screen-printing.

The CdTe thin –film solar cell has achieved a world record of 15.8 % efficiency. The majority of CdTe devices are deposited on glass/transparent conductor substrates in a superstrate configuration. The 15.2 % cell was fabricated on fluorine-doped, tin oxide-coated 7059 glass. A 50-80 nm thick CdS is formed by chemical vapour deposition from an aqueous solution containing Cd acetate followed by a 3-5μm thick CdTe layer deposited by close-space sublimation. The back contact is formed first by etching the CdTe surface and then depositing HgTe. The completed device is annealed in an inert gas and finally a MgF_2 antireflection coating on the front glass [36].

Using atomic layer epitaxy (ALE) process, an efficiency of 14 % was .achieved. ALE deposits the CdTe from elemental Cd, S and Te at 240 ^{0}C substrate

temperatures via a sequential chemical reaction on the deposition surface. In addition to the typical glass (TG) and CdS/CdTe structure, the device includes a 250 nm thick graded CdS_xTe_{1-x} between the 50 nm thick CdS and the 3 μm thick CdTe layers.

2.7.4 Copper-Indium-Diselenide (CIS) solar cell

The first ones utilized a thick CdS layer as the window layer and bilayer (CIS) sequence, where a Cu-rich layer is deposited first, followed by an In-rich layer [37]. For the second device, a layer of approximately 1 μm thick of molybdenum is deposited onto a glass substrate, and then the active layer of Co-In-Se_2 is deposited with a thickness of 1-3 μm in a high vacuum using a multilayer evaporation process. As with all thin film solar cells, a window of ZnO (band gap approximately 3.2 eV) is then deposited on to a thin buffer layer of CdS with thickness of 0.3 μm. This cell achieves higher J_{sc} by using ZnO as the transparent conductor and thin CdS layer at the junction [38].

The highest efficiencies have been achieved with devices using a ZnO transparent conductor with a thin CdS junction layer. The best device, 14.8% efficient, consist of soda-lime glass with a 1500 nm Mo layer, a 2500 nm co-evaporated CIS layer, a 10 nm chemically deposited CdS layer, a 500 nm RF magnetron sputtered Al-doped ZnO layer and final temperature is ramped from 350 120nm MgF_2 AR coating [39]. The substrate temperature is ramped from 350 ^{0}C to 550 ^{0}C during the CIS deposition. After fabrication, the cell was annealed in air at 200 ^{0}C; an additional annealing of cell at higher temperature improves the efficiency of the cell.

The $CuInSe_2$ layer itself is polycrystalline, so the influence of grain boundaries and electronic state which exist strongly influence the characteristics of

photocurrent and open circuit voltage. In addition, low defect densities are decisive for the very high efficiency greater than 15 % and this can only be achieved using high vacuum evaporation techniques. The cheaper screen printing technique has also been tested for the purpose of cost reduction. In addition, the surface layers have recently been improved both in the quality of the CdS buffer layer and the window film. Using this process, several laboratories have been able to achieve efficiency of up to 17 % [40-41].

2.7.5 Indium Phosphide solar cells

Indium phosphide (1.35 eV direct band gap) has nearly the optimum value for high efficiency. Since the early 1960s, continuous evaluation of InP with many different processing technologies has continued. The resultant efficiencies were not high (approximately 10 %) and because of the perceived scarcity of In, the substrate cost were even higher than that for GaAs and this appeared to blow their chance to be used in terrestrial or space applications. The mechanism controlling the photocurrent and the junction rectification differ among these structures, although high short-circuits current and open-circuit voltage are achieved.

For shallow homojunctions, an anodic oxide antireflection layer on the front surface reduces the effect of front surface recombination on the cell properties [42]. Similarly, for the CdS/InP hetrojunction, interface recombination plays an important role because close lattice match between CdS and InP [43].

2.7.6 Organic Solar cell

Organic solar cell includes dye-sensitized and polymer bulk hetro-junction cells. In this type of cell, a semiconductor electrolyte contact converts light energy into

electrical energy. The concept was developed by Gratzel in the late 1980s. Nanoporous TiO_2 is sintered at 500 ^{0}C unto a glass plate, which is coated with transparent conductive oxide (TOC). A tin oxide doped with fluorine, which has a sheet resistance of approximately 10 Ω/square is used as a conductive film. The significance of the more conductive ITO cannot, unfortunately be used as it would not survive the sintering process. The semiconductor TiO_2 is not an option for photovoltaic process, due to its band gap of approximately 3 eV. It is transparent to sunlight; almost no absorption is possible. Therefore, the porous TiO_2 is coated with a dye based on ruthenium, such that a monomolecular layer is created. The dye bonds chemically with the TiO_2 surface. Visible light can be absorbed in this dye and the TiO_2 is placed in an electrolyte iodide and tri-iodide

2.8 Summary

This chapter gave an over view of the different forms of solar cell designs. The basic differences between these cells depend on their substrate materials. The most common substrates used include Silicon, Gallium-Arsenide, Cadmium-Telluride and organic materials to fabricate the cells. This chapter also explained the different types of back junction cell which include, metallization wrap-through and emitter wrap-through. A brief advantage of back junction solar cell over the front junction cell was also discussed.

CHAPTER THREE

THE WORKING CONCEPT OF SOLAR CELL

3.1 Introduction

The previous chapter consisted of a review on solar cell research and different forms of cell design. This chapter explains the physics of the solar cell, upon which the working principles of the cell are build. The basic equations, particularly the current density and continuity equations, the minority carrier transport mechanism and current density of the p-n junctions as well as the theories of diffusion and oxidation are discussed.

3.2 The Structure of the p-n Junction

For a comprehensive understanding of how a solar cell works, it is necessary to understand the p-n junction. A p-n junction is formed when n-type and p-type semiconductor materials are brought in contact with each other. In a diode, electron from the n-type will diffuse due to concentration gradient into the p-type material. Similarly, holes from p-type part will diffuse into the n-type region.

The result is that the n-type semiconductor is positively charged, whereas at the same time a negative charge will be created in the p-type semiconductor, such that a space charge region is developed. The band edge E_C and E_V will be adjusted such that the Fermi level E_F is constant throughout the crystal as shown in Figure 3.1 [44].

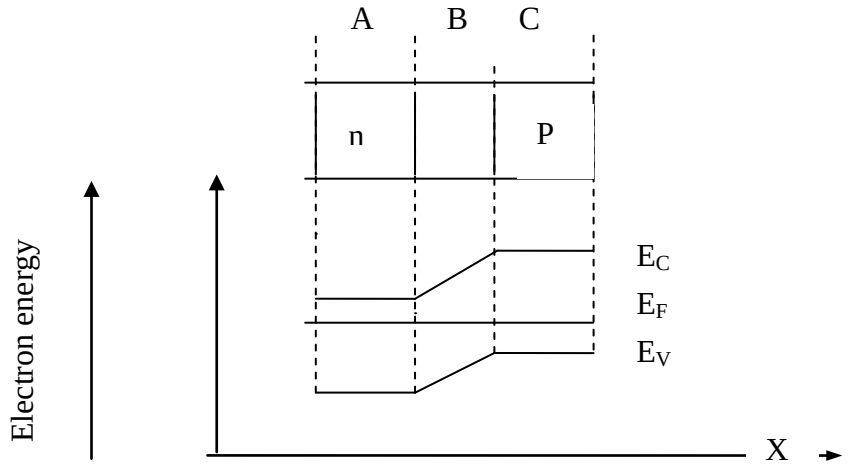

Figure 3.1: Semiconductor diode structure, E_c and E_v give the electron electrostatic energy, E_F the global electrochemical energy [44]

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3.3 p-n Junctions at Equilibrium

The ionized donor creates an internal electric field in the depletion region. The electric field produces the drift of minority carrier (holes) from the n-region to the p-region and the drift of the minority carrier electron from p-region to the n-region. Thus, the field produces the drift current in the direction from n-side to the p-side, opposing the diffusion current [45].

The motion of both the electrons and holes give rise to diffusion current in a direction from the p- region to the n- region. The magnitude of the electric field in the junction increases until the net current through the junction is zero; that is the drift current is equal and opposite to the diffusion current. When this condition of current balance is attained, the space charge region is said to be in thermal equilibrium. The electric field in the space charge region is large but outside the space charge region, neutrality prevails. The electric field in the space charge region works as a barrier preventing more electrons diffusing from n-side to the p-side.

Only the electron with enough energy can make transition. The majority carriers are the dominant carrier type ($n_{no} >> p_{no}$ and $p_{po} >> n_{po}$) therefore, n_{no} and n_{po} are the electron densities in the n- and p- sides respectively.

The concentration n_n of electrons (that is the number of electrons per unit volume) in the conduction band of n-type material and the concentration n_p of electrons (the minority carriers) in the conduction band of the p-type material in thermal equilibrium at temperature T, are given by the following equations [46].

$$n_n = N_C e^{\left[-\frac{E_C - E_F}{KB}\right]} \tag{3.1}$$

$$n_p = N_V e^{\left[-\frac{E_F - E_V}{KB}\right]} \tag{3.2}$$

where N_C and N_V are the effective density of states in the conduction band and valence band respectively. Dividing Eq (3.1) by Eq (3.2) we get;

$$\frac{n_n}{n_p} = \frac{e^{-\left[\frac{E_{Cn} - E_F}{KB}\right]}}{e^{-\left[\frac{E_{Cp} - E_F}{KB}\right]}} \tag{3.3}$$

The Fermi energy level E_F is closer to the bottom of the conduction band at energy level E_{Cn} in the n- type material and closer to the top of the valence band at energy level E_{Vp} in the p- type material.

Simplifying the right side of equation (3.3) we have the following,

$$\frac{n_n}{n_p} = e^{\frac{qV_D}{KB}} \tag{3.4}$$

Since,

$$E_{Cp} - E_{Cn} = qv_D \tag{3.5}$$

Taking the logarithm to base e of equation (3.4) and solving for V_D we get

$$V_D = \frac{KT}{q} \log e \left[\frac{n_n}{n_p} \right] \tag{3.6}$$

.

$$\frac{n_n}{n_p} = e^{\frac{[E_{CP} - E_{Cn}]}{KB}} \tag{3.7}$$

where E_{cp} and E_{cn} are conduction band in p-and n – materials respectively.

The same situation holds for the holes,

$$\frac{p_p}{p_n} = e^{\frac{qv_0}{KB}} \tag{3.8}$$

In n- and p- regions, the electrons and the hole concentration satisfy the law of mass-action.

$$n_n p_n = p_p n_p = n_i^2 \tag{3.9}$$

where n_i is the intrinsic carrier concentration. If all the donors and the acceptor atoms in n-and p-regions are respectively ionized then,

$$n_n \approx N_d \text{ and } p_p \approx N_a \tag{3.10}$$

where N_d and N_a are the concentrations of the donor and acceptor atoms respectively

$$n_p = \frac{n^2{}_i}{P_p} \approx \frac{n^2{}_i}{N_a} \tag{3.11}$$

Now substituting for n_n and n_p in equation (3.6) we get

$$V_D = \frac{KB}{q} \ln \left[\frac{N_d N_a}{n^2{}_i} \right] \tag{3.12}$$

The electron current flowing from the n-type to the p-type region strongly depends on barrier height. The n-type region forms an almost infinite electron source, however only those electrons which have enough energy will be able to diffuse over the built –in barrier V_D and to recombine in the p-type region.

Such an electron transport process is typically characterized by an exponential dependence on the barrier height, typically for a Boltzman distribution. This current is normally referred to as recombination current,

$$I_{recom} = I_0 \exp\left(-\frac{qv_D}{KB}\right) = I_{g,d} \qquad [94]$$

where K is the Boltzman constant, T the absolute temperature and I_0 the dark saturation current. This current is compensated by the current $I_{g,d}$ the generated current of electron in the p-type region which is independent of the barrier height and is determined by the availability of electrons on the p-side. In thermal equilibrium, these electrons are thermally generated.