DEVELOPMENT OF SiO_2 ON 4H-SiC BY DIRECT THERMAL OXIDATION AND POST OXIDATION ANNEALING IN HNO_3 & H_2O VAPOUR

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by

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LIST OF ABBREVIATIONS

AC	Alternating Current
AES	Auger Electron Spectroscopy
AFM	Atomic Force Microscope
AlN	Aluminum Nitride
Ar	Argon
ARXPS	Angular Resolved Photoelectron Spectroscopy
BN	Boron Nitride
BOE	Buffered Oxide Etch
B_2H_6	Diborane
C	Carbon
$(CH_3)_3Al$	Trimethyl-aluminium
Cl_2	Chlorine
CO	Carbon Monoxide
CO_2	Carbon Dioxide
C-V	Capacitance Voltage
DI	Dionized Water
et al.	et alii
E_B	Soft Breakdown
E_c	Conduction Band
E_{HDB}	Hard Breakdown
E_v	Valance Band
FIB	Focused Ion Beam
F_2	Fluorine

GaAs	Gallium Arsenide
GaN	Gallium Nitride
Ge	Germanium
GeO_2	Germanium Oxide
HCl	Hydrogen Chloride
He	Helium
HF	Hydrogen Fluoride
H_2	Hydrogen
H_2O	Water
H_2O_2	Hydrogen Peroxide
H_2SO_4	Sulfuric Acid
HNO_3	Nitric Acid
HRTEM	High Resolution Transmission Electron Microscopy
InN	Indium Nitride
I-V	Current-Voltage
J	Current Density
KOH	Potasium Hydroxide
Li	Litium
MOS	Metal-Oxide-Semiconductor
MOSFETs	Metal-Oxide-Semiconductor-Field-Effect-Transistors
Na	Natrium
Nacl	Sodium chloride
NAOS	Nitric Acid Oxidation of SiC
N_f	Fixed Oxide Charge Density
N_{it}	Near Interface Trap Density

NH_3	Ammonia
NHO_4	Ammonia Hydroxide
N_m	Mobile Oxide Charge Density
N_{ox}	Oxide Trapped Charge Density
N_2	Nitrogen
N_2O	Nitrous Oxide
NO	Nitric Oxide
O_2	Oxygen
O_3	Ozone
P	Phosphorus
PH_3	Phosphine
POA	Post Oxidation Anneal
$POCl_3$	Phosphoryl Chloride
PR	Photo Resist
Pt	Platinum
Q_{eff}	Effective Oxide Charge Density
QS	Quasi-Static
R_a	Average Roughness
RCA	Radio Corporation Of America
RMS	Root Mean Square
RTP	Rapid Thermal Processing
SEO	Sodium-Enhanced Oxidation
Si	Silicon
SiC	Silicon Carbide
SIMS	Secondary Ion Mass Spectroscopy

SiO_2	Silicon Dioxide
Ti	Titanium
TCE	Trichloroethylene
TofSIMS	Time-of-Flight Secondary Ion Mass Spectroscopy
TZDB	Time-Zero Dielectric Breakdown
UPS	Uninterruptible Power Supply
XPS	X-Ray Photoelectron Spectroscopy

LIST OF SYMBOLS

A	Capacitor Gate Area
A/cm^2	Current Per Centimeter Square
B	Parabolic Rate Constant
B/A	Linear Rate Constant
C_{fb}	Flat-band Capacitance
C_{ox}	Oxide Capacitance
C^o	The Interfacial Concentration of Corresponding Interstitials in the Oxide
C^1	The Solubility Limit of Corresponding Interstitials in the Oxide
$cm\ s^{-1}$	Centimeter Per Second
$cm^2\ s^{-1}$	Centimeter Square Per Second
$cm^2\ V^{-1}\ s^{-1}$	Centimeter Square Per Volatge Multiplied by Seceond
D	Defect Density (cm^{-2})
E	Electric Field (MV/cm)
E_A	Activation Energy
E_{ox}	Electric Field of Oxide
E_{SiC}	Electric Field if SiC
eV	Electron Volt
F	Cumulative Failure
I	Current
I_d	Drain Current
K	Kelvin
k	Boltzmann's Constant

k_l	Linear Rate Constant
k_0	The Interfacial Reaction Rate When Oxide Thickness Nearly Equals Zero
k_{ox}	Dielectric Constant of SiO_2 (3.9)
k_p	Parabolic Rate Constant
kV	Kilovolts
mJ/m^2	Milijoule Per Meter Square
ml/min	Millilitre Per Minute
mm	Milimeter
$m\ s^{-1}$	Meter Per Second
MV/cm	Megavolts Per Centimeter
N_D	Substrate Doping in Cm^{-3}
nm	Nanometer
q	Magnitude of Electronic Charge ($1.602 \text{ X } 10^{-19}$ C)
s	Second
T	Temperature
t	Oxidation Time
t_{ox}	Oxide Thickness
v	Interfacial Emission Rate
V	Voltage
$V\ cm^{-1}$	Voltage Per Centimeter
V_G	Gate Voltage
V_{th}	Threshold Voltage
Å	Angstrom
°C	Celsius

°C/min	Celsius Per Minute
ΔT	Temperature Difference
ΔV_{hys}	The Differences of V_{fb}
$\mu A/cm^2$	Micrometer Per Centimeter Square
μm	Micrometer
θ	Theta -Angle
λ	Lambda- Thermal Conductivity
%	Percentage
ε_{ratio}	Dielectric Constant Ratio
$\varepsilon_{r,SiC}$	Dielectric Constant of SiC ~ 10
$\varepsilon_{r,ox}$	Dielectric Constant of Oxide ~ 3.9
ε_o	The Free Space Permittivity ($8.854 \text{ X } 10^{-14} \text{ Fcm}^{-1}$)
ϕ_{ms}	Metal –Semiconductor Work-Function Difference
τ	Time Constant
α	The Production Rate of CO

PEMBANGUNAN FILEM NIPIS SiO_2 ATAS 4H-SiC MELALUI PENGOKSIDAAN TERMA LANGSUNG DAN POS PENGOKSIDAAN PENYEPUHLINDAPAN DALAM WAP HNO_3 & H_2O

ABSTRAK

Keperluan menghasilkan filem tebal SiO_2(> 50 nm) dengan keupayaan pecahan voltan yang lebih tinggi (> 5 MV/cm pada 1 uA/cm^2) melalui kaedah pengoksidaan terma adalah sangat penting bagi aplikasi peranti kuasa tinggi (> 600 V). Walau bagaimanapun, ia merupakan satu cabaran bagi menghasilkan oksida seperti dinyatakan di atas kerana oksida yang dihasilkan atas 4H-SiC telah dikenal pasti memiliki kepadatan kecacatan tinggi (> 10^{13} cm^{-2} eV^{-1}), disebabkan oleh kehadiran oksikarbida silikon, sisa kelompok C, Si- dan ikatan tergantung C- pada atau berhampiran muka SiO_2/SiC dan ini merosotkan prestasi peranti Logam-Oxida-Semikonduktor (MOS). Dalam kajian ini, suatu teknik novel iaitu pengoksidaan terma langsung dan pos pengoksidaan penyepuhlindapan menggunakan wap asid nitrik (HNO_3) dan H_2O melalui pelbagai suhu pemanasan 68% HNO_3 berair (60°C, 70°C, 80°C, 90°C, 100°C, 110°C) dan tempoh pemprosesan(1 jam, 2 jam dan 3 jam) telah dicadangkan bagi menyelesaikan isu-isu sepertimana yang dinyatakan di atas. Selepas kajian secara intensif, keadaan pemprosesan yang dipercayai paling menjanjikan untuk menghasilkan filem tebal SiO_2 (> 50 nm) dengan keupayaan pecahan voltan yang lebih tinggi (> 6 MV/cm pada 1 uA/cm^2) telah dinyatakan. Ia telah mendedahkan bahawa wap HNO_3 dan H_2O boleh digunakan sebagai ejen pengoksidaan terma langsung atau ejen pos pengoksidaan penyepuhlindapan pada suhu tinggi iaitu 1050°C, kedua-dua mereka memainkan peranan utama dalam mekanisma pengoksidaan/penitritan/penghidrogenan pada muka SiO_2/SiC dan

oksida pukal. Teknik di atas menyumbang kepada penghasilan filem tebal oksida dengan sifat-sifat elektrik yang lebih baik, kepadatan kecacatan perangkap muka yang lebih rendah (10^{11} cm^{-2} eV^{-1}-10^{12} cm^{-2} eV^{-1}) dan keupayaan pecahan voltan yang lebih tinggi (> 6 MV/cm at 1 uA/cm^2) berbanding dengan oksida yang dihasilkan dengan teknik pengoksidaan basah (H_2O wap sahaja) konvensional. Hasil kajian menunjukkan bahawa pengurangan ketara kandungan karbon pada muka SiO_2/SiC (~10^4 kiraan) berlaku semasa pengoksidaan/penyepuhlindapan dengan gabungan wap HNO_3 dan H_2O. Dengan menggunakan Spektroskopi Jisim Ion Sekunder Masa-Penerbangan dan Spektroskopi Fotoelektron Sinar-X, kesan daripada spesis hidrogen dan nitrogen yang mempasivasi kecacatan struktur pada oksida pukal dan antara muka SiO_2/SiC telah dibincangkan. Kesan wap HNO_3 dan H_2O pada sifat struktur substrat SiC selepas penyingkiran oksida dalam pelbagai keadaan eksperimen telah disiasat secara sistematik. Pencirian terhadap tenaga permukaan dan kekasaran permukaan substrat telah dikaji melalui Goniometer dan Mikroskop Tenaga Atom, masing-masing. Keputusan elektrik, reliabiliti, kimia dan fizikal filem SiO_2 yang dihasilkan atas 4H-SiC di dalam ambien wap H_2O dan HNO_3 telah dibentangkan dan hasil perbincangan dengan jelas memaparkan potensi baik teknik baru ini.

DEVELOPMENT OF SiO_2 ON 4H-SiC BY DIRECT THERMAL OXIDATION AND POST OXIDATION ANNEALING IN HNO_3 & H_2O VAPOUR

ABSTRACT

The need to thermally grow a thick SiO_2 film (>50 nm) with high breakdown voltage (> 5 MV/cm at 1 uA/cm^2) is crucial for high power devices (> 600 V) applications. However, it has been challenging to grow such oxides since the oxides grown on 4H–SiC has been identified to possess high density of defects (> 10^{13} cm^{-2} eV^{-1}), mainly attributed to the presence of silicon oxycarbides, residual C clusters, Si- and C- dangling bonds at or near the SiO_2/SiC interface which degrades the performance of Metal-Oxide-Semiconductor (MOS) devices. In this study, a novel technique of direct thermal oxidation and post oxidation annealing using nitric acid (HNO_3) and H_2O vapour at varied 68% HNO_3 aqueous solutions heating temperatures (60°C, 70°C, 80°C, 90°C, 100°C, 110°C) and process durations (1 hour, 2 hours and 3 hours) have been proposed to solve the above-mentioned issues. After intensive feasibility investigations of the experimental work, the most promising processing condition to produce thick SiO_2 film (> 50 nm) with high breakdown voltage (> 6 MV/cm at 1 uA/cm^2) was determined. It has been revealed that HNO_3 and H_2O vapour can be utilized as direct thermal oxidation or post oxidation annealing agents at high oxidation/annealing temperature of 1050°C; as they play a major role in oxidation/nitridation/hydrogenation mechanisms at the bulk oxide and SiO_2/SiC interface. The varied process durations of the above-mentioned techniques contribute to the development of thicker gate oxides (> 50 nm) with lower interface-state density (10^{11} cm^{-2} eV^{-1}-10^{12} cm^{-2} eV^{-1}) and higher breakdown

voltage (> 6 MV/cm at 1 uA/cm^2) as compared to oxides grown through a more conventional wet (H_2O vapour only) oxidation technique. The findings show that significant reduction of carbon content at the SiO_2/SiC interface (~10^4 counts) occurs with combination of HNO_3 and H_2O vapour during oxidation/annealing process. The study highlights the effects of hydrogen and nitrogen species on the passivation of structural defects at the bulk oxide and the SiO_2/SiC interface revealed through the use of Time-of-Flight Secondary Ion Mass Spectroscopy and X-ray Photoelectron Spectroscopy. It also systematically investigates the effects of HNO_3 and H_2O vapour on the structural properties of the SiC substrate after the oxide has been removed for various experimental conditions. The contact angles and the surface roughness of the substrate were recorded using a Goniometer and an Atomic Force Microscope respectively. The electrical, reliability, chemical and physical results of SiO_2 film grown on 4H-SiC in H_2O and HNO_3 ambient are presented and discussed clearly showing the potential of the new technique.

CHAPTER 1

INTRODUCTION

1.1 Introduction

In the early years of semiconductor electronics industry, Germanium (Ge) was the original material used to fabricate semiconductor devices such as diodes and transistors. However, the narrow band gap (0.66 eV) characteristic of Ge causes reverse-biased *pn* junctions in Ge and this eventually contributes to large leakage currents. This limits Ge device operation to temperature lower than 100°C. In addition, integrated circuit planar processing requires the capability of fabricating a passivation layer on the semiconductor surface. Germanium oxide (GeO_2) could act as such layer but it is water soluble and dissociates at 800°C, which resulted in Silicon (Si) replacing Ge for semiconductor devices fabrication (Stanley and Richard, 2000).

Si has a larger bandgap (1.12 eV) in comparison with Ge which results in smaller leakage currents and thereby allows Si based devices to be built with maximum operating temperature of about 150°C. The feasibility to form chemically stable silicon dioxide (SiO_2) which is the critical requirement for the gate oxide formation has made Si the dominant semiconductor for the electronics industry (Nicollian and Brews, 1982; Stanley and Richard, 2000). However, Si is not suitable for high temperature, high power and switching frequencies applications as its bulk properties is unable to withstand high breakdown field (Si critical avalanche electric

field is 0.3 MV/cm) (Zhao, 2005). To overcome these limitations, wide bandgap semiconductors are presently switching from research and development into real world applications. Wide bandgap semiconductors such as Silicon Carbide (SiC), Gallium Nitride (GaN) and Indium Nitride (InN) can be categorized into one group while diamond, Boron Nitride (BN) and Aluminum Nitride (AlN) into another because the former has bandgap of 2-3.5 eV and the latter 5.5-6.5 eV (Chow and Agarwal, 2006). As compared to Si, wide bandgap semiconductors have superior physical properties which offer a lower intrinsic carrier concentration (10 to 35 orders of magnitude), higher electric breakdowns field (4-20 times), a higher thermal conductivity (3-13 times) and a larger saturated electron drift velocity (2-2.5 times) (Siergiej *et al.*, 1999; Wang and Zhong, 2002; Dimitrijev and Jamet, 2003; Chow and Agarwal, 2006).

Of all the wide bandgap semiconductors, SiC has become the material of choice for semiconductor devices because the other wide bandgap nitride materials (GaN, InN, BN, AlN) need to be grown on substrates such as sapphire to get thermal advantages. On the other hand, diamond is a harder material which needs higher temperature for processing (Committee on Materials for High-Temperature Semiconductor Devices, 1995). SiC has the ability to grow SiO_2 using conventional thermal oxidation (like Si) and able to withstand harsh environment such as at elevated temperature. This makes SiC as a choice of material for the development of power semiconductor devices applications (Fujihira *et al.*, 2004).

1.2 Problem Statement

SiC exists in approximately 200 of polytypes, however, efforts were subsequently shifted toward 4H-SiC which has a larger forbidden energy bandgap of 3.2 eV and higher carrier mobility, as compared to 6H-SiC and 3C-SiC counterparts (Zhao, 2005). Despite of 4H-SiC materials advantages, there are many problems still exists in the full implementation of this material into semiconductor devices. This is due to large band gap of 4H-SiC polytype, which is about three times that of Si, may causes states associated with interface traps more likely to be induced in levels located within the bandgap (Shenoy *et al.*, 1996). Thus, the making of defect free SiO_2/SiC interface is more difficult than in the case of SiO_2/Si as oxides grown on SiC have high interface and near interface traps originating from silicon oxycarbides, residual C clusters, Si- and C- dangling bonds at or near the SiO_2/SiC interface. Types and origin of oxide trap charges in SiO_2/SiC system are discussed thoroughly in Section 2.2.3.

Basically, the above mentioned traps contribute to the scattering of electrons and trapping of carriers in near interface traps located within the oxide adjacent to the interface. This causes low electron mobility which leads to threshold voltage instability in SiC based Metal-Oxide Semiconductor (MOS) devices (Rudenko *et al.*, 2005; Dixit *et al.*, 2006). The low electron mobility particularly in fabricated Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) on 4H-SiC is of major concern and researchers are constantly looking for new ways of growing a dielectric. More extensive work is needed to seek the correlation between the channel mobility, fixed oxide charge, interface trapped charge, near interface trapped charge and oxide breakdown field (Zetterling, 2002).

Besides, power MOSFETs for 600 V and higher voltage applications such as switch-mode power supplies, AC motor drives, solar inverters and automotive electronics (Casady *et al.*, 1998; Hamada *et al.*, 2010; Fairchild Semiconductor, 2007; CREE Inc., 2012) , a high-quality with relatively thick gate oxide (> 50 nm) subjected to high electric field (>5 MV/cm) is much needed (Agarwal *et al.*, 2004; Takaya *et al.*, 2013). However, it has been challenging to grow such oxides since the oxides grown on 4H–SiC has been identified to possess high interface and near-interface traps. In order to solve the aforementioned issues, much effort has been spent in the quest to produce a high quality, reliable and thick gate oxide.

To date, thermally nitridated SiO_2 which is formed by direct oxidation or post oxidation annealing (POA) techniques in nitrogen-containing gases such as nitrous oxide (N_2O) or nitric oxide (NO) was found to be the effective processes to improve the SiO_2/SiC interface properties (Jamet *et al.*, 2001a,b; Dimitrijev *et al.*, 2004a,b; Noborio *et al.*, 2010; Swanson *et al.*, 2013). However, these techniques are not the favoured processing conditions to grow thick gate oxide which particularly requires high thermal budget and long hours processing durations.

Generally, thicker oxide could be obtained by growing oxides in wet ambient rather than in dry ambient due to a much higher solid solubility of H_2O in SiO_2 than O_2 in SiO_2, which in addition provides hydrogen passivation of electrically active defects near the SiO_2/SiC interface (Harris and Afanas'ev, 2000; Xu *et al.*, 2003; Benfdila and Zekentes, 2010). It has been reported that a large reduction in interface-trap density and improvement in reliability for both n- and p-types of 6H-SiC based MOS devices were obtained by wet N_2O nitridation (bubbling N_2O gas through de-ionized water at 95°C) as compared to the conventional dry N_2O nitridation (Xu *et al.*, 2003). So far, related observations are not being reported in

4H-SiC substrate**.** The reasons for the improvement of wet N_2O nitridation may be attributed to the effects of interface-traps passivation by hydrogen and nitrogen (Xu *et al.*, 2003). The passivation effects of both elements are identified to be pronounced when nitridated interfaces were annealed in hydrogen (Dhar *et al.*, 2006) or thermally grown oxides were annealed in ammonia (NH_3) ambient (Senzaki *et al.*, 2010; Soejima *et al.*, 2013). Both these techniques improve the SiO_2/SiC interface qualities and oxide reliability, however, additional oxide growth has been prevented. The factors influencing the fabrication of thermally grown SiO_2 films on SiC substrate is discussed thoroughly in Section 2.3.

Taking into account the major role of hydrogen and nitrogen as passivation elements and the necessity to grow thick gate oxide in optimized processing conditions for high power devices, a novel technique of the direct thermal oxidation and POA using nitric acid (HNO_3) and H_2O vapour at varied 68% HNO_3 aqueous solution (azeotropic mixture of 68% HNO_3 with 32% water) heating temperatures and durations have been proposed. In this study, the utilization of HNO_3 and H_2O vapour as direct thermal oxidation or post oxidation annealing agent are systematically analyzed. They play a major role in oxidation/nitridation/ hydrogenation mechanisms at the SiO_2/SiC interface and bulk oxide at high oxidation/annealing temperature (1050°C). The new oxidation technique in this research work is expected to provide an alternate fabrication and technological processes of SiO_2 films on SiC by producing a reliable thick oxide in favour of industry demands.

1.3 Objectives

The main objective of this study is to investigate the role of HNO_3 and H_2O vapour as direct thermal oxidation and post oxidation annealing agent at high oxidation/annealing temperature. The goal of this project is to reveal MOS device characterization results for various parameters studies, which the outcomes of this work can be utilized to produce a reliable and a thicker gate oxide (> 50 nm) for high power (> 600 V) devices applications.

The performed experiments are to accomplish the following proposed objectives:

- To introduce a novel idea of fabricating oxides by using HNO_3 and H_2O vapour on the SiC at high temperature of 1050°C and investigate the oxidation/nitridation/hydrogenation mechanisms at the SiO_2/SiC interface and bulk oxide.
- To utilize HNO_3 and H_2O vapour as direct thermal oxidation agent on 4H-SiC at varied 68% HNO_3 solution heating temperatures (60°C,70°C,80°C,90°C,100°C and 110°C) and oxidation process durations (1,2 and 3 hours).
- To utilize HNO_3 and H_2O vapour as post oxidation annealing agent on 4H-SiC at varied 68% HNO_3 solution heating temperatures (60°C,70°C,80°C,90°C,100°C and 110°C) and post oxidation annealing durations (1,2 and 3 hours).
- To determine the optimized condition to grow thick SiO_2 film (>50 nm) on 4H-SiC between direct thermal oxidation and post oxidation annealing techniques in HNO_3 & H_2O vapour.

1.4 Scope of Study

The scope of the project is to fabricate a reliable thick gate oxide on 4H-SiC in a combination of HNO_3 and H_2O vapour by direct thermal oxidation and post oxidation annealing techniques. The set of experiments are performed to study the effects of SiO_2 film grown on 4H-SiC with varied heating temperatures of 68%HNO_3 solution and process durations for direct thermal oxidation and post oxidation annealing techniques, respectively. MOS structure was used to evaluate the electrical, reliability, chemical and physical results for both techniques.

In the Experiment Set 1, SiO_2 thin film was grown on 4H-SiC at various heating temperatures (60°C, 70°C, 80°C, 90°C, 100°C and 110°C) of 68% HNO_3 solution simultaneously with H_2O vapour via direct thermal oxidation technique. The purpose of this experiment is to determine the optimized 68% HNO_3 solution heating temperature by analyzing the oxide thickness and examining the electrical, reliability, chemical and physical results of the grown oxides. The Experiment Set 2 explores the direct thermal oxidation duration studies (1 hour, 2 hours and 3 hours) based on the best obtained results of 68% HNO_3 solution heating temperature from the Experiment Set 1. Despite examines the electrical, reliability, chemical and physical results of the grown oxides, the main idea of this set of experiment is to grow thicker and reliable oxide using HNO_3 vapour as direct thermal oxidation agent simultaneously with H_2O vapour with longer direct thermal oxidation duration.

The following Experiment Set 3 is performed to analyze the role of HNO_3 as post oxidation anneal agent. In this set of experiment, the oxides were fabricated on 4H-SiC in wet ambient (H_2O vapour) and annealed using HNO_3 vapour at varied 68% HNO_3 solution heating temperatures (60°C,70°C,80°C,90°C,100°C and

110°C). The purpose of this experiment is to determine the optimized 68% HNO_3 solution heating temperature by analyzing the oxide thickness and examining the electrical, reliability, chemical and physical results of the grown oxides using HNO_3 vapour as post oxidation anneal agent. The Experiment Set 4 explores the duration studies (1 hour, 2 hours and 3 hours) of the best obtained results of 68% HNO_3 solution heating temperature from the Experiment Set 3. The main idea of this set of experiment is to evaluate the oxide quality, reliability and most importantly to grow thicker oxide using HNO_3 vapour as post oxidation anneal agent with longer post oxidation anneal duration.

In the final analysis, the optimized results from Experiment Set 2 (direct thermal oxidation technique) and Experiment Set 4 (post oxidation annealing technique) are compared and discussed by additional chemical and physical characterizations. The reason for this analysis is to examine the effects of HNO_3 and H_2O vapour as direct thermal oxidation and post oxidation anneal agent on SiC substrate, which the best technique to produce a reliable thicker oxide could be further recommended for power devices fabrication process technology.

The key electrical parameters used to determine oxide quality are oxide thickness, flatband voltage shift, density of interface and near-interface traps, effective oxide traps, leakage current and maximum breakdown field of the oxide. The parameters are extracted by capacitance-voltage measurement and current-voltage measurement. Another important investigated issue is the reliability of the oxides which the flatband voltage shifts of the samples are determined after the samples have been treated under high-field stressing (7 MV/cm). In addition, Time-Zero Dielectric Breakdown (TZDB) on all experimental samples have been studied using Weilbull plots. The chemical analysis parameters included in this work are

Secondary Ion Mass Spectrometry (SIMS) and X-ray photoelectron Spectroscopy (XPS). On the other hand, surface roughness and surface energy of the 4H-SiC substrate after oxides removals are performed by Atomic Force Microscopy (AFM) and Goniometer characterization, respectively. The physical topologies of the thermally grown oxides on 4H-SiC by optimized process techniques are observed using High Resolution Transmission Electron Microscopy (HRTEM).

1.5 Outline of Thesis

This thesis is divided into 5 main chapters, whereby Chapter 2 details the relevant literature review of the study and Chapter 3 briefs on the methodology of the research work. Chapter 4 comprises the electrical, reliability, chemical and physical results which are obtained from the performed experiments. In this chapter, the results are displayed and discussed. Finally, Chapter 5 presents the conclusion and recommendations to further improvise the research work.

CHAPTER 2

LITERATURE REVIEW

2.1 SiC as a Semiconductor Substrate

SiC has been existed as a semiconductor substrate almost longer than Si but its usage was limited only for niche applications (Zetterling, 2002). There are several reasons for this, which the most critical problem is making SiC material of sufficient quality for power semiconductor devices applications (Zolper and Skowronski, 2005). The possibility to exploit the material for electronic devices became reality in the late 1980s after SiC wafers became available from a commercial vendor (Zetterling, 2002). The significant progress achieved in developing SiC material for semiconductor devices in the recent years has open up interest of more researchers to investigate in detail about the benefits of the material.

SiC crystal comprised of two atoms which are silicon (Si) and carbon (C) and normally each Si atom has exactly four C atom neighbours and vice versa. SiC generally has several hundred stacking orders possible which has been identified in nature (Figure 2.1). One of the stacking orders which forms hexagonal close packed scheme in which Si atoms stacked in this way with a layer of smaller C atoms directly on top (Figure 2.2). Four principal axes are commonly used: a1, a2, a3 and c to describe directions and planes in hexagonal crystal structures. In the close-packed plane, the three a-vectors or commonly called the a-plane has 120°C angles between each other, whereas the c-axis is perpendicular to this plane (Figure 2.3). On the other hand, three Miller indices, hkl, are used to describe directions and planes in the

cubic crystal. For example, the (100) plane is one of the six surfaces of the cube, whereas the (111) plane is perpendicular to the volume diagonal (Zetterling, 2002; Ayalew, 2004).

SiC has a polar crystal structure in which by looking perpendicularly at the a-plane, we will either see C atoms directly on top of Si atoms, or vice versa. The former is called the silicon face orientation, the latter the carbon face. In comparison with two faces, the silicon face is most commonly polished and used to manufacture devices on. The dopants used are aluminum and boron for p-type. On the other hand, nitrogen and phosphorous are used as dopants for n-type with trimethyl-aluminium $(CH_3)_3Al$, diborane (B_2H_6), nitrogen gas(N_2) and phosphine (PH_3) as the most common dopant precursors (Zetterling, 2002).

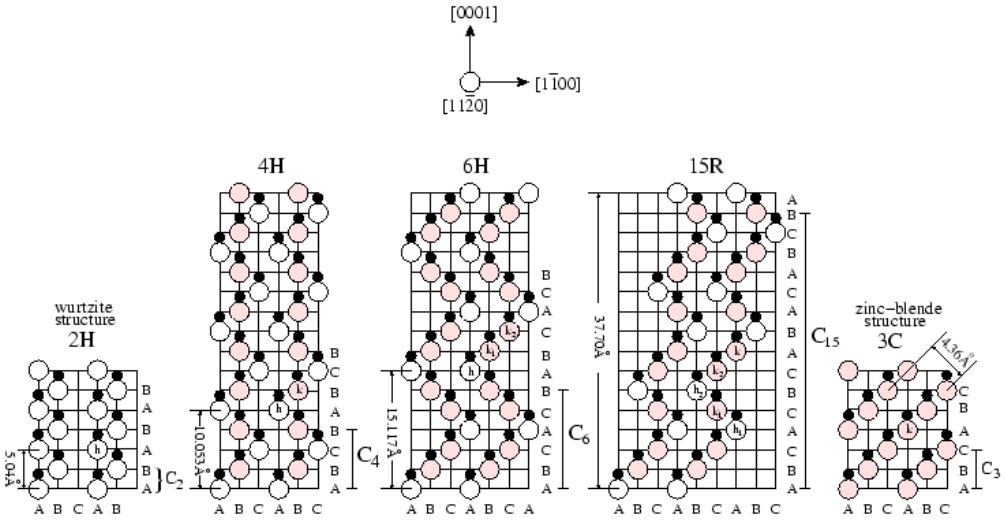

Figure 2.1: Stacking sequences for different SiC polytypes in the [1120] plane (Ayalew, 2004)

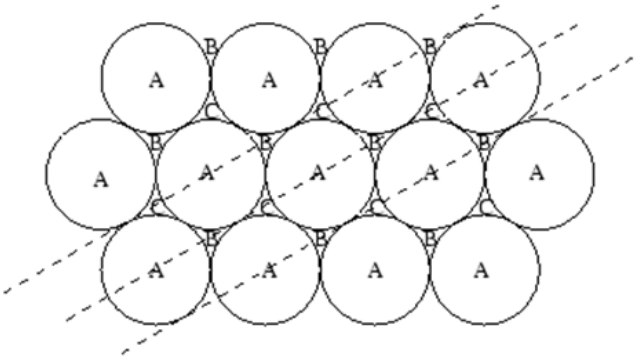

Figure 2.2: Site locations for C atoms in the [1100] plane (Ayalew, 2004)

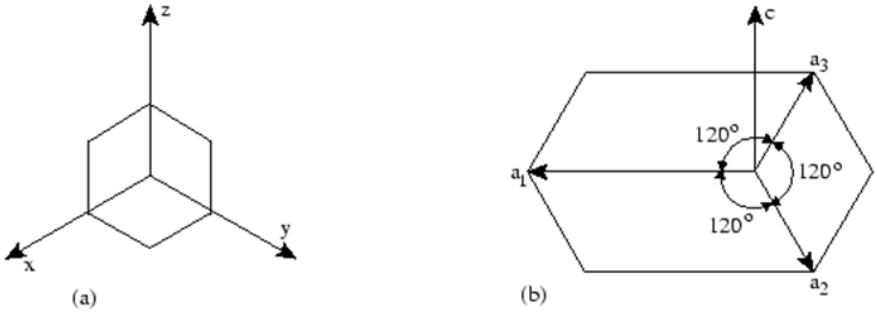

Figure 2.3: Principal axes (a) for cubic and (b) for hexagonal crystals (Ayalew, 2004)

SiC has emerged as a semiconductor device substrate, due to several good reasons which the relevant electrical property depends on the device application intended. The key reason to almost all advantages of using SiC in devices is its wide bandgap characteristics. The ability to withstand harsh environment such as at elevated temperature added advantage for the development of SiC for semiconductor devices (Choyke *et al.*, 2001). For high-temperature devices, higher doping may be used in order to raise the threshold, the intrinsic temperature, where thermal generation is too high. SiC with its wide bandgap, depending on polytype and doping has an intrinsic temperature around 1000°C (Zetterling, 2002).

SiC as the wide bandgap material has high impact ionization energy which means that the electric field can become very high without avalanche multiplication of ionized carriers. SiC offers approximately ten times higher electric breakdowns field than Si for the same depletion width. Therefore, the doping in the low-doped region for SiC can be 100 times higher for the same breakdown voltage. With a ten times thinner depletion region and 100 times higher doping, the on-resistance is approaching 1000 times lower values which offers advantages for high-voltage devices (Zetterling, 2002).

Basically, SiC can be made smaller for the same breakdown voltage or in other words the signal has a shorter distance to travel which makes the device operates faster. The relative dielectric constant is also lower for SiC than for most other semiconductors and since the capacitance is directly proportional to the dielectric constant, the parasitic capacitances will be smaller as well. The saturated electron velocity is also high in SiC, twice that of Si and GaAs (Zetterling, 2002).

In terms of applications, recent developments in SiC device technology have opened up the aerospace and aircraft domains for SiC based power electronics, where these devices could be utilized for substantial weight savings and enhanced jet engine performance (Dixit, 2008). SiC material can be used to replace Si as substrate in power circuits of electric motors and power control for electric vehicles, robotics, and power supplies (Dhar *et al.*, 2005). It offers much higher efficiencies than Si in these applications.

Figure 2.4 shows that by replacing the Si-based devices to SiC-based devices, the power conversion loss can be reduced to one-third and by 2030, approximately 5.8 million kW of energy can be saved. Figure 2.4 also shows that energy in crude oil also can be saved in the near future if SiC material is successfully implemented in power devices. The facts clearly show SiC-based devices will have a major impact on the size, efficiency and application of power electronics (Arai, 2011).

Table 2.1 are some of the important electrical properties of the common polytypes of SiC. In terms of applications purpose, the wafer has to be single crystal and only a few polytypes are stable enough for large wafers production. Commercial wafers are available as either in 4H-SiC or 6H-SiC with diameters of 50, 75 or even 100 mm (Zetterling, 2004). Of 200 types of SiC polytypes, efforts were subsequently shifted toward 4H-SiC which has a larger forbidden energy bandgap of 3.2 eV and higher carrier mobility, compared with 6H-SiC and 3C-SiC (Zhao, 2011). As compared to Si and GaAs, SiC possess higher bandgap, breakdown field and thermal conductivity (Figure 2.5).

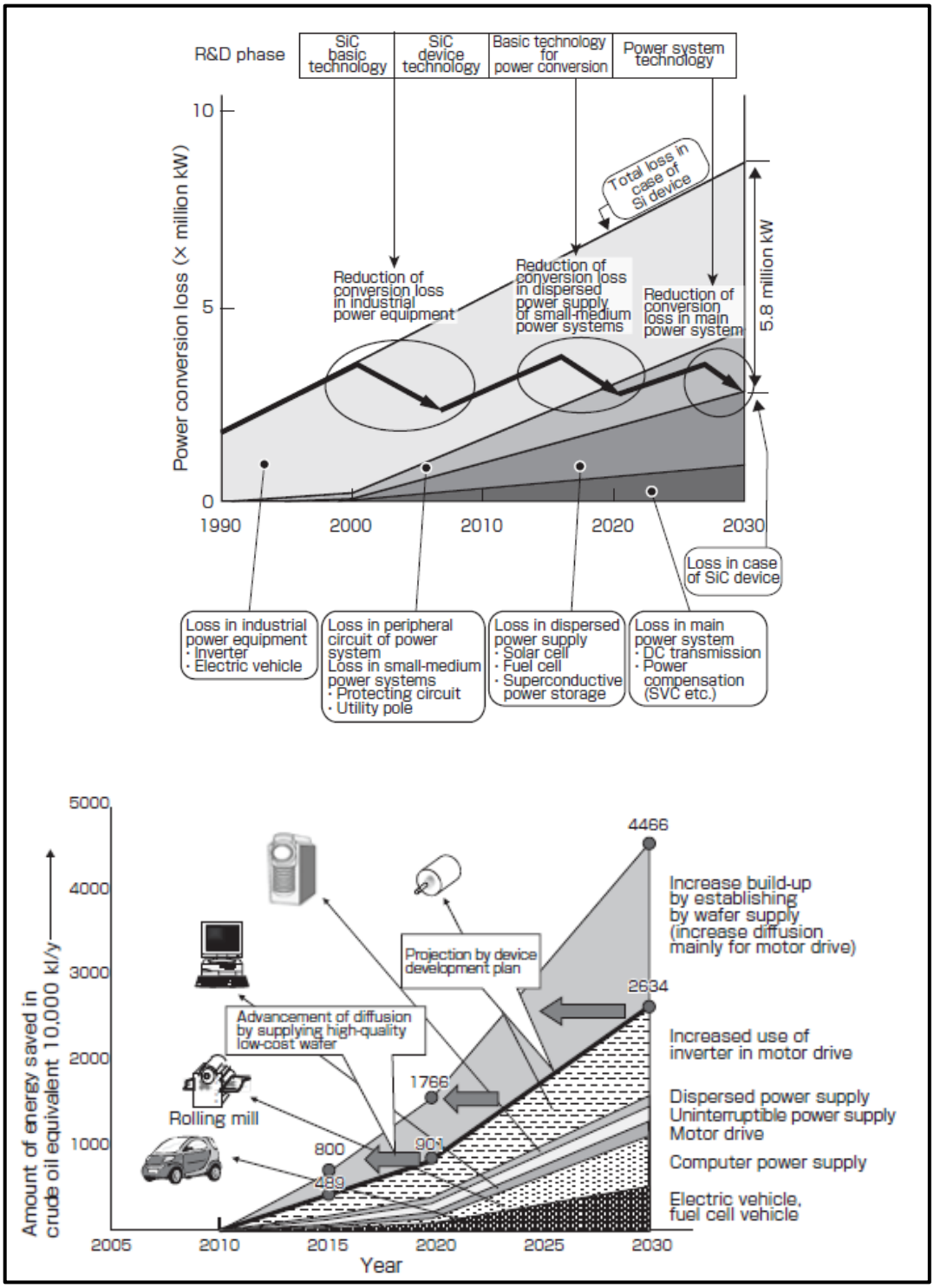

Figure 2.4: Effect on energy saving when the SiC device is implemented in Japan (Arai, 2011)

Table 2.1: Electrical Properties of common polytypes of SiC (Park, 1998; Levinshtein and Shur, 2001)

Properties	3C	4H	6H
Breakdown Field (V cm^{-1})	~10^6	6x10^5	6x10^5
Mobility ($cm^2 V^{-1} s^{-1}$)			
electrons	$\leq$ 800	$\leq$ 900	$\leq$ 400
holes	$\leq$ 320	$\leq$ 120	$\leq$ 90
Diffusion coefficient ($cm^2 s^{-1}$)			
electrons	$\leq$ 20	$\leq$ 22	$\leq$ 10
holes	$\leq$ 8	$\leq$ 3	$\leq$ 2
Electron Thermal Velocity (m s^{-1})	2 x 10^5	1.9 x 10^5	1.5 x 10^5
Hole Thermal Velocity (m s^{-1})	1.5 x 10^5	1.2 x 10^5	1.2 x 10^5
Saturated Electron Drift Velocity (cm s^{-1})	2 x 10^7	2 x 10^7	2 x 10^7

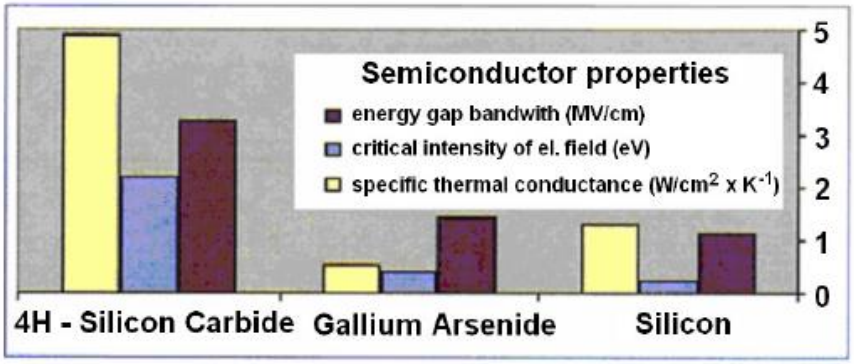

Figure 2.5: SiC properties compared to Si and GaAs (SiC Power Applications and Device Roadmap (Drabek, 2008)

2.2 Gate Oxide on SiC Substrate

The gate oxide is the dielectric layer that isolates the gate terminal of a MOS transistor from the underlying source and drain terminals as well as the conductive channel that links source and drain when the transistor is turned on (Figure 2.6). When there is no bias is applied to the gate with respect to the substrate, source and drain are isolated. In contrast, if the applied gate voltage is high enough, a thin conductive layer of electrons is induced in the substrate, and connects source and drain via a channel formation. In this condition, current can flow from source to drain if also a drain voltage is being applied as well (Zeghbroeck, 2011).

From the above description, it appears clearly that the operation of the MOS transistor is based on the insulating properties of the oxide layer. Therefore, it is crucial to understand the properties of thermally grown gate oxide on semiconductor substrate, particularly SiC substrate in this study. Generally, a MOS structure (Figure 2.7) is used to investigate the quality and reliability of the thermally grown oxide as it is a simple structure and easy to fabricate. Besides, it is also considered as the first step towards integration of MOSFET transistor. MOS structure provides considerable information regarding the properties of the oxide (SiO_2), the underlying semiconductor substrate (SiC) and the oxide/substrate (SiO_2/SiC) interface (Bentarzi, 2011).

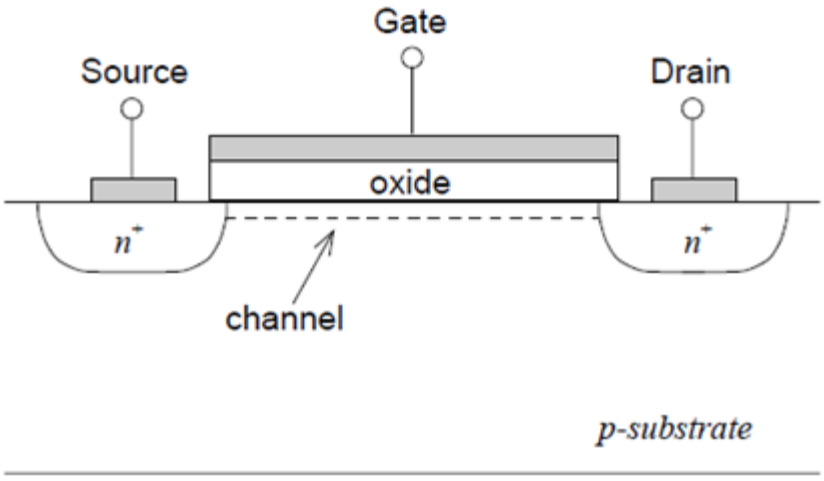

Figure 2.6: Schematic structure of a n-MOS transistor (Zeghbroeck, 2011)

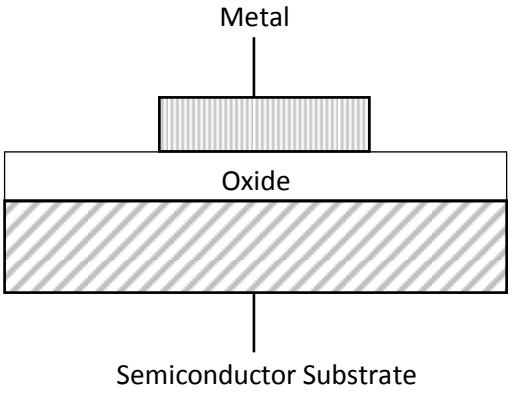

Figure 2.7: Schematic structure of a MOS structure (Bentarzi, 2011)

2.2.1 Importance of Thick Gate Oxide on SiC Substrate

Table 2.2 shows major applications of SiC MOSFET and respective voltage ratings. In terms of power MOSFETs for 600 V and higher voltage applications such as switch-mode power supplies, AC motor drives, solar inverters and automotive electronics (Hamada *et al.*, 2010), (Casady *et al.*, 1998), (Fairchild Semiconductor, 2007), (CREE Inc., 2012), a high-quality with relatively thick gate oxide subjected to high electric field is much needed (Takaya *et al.*, 2013), (Agarwal *et al.*, 2004). Below equation shows the dielectric constant ratio between the 4H-SiC and oxide:

$$\varepsilon_{ratio}=\frac{\varepsilon_{r,SiC}}{\varepsilon_{r,ox}} \tag{2.1}$$

where dielectric constant of SiC, $\varepsilon_{r,SiC}$ = 10 and dielectric constant of SiO_2, $\varepsilon_{r,ox}$ = 3.9. From the equation, it can be calculated that the electric field in the gate oxide would be roughly 2.5x higher than in SiC when the device is in blocking mode of operation (Agarwal *et al.*, 2004; Krishnaswami *et al.*, 2004).

The electric field in the SiC and gate oxide is given by the following equation:

$$E_{SiC}=E_{ox}\left(\frac{\varepsilon_{r,ox}}{\varepsilon_{r,SiC}}\right) \tag{2.2}$$

where E_{SiC} is the electric field in SiC and E_{ox} is the electric field in gate oxide. In order to insure long-term device reliability in SiO_2/4H-SiC system, the maximum surface electric field for SiC, $E_{SiC,}$ has to be kept approximately 1.2 MV/cm which is equivalent to 3 MV/cm of electric field in the gate oxide, E_{ox} (Agarwal *et al.*, 2004).

The gate oxide thickness can be related to the gate voltage and electric field in the gate oxide by the following expression:

$$t_{ox} = \frac{(V_G - \phi_{ms})}{E_{ox}} \tag{2.3}$$

where t_{ox} is the gate oxide thickness, V_G is the gate voltage and ϕ_{ms} is the metal – semiconductor work-function difference. Considering E_{ox}=3 MV/cm as the maximum electric field limitation value for 4H-SiC based gate oxide and ϕ_{ms} =0.45 V, a minimum gate oxide thickness of 50 nm is required in order to support gate voltage, V_G, of 15 V (Agarwal *et al.*, 2004; Gurfinkel *et al.*, 2008). On the other hand, as the gate voltage increases, the electric field in the oxide also increases, resulting in a large current flow into the oxide due to Fowler-Nordheim tunnelling which eventually leads to oxide breakdown (Agarwal *et al.*, 1997; Agarwal *et al.*, 2004; Gupta *et al.*, 2011). Hence, the need to thermally grow a thick SiO_2 gate (>50 nm) with good quality is crucial for high power devices applications.

Table 2.2: Major Applications of SiC-MOSFET in Motor Controls and Power Supplies (Majumdar, 2013)

Applications	**Voltage Ratings**
Home Appliances (refrigerator, air-conditioner and washing machines)	600 V
Automotive	600-1200 V
Elevators, UPS and Factory Automation, Power supplies, Alternative energy sources	600-1700 V
Electric Railway Systems, Metal Industries	1200-6500 V
Power network, Utilities	>10kV

2.2.2 Growth Mechanisms of Thermally Grown SiO_2 Films on SiC

The knowledge of thermal oxidation mechanisms on SiC is important in order to produce reliable and high-quality gate oxides for high power devices applications. Different quality of SiO_2/SiC interfaces are created by various oxide growth processing techniques. The mechanisms of thermally grown SiO_2 films on SiC is explained well using two common oxidation techniques which are dry and wet oxidation models. It is important to understand the effects associated to each models and use this knowledge for development of an optimized process conditions in particular for gate oxide growth in the industry-preferred environment.

2.2.2.1 Dry Oxidation Model

In general, the oxidation rate of SiC is more than one order of magnitude lower than that of Si (Harris and Afanas'ev, 1997). As a compound semiconductor, the reaction of SiC to form SiO_2 results in a by-product containing C. It is increasingly clear that C plays a detrimental role in the formation of a high quality oxide (Harris and Afanas'ev, 1997). It has been shown that the oxidation kinetics of SiC is described by the same kinetics rules as oxidation of Si, as defined by Deal and Grove. In the beginning, oxidation is limited by reactions at the SiO_2/SiC interface. Then, once an oxide layer is formed, the oxidizing species have to pass through this oxide layer (Harris and Afanas'ev, 1997). For increasing oxide thickness there will be a point at which the reaction is oxygen deficient and a parabolic dependence sets in leading to some speculation that the reaction should be limited by the out-diffusion of CO.This growth law could be written as:

$$x^2 + Ax = B(t + \tau), \tag{2.4}$$

where x is the oxide thickness and *t* is the oxidation time. When a thermal oxide thickness, *x*, is formed, 0.45*x* of the thickness of SiC is consumed (Raynaud, 2001). The time constant, τ, determines the thickness of the initial oxide layer. Ratio *B/A* is called the linear rate and is proportional to the reaction rate of the slowest reaction. Constant *B* is proportional to the diffusion coefficient and is called the parabolic rate. These two constants are thermally activated as exp ($-E_{B/A}/kT$) and exp ($-E_B/kT$) for the linear and parabolic rate, respectively (Raynaud, 2001).

Contrary to the relatively simple oxidation of Si, there are five major steps in the thermal oxidation of SiC (Gupta and Akhtar, 2011):

1. Transport of molecular oxygen gas to the oxide surface.
2. In-diffusion of oxygen through the oxide film.
3. Reactions with SiC at the oxide/SiC interface.
4. Out-diffusion of product gases (e.g., CO_2) through the oxide film.
5. Removals of product gases away from the oxide surface.

The last two steps are not involved in the oxidation of Si. The first and last steps are rapid and the fact that the reaction rate is not constant over time shows that this is not the rate limiting step but diffusion limited model. The principal chemical reactions that can occur at the SiC interface are as following expressions (Harris and Afanas'ev, 1997):

$$SiC + \frac{3}{2}\, O_2 \leftrightarrow\ SiO_2 + CO, \tag{2.5}$$

$$SiC + O_2 \leftrightarrow SiO_2 + C, \tag{2.6}$$

In addition there are a number of secondary reactions that will determine the equilibrium at the reaction interface:

$$SiC + 2CO \leftrightarrow 3C + SiO_2\,, \tag{2.7}$$

$$2C + O_2 \leftrightarrow 2CO, \tag{2.8}$$

Comparing molecular diameters CO has approximately the same size as molecular oxygen at 1000°C and would therefore be expected to have a similar diffusivity. The oxidation rate is a strong dependence on crystal orientation, face, polytype, doping density type and concentration (Harris and Afanas'ev, 1997). However, Deal-Grove model cannot explained the growth rate in thin oxide regime (< 20 nm) (Hijikata *et al.*, 2009) as reported in Si. A good fitting could not be achieved with any values *B/A* and *B*, though the fittings are well in the oxide thickness larger than 20 nm (Hijikata *et al.*, 2009).

On the other hand, 'Si-C emission' model describes the SiC oxidation process better than the Deal-Grove model (Hijikata *et al.*, 2009). In 'Si-C emission' model, the interfacial Si and C emission accompanied by the oxidation of SiC, showed that the model well reproduced the oxide growth rates of SiC at the entire thickness range both for the (0001)Si-face and (000-1) C-face.

Taking into account that Si and C atoms emitted from the interface during the oxidation, the reaction equation for SiC oxidation can be written as (Hijikata *et al.*, 2009):

$$\mathrm{SiC} + \left(2 - v_{Si} - v_c - \frac{\alpha}{2}\right)\mathrm{O}_2 \rightarrow (1 - v_{Si})SiO_2 + v_{Si}Si + v_cC + \alpha\mathrm{CO} + (1 - v_c - \alpha)CO_2\,, \tag{2.9}$$

where v and α denote the interfacial emission rate and the production rate of CO, respectively, and the subscripts, Si and C, denote the values for the corresponding atoms. Interfacial reaction rate for SiC oxidation (k) is thought to be suppressed by the accumulation of Si atoms and C atoms emitted near the interface, k is given by multiplying decreasing functions for Si and C (Hijikata *et al.*, 2009):

$$k = k_0 \left(1-\frac{C_{Si}^1}{C_{Si}^0}\right)\left(1 - \frac{C_C^0}{C_C^0}\right), \tag{2.10}$$

where $C^1$and C^0 are the interfacial concentration of corresponding interstitials and the solubility limit the corresponding interstitials in the oxide, respectively, and k_0 is the interfacial reaction rate when oxide thickness nearly equals zero, i.e. intrinsic interfacial interaction rate without influence of the accumulation of emitted Si and C atoms.

Higher oxidation temperatures result in the higher areal densities of Si interstitials regardless of Si- and C-face. The decline of C_{Si} with respect to the distance from the interface for Si-face is little dependent on oxidation temperature, in contrast, that for C-face decreases remarkably with decreasing oxidation temperature. In comparison of Si- and C-face, C_{Si} for Si-face is higher than that for C-face regardless of temperature. The concentration of C interstitials C_{C} is nearly constant against the distance from the interface at any temperature for both of Si- and C-faces and this indicates that C interstitials rapidly diffuse through the oxide. Likewise the case of Si interstitials, the higher oxidation temperatures bring about the higher concentrations of C interstitials regardless of Si- and C-face. In comparison of Si- and C-face, the C_{C} for Si-face is lower than that for C-face at any temperatures, which is opposite to the case of Si interstitials. The SiC–oxide

interface structure can also be discussed on the basis of Si-C emission model, leading to the estimation of D_{it} (Hijikata *et al.*, 2009).

Besides Deal-Grove and Si-C emission models, first principles simulation suggests that oxygen molecules are dissociated in the SiO_2 layers or by Si atoms at the SiO_2 interface. The O atoms of the O_2 molecule oxidize the C atoms at the SiC interface and form Si-C-O or CO_2-C complexes. CO_x (x=1 or 2) molecules are desorbed from these complexes by thermal motion. CO_x molecules diffuse in the SiO_2 layers when they do not react with dangling bonds. CO_x molecule being formed during C-face oxidation is more easily diffuse than those formed during Si-face oxidation in the interface region (Ohnuma et al., 2007). A single carbon residing within the interfacial region of the SiO_2 results in a Si-C-Si bridge and an oxygen protrusion. This carbon atom is close to the conduction band edge associated with the carbon dangling bond (Rozen *et al*., 2009b).

2.2.2.2 Wet Oxidation Model

In the case of wet oxidation, only a few literatures have been reported on the mechanisms involved during oxide growth on SiC. Based on the reported literature (Raynaud, 2001), the growth rate can be fitted by linear-parabolic functions independently of the SiC terminal face. During the linear growth, activation energy, $E_{B/A}$, is 3 eV, which is within the range of the binding energy of SiC. Therefore, the disruption of Si-C bonds explains rather well the activation energies. During parabolic growth, E_B is much larger than the activation energy of 0.79 eV found for the diffusion of H_2O. This proves that the oxidation process is not limited by the diffusion of H_2O, whereas, the limiting factor is the out-diffusion of CO or the diffusion of O_2 (Raynaud, 2001).